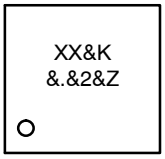
Fixed-Output Synchronous Regulator, TINYBOOST®, 2.5 MHz

FAN48610

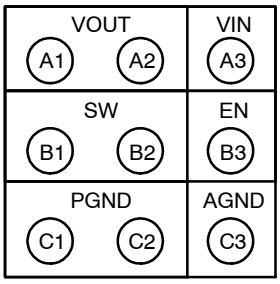
WLCSP9
CASE 567QW

MARKING DIAGRAM



XX = KA / KF / KN
&K = Lot Code
&. = Alphabetical Year Code
&2 = Numeric Date Code
&Z = Assembly Plant Code

PIN ASSIGNMENT



(Top View)

ORDERING INFORMATION

See detailed ordering and shipping information on page 2 of this data sheet.

NOTE: Some of the devices on this data sheet have been **DISCONTINUED**. Please refer to the table on page 2.

Description

The FAN48610 is a low-power boost regulator designed to provide a minimum voltage-regulated rail from a standard single-cell Li-Ion battery and advanced battery chemistries. Even below the minimum system battery voltage, the device maintains the output voltage regulation for a minimum output load current of 1.0 A. The combination of built-in power transistors, synchronous rectification, and low supply current suit the FAN48610 for battery-powered applications.

The FAN48610 is available in a 9-bump, 0.4 mm pitch, Wafer-Level Chip-Scale Package (WLCSP).

Features

- Input Voltage Range: 2.5 V to 4.8 V
- Output Voltages Range: 3.0 V to 5.0 V
- I_{OUT} ≥ 1 A at V_{OUT} = 5.0 V, V_{IN} ≥ 2.5 V
- I_{OUT} ≥ 1.5 A at V_{OUT} = 5.0 V, V_{IN} ≥ 3.0 V
- Up to 94% Efficient
- Internal Synchronous Rectification
- Soft-Start with True Load Disconnect
- Short-Circuit Protection
- 9-Bump, 1.215 mm × 1.215 mm, 0.4 mm Pitch WLCSP
- Three External Components: 2016 0.47 μH Inductor, 0603 Case Size Input / Output Capacitors
- Total Application Board Solution Size: < 11 mm^2

Applications

- Class-D Audio Amplifier and USB OTG Supply
- Boost for Low-Voltage Li-Ion Batteries
- Smart Phones, Tablets, Portable Devices, Wearables

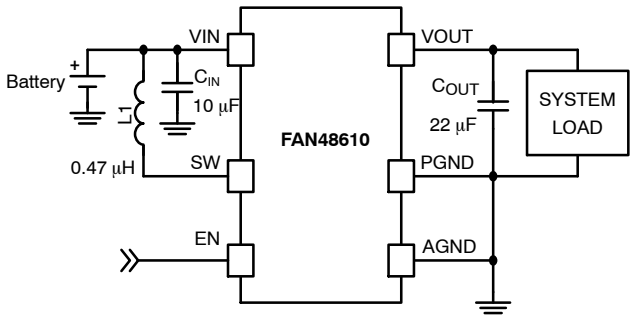


Figure 1. Typical Application

Table 1. ORDERING INFORMATION

Part Number	V_{OUT}	Operating Temperature	Package	Packing†	Device Marking
FAN48610UC50X	5.0 V	−40 °C to 85 °C	WLCSP, 0.4 mm Pitch	Tape and Reel	KF
FAN48610BUC50X (Note 2)					
FAN48610BUC45X (Note 2)	4.5 V				KA

DISCONTINUED (Note 1)

FAN48610BUC33X (Note 2)	3.3 V	−40 °C to 85 °C	WLCSP, 0.4 mm Pitch	Tape and Reel	KN

† For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

1. **DISCONTINUED:** This device is not recommended for new design. Please contact your **onsemi** representative for information. The most current information on this device may be available on www.onsemi.com.
2. Includes backside lamination.

BLOCK DIAGRAM

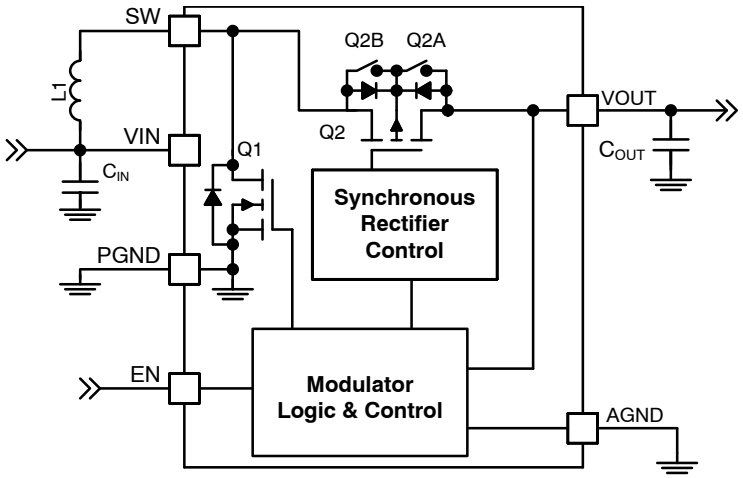


Figure 2. IC Block Diagram

Table 2. RECOMMENDED COMPONENTS

Component	Description	Ventor	Parameter	Typ.	Unit
L1	0.47 μH, 30%, 2016	Toko: DFE201612C DFR201612C Cyntec: PIFE20161B	L	0.47	μH
			DCR (Series R)	40	mΩ
C_{IN}	10 μF, 10%, 6.3 V, X5R, 0603	Murata: GRM188R60J106K TDK: C1608X5R0J106K	C	10	μF
C_{OUT}	22 μF, 20%, 6.3 V, X5R, 0603	TDK: C1608X5R0J226M	C	22	μF

PIN CONFIGURATION

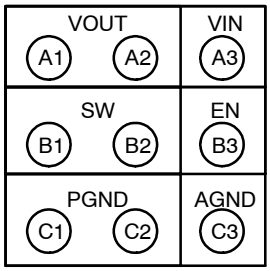


Figure 3. Top View

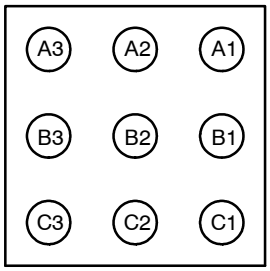


Figure 4. Bottom View

Table 3. PIN DEFINITIONS

Pin #	Name	Description
A1, A2	VOUT	**Output Voltage**. This pin is the output voltage terminal; connect directly to C_{OUT}.
A3	VIN	**Input Voltage**. Connect to Li-Ion battery input power source and the bias supply for the gate drivers.
B1, B2	SW	**Switching Node**. Connect to inductor.
B3	EN	**Enable.** When this pin is HIGH, the circuit is enabled.
C1, C2	PGND	**Power Ground**. This is the power return for the IC. C_{OUT} capacitor should be returned with the shortest path possible to these pins.
C3	AGND	**Analog Ground**. This is the signal ground reference for the IC. All voltage levels are measured with respect to this pin – connect to PGND at a single point.

Table 4. ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter		Min.	Max.	Unit
V_{IN}	Voltage on VIN Pin		−0.3	6.0	V
V_{OUT}	Voltage on VOUT Pin		−0.3	6.0	V
SW	SW Node	DC	−0.3	6.0	V
		Transient: 10 ns, 3 MHz	−1.0	8.0	
V_{CC}	Voltage on Other Pins		−0.3	6.0 (Note 3)	V
ESD	Electrostatic Discharge Protection Level	Human Body Model per JESD22-A114	2		kV
		Charged Device Model per JESD22-C101	1		
T_J	Junction Temperature		−40	+150	°C
T_{STG}	Storage Temperature		−65	+150	°C
T_L	Lead Soldering Temperature, 10 Seconds			+260	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

3. Lesser of 6.0 V or V_{IN} + 0.3 V.

Table 5. RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min.	Max.	Unit
V_{IN}	Supply Voltage	2.5	4.8	V
I_{OUT}	Maximum Output Current	1000		mA
T_A	Ambient Temperature	–40	+85	°C
T_J	Junction Temperature	–40	+125	°C

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

Table 6. THERMAL PROPERTIES

Symbol	Parameter	Typical	Unit
θ_{JA}	Junction-to-Ambient Thermal Resistance	50	°C/W

Junction-to-ambient thermal resistance is a function of application and board layout. This data is measured with four-layer 2s2p boards in accordance to JEDEC standard JESD51. Special attention must be paid not to exceed junction temperature $T_{J(max)}$ at a given ambient temperate T_A.

Table 7. ELECTRICAL CHARACTERISTICS
(Recommended operating conditions, unless otherwise noted, circuit per Figure 1, V_{OUT}= 3.0 V to 5.0 V, V_{IN} = 2.5 V to 4.5 V, T_A = –40 °C to 85 °C. Typical values are given V_{IN} = 3.6 V and T_A = 25 °C)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
POWER SUPPLY						
I_Q	V_{IN} Quiescent Current	V_{IN} = 3.6 V, I_{OUT} = 0 A, EN = V_{IN}		85	125	μA
		Shutdown: EN = 0, V_{IN} = 3.6 V		3	10	
V_{UVLO}	Under-Voltage Lockout	V_{IN} Rising		2.2	2.3	V
V_{UVLO_HYS}	Under-Voltage Lockout Hysteresis			150		mV
INPUTS						
V_{IH}	Enable HIGH Voltage		1.05			V
V_{IL}	Enable LOW Voltage				0.4	V
I_{PD}	Current Sink Pull-Down	EN Pin, Logic HIGH		100		nA
R_{LOW}	Low-State Active Pull-Down	EN Pin, Logic LOW	200	300	400	kΩ
OUTPUTS						
V_{REG}	Output Voltage Accuracy DC (Note 4)	Referred to V_{OUT}, 2.5 V ≤ V_{IN} ≤ V_{OUT} –150 mV	–2		4	%
I_{LK_OUT}	VIN-to-VOUT Leakage Current	V_{OUT} = 0, EN = 0, V_{IN} = 4.2 V			1	μA
I_{LK}	VOUT-to-VIN Reverse Leakage Current	V_{OUT} = 5.0 V, EN = 0, V_{IN} = 2.5 V			3.5	μA
V_{TRSP}	Output Voltage Accuracy Transient (Note 5)	Referred to V_{OUT}, 50–500 mA Load Step	–5		5	%
TIMING						
f_{SW}	Switching Frequency	V_{IN} = 3.6 V, V_{OUT} = 5.0 V, Load = 1000 mA	2.0	2.5	3.0	MHz
t_{SS}	Soft-Start EN HIGH to Regulation (Note 5)	50 Ω Load, V_{OUT} = 5.0 V		600		μA
t_{RST}	FAULT Restart Timer (Note 5)			20		ms

Table 7. ELECTRICAL CHARACTERISTICS (continued)
(Recommended operating conditions, unless otherwise noted, circuit per Figure 1, V_{OUT}= 3.0 V to 5.0 V, V_{IN} = 2.5 V to 4.5 V, T_A = −40 °C to 85 °C. Typical values are given V_{IN} = 3.6 V and T_A = 25 °C)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
POWER STAGE						
$R_{DS(ON)N}$	N-Channel Boost Switch $R_{DS(ON)}$	V_{IN} = 3.6 V, V_{OUT} = 5.0 V		80	130	mΩ
$R_{DS(ON)P}$	P-Channel Sync. Rectifier $R_{DS(ON)}$	V_{IN} = 3.6 V, V_{OUT} = 5.0 V		65	115	mΩ
I_{V_LIM}	Boost Valley Current Limit	V_{OUT} = 5.0 V		3.00	3.85	A
$I_{V\_LIM\_SS}$	Boost Soft-Start Valley Current Limit	V_{IN} < V_{OUT} < V_{OUT_TARGET}, SS Mode		1.7		A
$V_{MIN\_1.0A}$	Minimum V_{IN} for 1000 mA Load (Note 5)	V_{OUT} = 5.0 V		2.5		V
$V_{MIN\_1.5A}$	Minimum V_{IN} for 1500 mA Load (Note 5)	V_{OUT} = 5.0 V		3.0		V
T_{150T}	Over-Temperature Protection (OTP)			150		°C
T_{150H}	OTP Hysteresis			20		°C

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

4. DC I_{LOAD} from 0 to 1 A. V_{OUT} measured from mid-point of output voltage ripple. Effective capacitance of $C_{OUT} \geq 3$ μF.
5. Guaranteed by design and characterization; not tested in production.

TYPICAL CHARACTERISTICS

(UNLESS OTHERWISE SPECIFIED; V_{IN} = 3.6 V, V_{OUT} = 5.0 V, T_A = 25 °C, AND CIRCUIT AND COMPONENTS ACCORDING TO FIGURE 1)

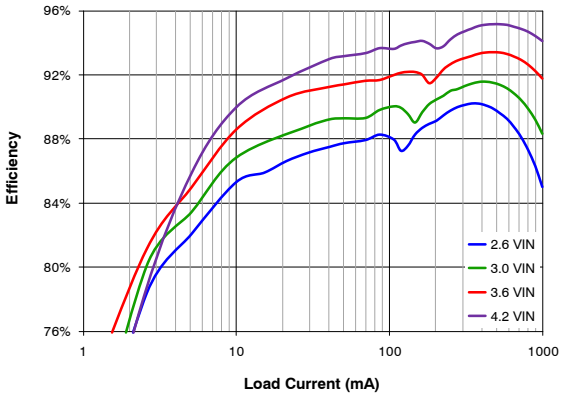


Figure 5. Efficiency vs. Load Current and Input Voltage

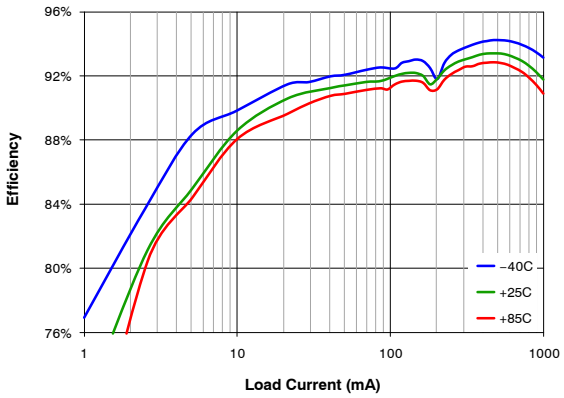


Figure 6. Efficiency vs. Load Current and Temperature

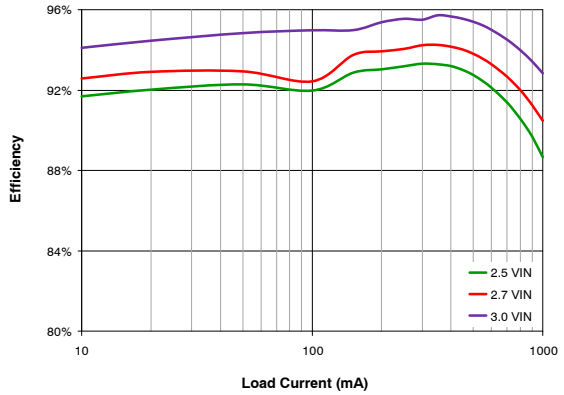


Figure 7. Efficiency vs. Load Current and Input Voltage, V_{OUT} = 3.3 V

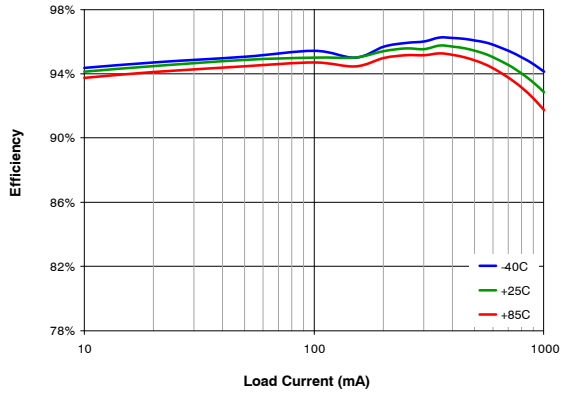


Figure 8. Efficiency vs. Load Current and Temperature, V_{IN} = 3.0 V, V_{OUT} = 3.3 V

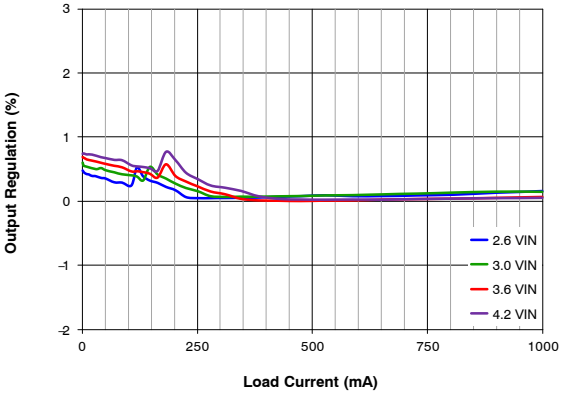


Figure 9. Output Regulation vs. Load Current and Input Voltage (Normalized to 3.6 V_{IN}, 500 mA Load)

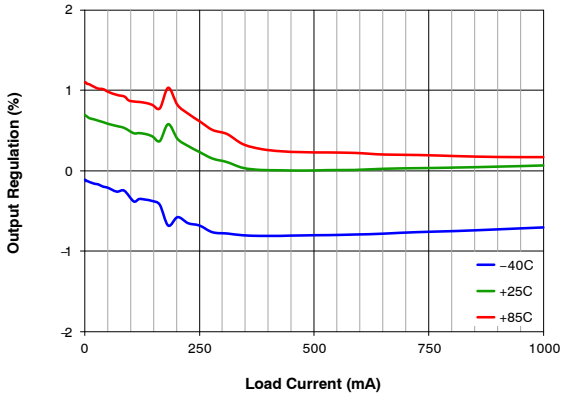


Figure 10. Output Regulation vs. Load Current and Temperature (Normalized to 3.6 V_{IN}, 500 mA Load, T_A = 25°C)

TYPICAL CHARACTERISTICS

(UNLESS OTHERWISE SPECIFIED; V_{IN} = 3.6 V, V_{OUT} = 5.0 V, T_A = 25 °C, AND CIRCUIT AND COMPONENTS ACCORDING TO FIGURE 1)

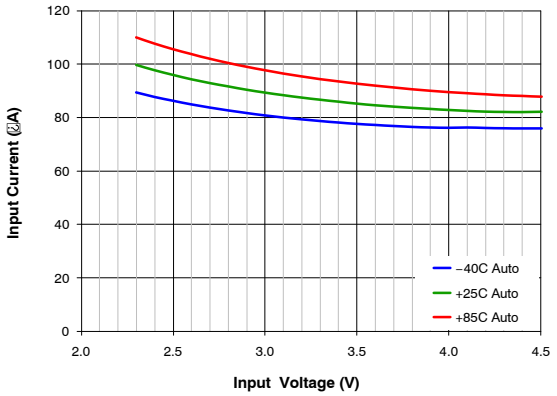


Figure 11. Quiescent Current vs. Input Voltage, Temperature

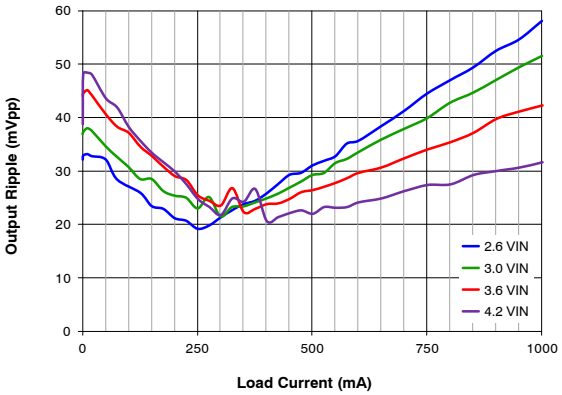


Figure 12. Output Ripple vs. Load Current and Input Voltage

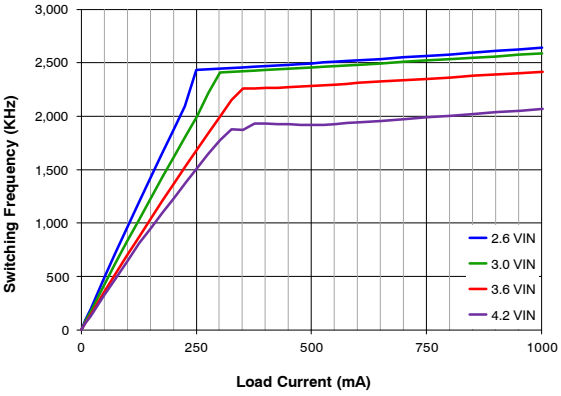


Figure 13. Frequency vs. Load Current and Input Voltage

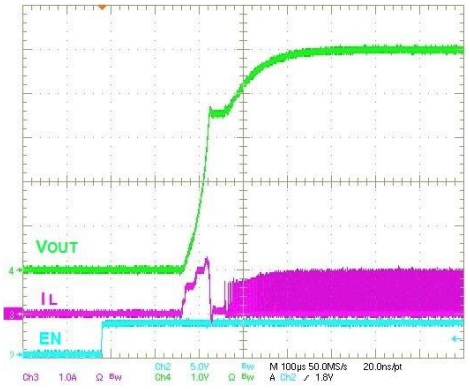


Figure 14. Startup, 50 Ω Load

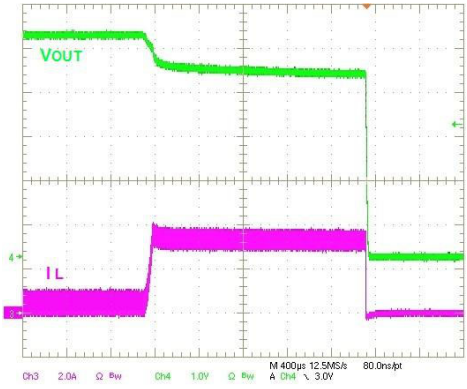


Figure 15. Overload Protection

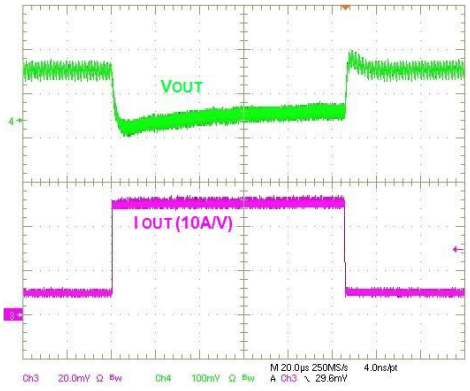


Figure 16. Load Transient, 100–500 mA, 100 ns Edge

TYPICAL CHARACTERISTICS

(UNLESS OTHERWISE SPECIFIED; V_{IN} = 3.6 V, V_{OUT} = 5.0 V, T_A = 25 °C, AND CIRCUIT AND COMPONENTS ACCORDING TO FIGURE 1)

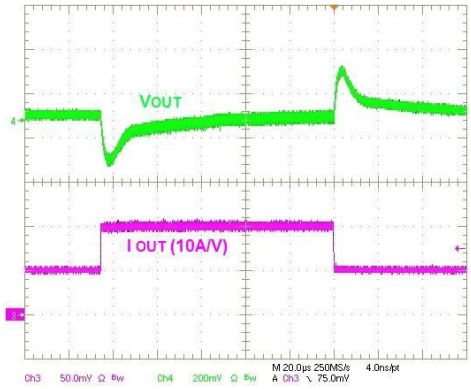


Figure 17. Load Transient, 500–1000 mA, 100 ns Edge

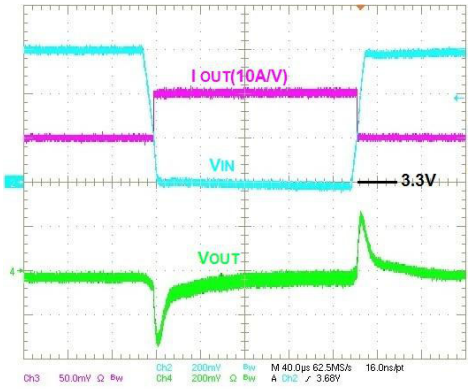


Figure 18. Simultaneous Line / Load Transient, 3.3 –3.9 V_{IN}, 10 μs Edge, 500–1000 mA Load, 100 ns Edge

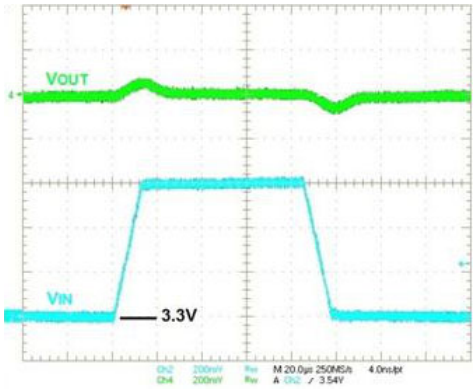


Figure 19. Line Transient, 3.3–3.9 V_{IN}, 10 μs Edge, 500 mA Load

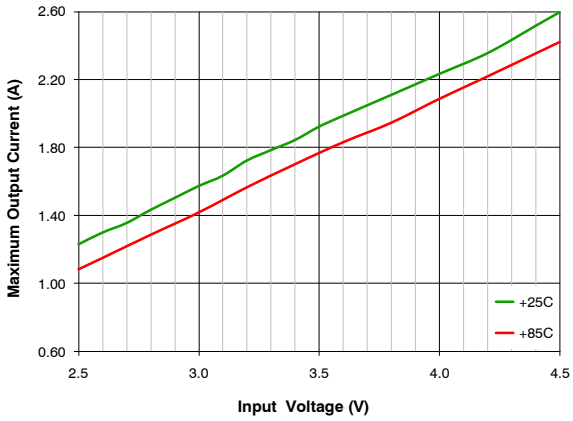


Figure 20. Typical Maximum Output Current vs. Input Voltage

CIRCUIT DESCRIPTION

FAN48610 is a synchronous boost regulator, typically operating at 2.5 MHz in Continuous Conduction Mode (CCM), which occurs at moderate to heavy load current and low V_{IN} voltages. The regulator's Pass-Through Mode automatically activates when V_{IN} is above the boost regulator's set point.

Table 8. OPERATING MODES

Mode	Description	Invoked When:
LIN	Linear Startup	$V_{IN} > V_{OUT}$
SS	Boost Soft-Start	$V_{IN} < V_{OUT} < V_{OUT(TARGET)}$
BST	Boost Operating Mode	$V_{OUT} = V_{OUT(TARGET)}$
PT	Pass-Through Mode	$V_{IN} > V_{OUT(TARGET)}$

Boost Mode Regulation

The FAN48610 uses a current-mode modulator to achieve excellent transient response and smooth transitions between CCM and DCM operation. During CCM operation, the device maintains a switching frequency of about 2.5 MHz. In lightload operation (DCM), frequency is naturally reduced to maintain high efficiency.

Shutdown and Startup

When EN is LOW, all bias circuits are off and the regulator is in Shutdown Mode. During shutdown, current flow is prevented from VIN to VOUT, as well as reverse flow from VOUT to VIN. It is recommended to keep load current draw below 500 mA until the devices successfully executes startup. The following table describes the startup sequence.

Table 9. BOOST STARTUP SEQUENCE

Start Mode	Entry	Exit	End Mode	Timeout (μs)
LIN1	$V_{IN} > V_{UVLO}$, EN = 1	$V_{OUT} > V_{IN} - 300$ mV	SS	
		TIMEOUT	LIN2	512
LIN2	LIN1 Exit	$V_{OUT} > V_{IN} - 300$ mV	SS	
		TIMEOUT	FAULT	1024
SS	LIN1 or LIN2 Exit	$V_{OUT} = V_{OUT(TARGET)}$	BST	
		OVERLOAD TIMEOUT	FAULT	64

LIN Mode

When EN is HIGH and $V_{IN} > V_{UVLO}$, the regulator first attempts to bring V_{OUT} within 300 mV of V_{IN} by using the internal fixed-current source from VIN (Q2). The current is limited to the LIN1 set point.

If V_{OUT} reaches $V_{IN} - 300$ mV during LIN1 Mode, the SS Mode is initiated. Otherwise, LIN1 times out after 512 μs and LIN2 Mode is entered.

In LIN2 Mode, the current source is incremented to 1.6 A. If V_{OUT} fails to reach $V_{IN} - 300$ mV after 1024 μs, a fault condition is declared and the device waits 20 ms to attempt an automatic restart.

Soft-Start (SS) Mode

Upon the successful completion of LIN Mode ($V_{OUT} \geq V_{IN} - 300$ mV), the regulator begins switching with boost pulses current limited to 50% of nominal level.

During SS Mode, if V_{OUT} fails to reach regulation during the SS ramp sequence for more than 64 μs, a fault is declared. If large C_{OUT} is used, the reference is automatically stepped slower to avoid excessive input current draw.

Boost (BST) Mode

This is a normal operating mode of the regulator.

Pass-Through (PT) Mode

In normal operation, the device automatically transitions from Boost Mode to Pass-Through Mode if V_{IN} goes above the target V_{OUT}. In Pass-Through Mode, the device fully enhances Q2 to provide a very low impedance path from VIN to VOUT. Entry to the Pass-Through Mode is triggered by condition where $V_{IN} > V_{OUT}$ and no switching has occurred during the past 5 μs. To soften the entry into Pass-Through Mode, Q2 is driven as a linear current source for the first 5 μs. Pass-Through Mode exit is triggered when V_{OUT} reaches the target V_{OUT} voltage. During Automatic Pass-Through Mode, the device is short-circuit protected by a voltage comparator tracking the voltage drop from V_{IN} to V_{OUT}; if the drop exceeds 300 mV, a fault is declared.

Fault State

The regulator enters Fault State under any of the following conditions:

- V_{OUT} fails to achieve the voltage required to advance from LIN Mode to SS Mode.
- V_{OUT} fails to achieve the voltage required to advance from SS Mode to BST Mode.
- Boost current limit triggers for 2 ms during BST Mode.

- $V_{IN} - V_{OUT} > 300$ mV; this fault can occur only after successful completion of the soft-start sequence.
- $V_{IN} < V_{UVLO}$.

Once a fault is triggered, the regulator stops switching and presents a high-impedance path between VIN and VOUT. After waiting 20 ms, an automatic restart is attempted.

Over-Temperature

The regulator shuts down if the die temperature exceeds 150 °C. Restart occurs when the IC has cooled by approximately 20°C.

APPLICATION INFORMATION

Output Capacitance (C_{OUT})

The effective capacitance (C_{EFF} (Note 6)) of small, high-value ceramic capacitors decreases as their bias voltage increases, as illustrated in the graph below:

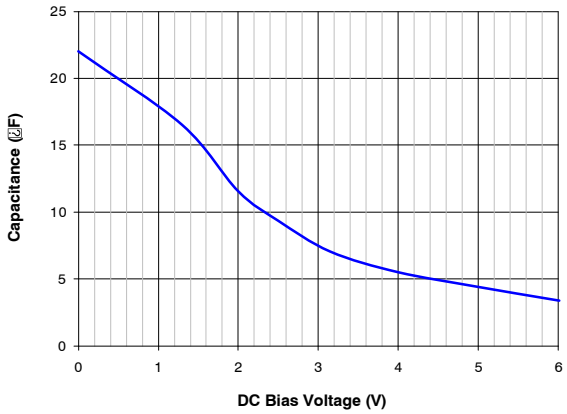


Figure 21. C_{EFF} for 22 µF, 0603, X5R, 6.3 V-Rated Capacitor (TDK C1608X5R0J226M)

FAN48610 is guaranteed for stable operation with the minimum value of C_{EFF} ($C_{EFF(MIN)}$) outlined in Table 10.

Table 10. MINIMUM C_{EFF} REQUIRED FOR STABILITY

Operating Conditions			$C_{EFF(MIN)}$ (µF)
V_{OUT} (V)	V_{IN} (V)	I_{LOAD} (mA)	
5.0	2.5 to 4.5	0 to 1000	3.0

6. C_{EFF} varies by manufacturer, capacitor material, and case size.

Introduction Selection

Recommended nominal inductance value is 0.47 µH. The FAN48610 employs valley-current limiting, so peak inductor current can reach 3.8 A for a short duration during overload conditions. Saturation effects cause the inductor current ripple to become higher under high loading, as only the valley of the inductor current ripple is controlled.

Startup

Input current limiting is in effect during soft-start, which limits the current available to charge C_{OUT} and any additional capacitance on the V_{OUT} line. If the output fails to achieve regulation within the limits described in the Soft-Start section above, a fault occurs, causing the circuit to shut down. It waits about 20 ms before attempting a restart. If the total combined output capacitance is very high, the circuit may not start on the first attempt, but eventually achieves regulation if no load is present. If a high current load and high capacitance are both present during soft-start, the circuit may fail to achieve regulation and continually attempt soft-start, only to have the output capacitance discharged by the load when in Fault State.

Output Voltage Ripple

Output voltage ripple is inversely proportional to C_{OUT}. During t_{ON}, when the boost switch is on, all load current is supplied by C_{OUT}.

$$V_{RIPPLE(P-P)} = t_{ON} \cdot \frac{I_{LOAD}}{C_{OUT}} \quad \text{(eq. 1)}$$

And

$$t_{ON} = t_{SW} \cdot D = t_{SW} \cdot \left(1 - \frac{V_{IN}}{V_{OUT}}\right) \quad \text{(eq. 2)}$$

therefore:

$$V_{RIPPLE(P-P)} = t_{SW} \cdot \left(1 - \frac{V_{IN}}{V_{OUT}}\right) \cdot \frac{I_{LOAD}}{C_{OUT}} \quad \text{(eq. 3)}$$

$$t_{SW} = \frac{1}{f_{SW}} \quad \text{(eq. 4)}$$

The maximum V_{RIPPLE} occurs when V_{IN} is minimum and I_{LOAD} is maximum. For better ripple performance, more output capacitance can be added.

Layout Recommendations

The layout recommendations below highlight various topcopper pours by using different colors.

To minimize spikes at VOUT, C_{OUT} must be placed as close as possible to PGND and VOUT, as shown below.

For thermal reasons, it is suggested to maximize the pour area for all planes other than SW. Especially the ground pour should be set to fill all available PCB surface area and tied to internal layers with a cluster of thermal vias.

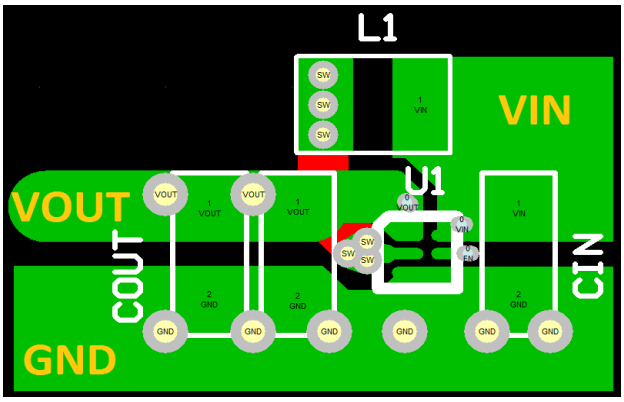
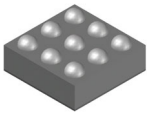


Figure 22. Layout Recommendation

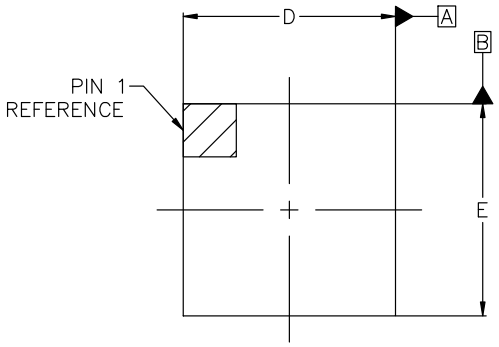
PRODUCT-SPECIFIC DIMENSIONS (This table pertains to the package information on the following page.)

D	E	X	Y
1.215 ±0.030 mm	1.215 ±0.030 mm	0.2075 mm	0.2075 mm

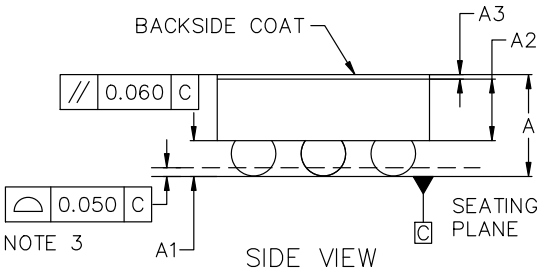


WLCSP−9 1.22x1.22x0.38, 0.40P
CASE 567QW
ISSUE C

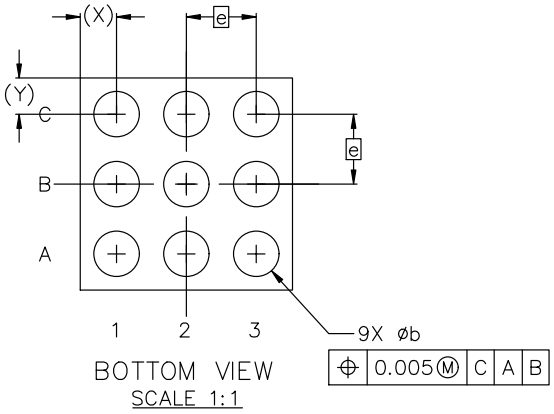
DATE 11 MAY 2026



TOP VIEW
SCALE 1:1



SIDE VIEW
SCALE 1:1

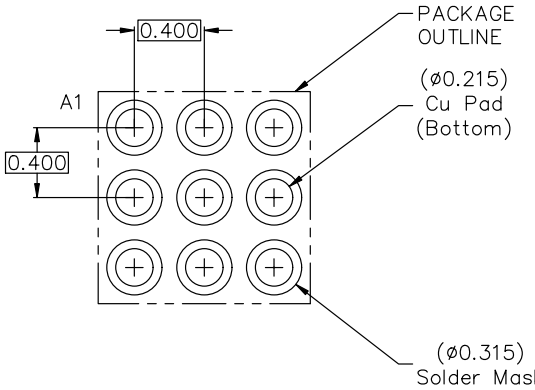


BOTTOM VIEW
SCALE 1:1

NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 2018.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. COPLANARITY APPLIES TO THE SPHERICAL CROWNS OF THE SOLDER BALLS.
4. DATUM C, THE SEATING PLANE, IS DEFINED BY THE SPHERICAL CROWNS OF THE SOLDER BALLS.
5. DIMENSION b IS MEASURED AT THE MAXIMUM SOLDER BALL DIAMETER PARALLEL TO DATUM C.

DIM	MILLIMETERS		
	MIN.	NOM.	MAX.
A	0.542	0.581	0.620
A1	0.183	0.203	0.223
A2	0.335	0.353	0.371
A3	0.022	0.025	0.027
b	0.240	0.260	0.280
D	1.185	1.215	1.245
E	1.185	1.215	1.245
e	0.400 BSC		
X	0.208 REF.		
Y	0.208 REF.		



RECOMMENDED MOUNTING FOOTPRINT

*FOR ADDITIONAL INFORMATION ON OUR Pb−FREE STRATEGY AND SOLDERING DETAILS, PLEASE DOWNLOAD THE ONSEMI SOLDERING AND MOUNTING TECHNIQUES REFERENCE MANUAL, SOLDERRM/D.

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