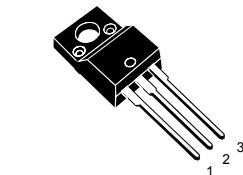
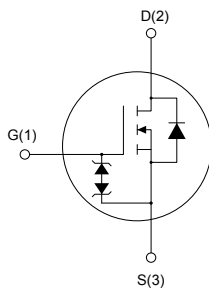


## N-channel 650 V, 1.1 $\Omega$ typ., 5.4 A MDmesh K3 Power MOSFET in a TO-220FP package



TO-220FP



AM01476v1


**Product status link**
[STF6N65K3](#)
**Product summary**

|                   |           |
|-------------------|-----------|
| <b>Order code</b> | STF6N65K3 |
| <b>Marking</b>    | 6N65K3    |
| <b>Package</b>    | TO-220FP  |
| <b>Packing</b>    | Tube      |

### Features

| Order code | $V_{DS}$ | $R_{DS(on)}$ max. | $I_D$ |
|------------|----------|-------------------|-------|
| STF6N65K3  | 650 V    | 1.3 $\Omega$      | 5.4 A |

- 100% avalanche tested
- Extremely high dv/dt capability
- Very low intrinsic capacitance
- Improved diode reverse recovery characteristics
- Zener-protected

### Applications

- Switching applications

### Description

This MDmesh K3 Power MOSFET is the result of improvements applied to STMicroelectronics' MDmesh technology, combined with a new optimized vertical structure. This device boasts an extremely low on-resistance, superior dynamic performance and high avalanche capability, rendering it suitable for the most demanding applications.

# 1 Electrical ratings

**Table 1. Absolute maximum ratings**

| Symbol         | Parameter   | Value      | Unit |
|----------------|---|------------|------|
| $V_{DS}$       | Drain-source voltage  | 650        | V    |
| $V_{GS}$       | Gate-source voltage   | ±30        | V    |
| $I_D$          | Drain current (continuous) at $T_C = 25\text{ °C}$  | 5.4        | A    |
|                | Drain current (continuous) at $T_C = 100\text{ °C}$   | 3          |      |
| $I_{DM}^{(1)}$ | Drain current (pulsed)  | 21.6       | A    |
| $P_{TOT}$      | Total power dissipation at $T_C = 25\text{ °C}$   | 30         | W    |
| $dv/dt^{(2)}$  | Peak diode recovery voltage slope   | 12         | V/ns |
| ESD            | Gate-source human body model ( $R = 1.5\text{ k}\Omega$ , $C = 100\text{ pF}$ )   | 2.5        | kV   |
| $V_{ISO}$      | Insulation withstand voltage (RMS) from all three leads to external heat sink ( $t = 1\text{ s}$ , $T_C = 25\text{ °C}$ ) | 2.5        | kV   |
| $T_{stg}$      | Storage temperature range   | -55 to 150 | °C   |
| $T_J$          | Maximum operating junction temperature  | 150        | °C   |

1. Pulse width is limited by safe operating area.

2.  $I_{SD} \leq 5.4\text{ A}$ ,  $di/dt = 400\text{ A}/\mu\text{s}$ ,  $V_{DD} = 520\text{ V}$ .

**Table 2. Thermal data**

| Symbol     | Parameter                               | Value | Unit |
|------------|---|-------|------|
| $R_{thJC}$ | Thermal resistance, junction-to-case    | 4.17  | °C/W |
| $R_{thJA}$ | Thermal resistance, junction-to-ambient | 62.5  | °C/W |

**Table 3. Avalanche characteristics**

| Symbol   | Parameter  | Value | Unit |
|----------|--|-------|------|
| $I_{AR}$ | Avalanche current, repetitive or non-repetitive (pulse width limited by $T_J$ max.)                      | 5.4   | A    |
| $E_{AS}$ | Single pulse avalanche energy (starting $T_J = 25\text{ °C}$ , $I_D = I_{AR}$ , $V_{DD} = 50\text{ V}$ ) | 100   | mJ   |

## 2 Electrical characteristics

$T_C = 25\text{ °C}$  unless otherwise specified.

**Table 4. Static**

| Symbol        | Parameter                         | Test conditions   | Min. | Typ. | Max.    | Unit          |
|---------------|-----------------------------------|---|------|------|---------|---------------|
| $V_{(BR)DSS}$ | Drain-source breakdown voltage    | $V_{GS} = 0\text{ V}$ , $I_D = 1\text{ mA}$                                   | 650  | -    | -       | V             |
| $I_{DSS}$     | Zero gate voltage drain current   | $V_{GS} = 0\text{ V}$ , $V_{DS} = 650\text{ V}$                               | -    | -    | 0.8     | $\mu\text{A}$ |
|               |                                   | $V_{GS} = 0\text{ V}$ , $V_{DS} = 650\text{ V}$ , $T_C = 125\text{ °C}^{(1)}$ | -    | -    | 50      |               |
| $I_{GSS}$     | Gate-body leakage current         | $V_{DS} = 0\text{ V}$ , $V_{GS} = \pm 20\text{ V}$                            | -    | -    | $\pm 9$ | $\mu\text{A}$ |
| $V_{GS(th)}$  | Gate threshold voltage            | $V_{DS} = V_{GS}$ , $I_D = 50\text{ }\mu\text{A}$                             | 3    | 3.75 | 4.5     | V             |
| $R_{DS(on)}$  | Static drain-source on-resistance | $V_{GS} = 10\text{ V}$ , $I_D = 2.7\text{ A}$                                 | -    | 1.1  | 1.3     | $\Omega$      |

1. Specified by design, not tested in production.

**Table 5. Dynamic**

| Symbol            | Parameter                             | Test conditions   | Min. | Typ. | Max. | Unit     |
|-------------------|---------------------------------------|---|------|------|------|----------|
| $C_{iss}$         | Input capacitance                     | $V_{DS} = 50\text{ V}$ , $f = 1\text{ MHz}$ , $V_{GS} = 0\text{ V}$   | -    | 880  | -    | pF       |
| $C_{oss}$         | Output capacitance                    |   | -    | 65   | -    | pF       |
| $C_{rss}$         | Reverse transfer capacitance          |   | -    | 12   | -    | pF       |
| $C_{o(tr)}^{(1)}$ | Time-related equivalent capacitance   | $V_{DS} = 0\text{ to }520\text{ V}$ , $V_{GS} = 0\text{ V}$   | -    | 43   | -    | pF       |
| $C_{o(er)}^{(2)}$ | Energy-related equivalent capacitance |   | -    | 27   | -    | pF       |
| $R_g$             | Intrinsic gate resistance             | $f = 1\text{ MHz}$ , $I_D = 0\text{ A}$   | -    | 3.5  | -    | $\Omega$ |
| $Q_g$             | Total gate charge                     | $V_{DD} = 500\text{ V}$ , $I_D = 5.4\text{ A}$ , $V_{GS} = 0\text{ to }10\text{ V}$<br>(see the Figure 15. Test circuit for gate charge behavior) | -    | 33   | -    | nC       |
| $Q_{gs}$          | Gate-source charge                    |   | -    | 4    | -    | nC       |
| $Q_{gd}$          | Gate-drain charge                     |   | -    | 21   | -    | nC       |

1.  $C_{o(tr)}$  is a constant capacitance value that gives the same charging time as  $C_{oss}$  while  $V_{DS}$  is rising from 0 V to the stated value.

2.  $C_{o(er)}$  is a constant capacitance value that gives the same stored energy as  $C_{oss}$  while  $V_{DS}$  is rising from 0 V to the stated value.

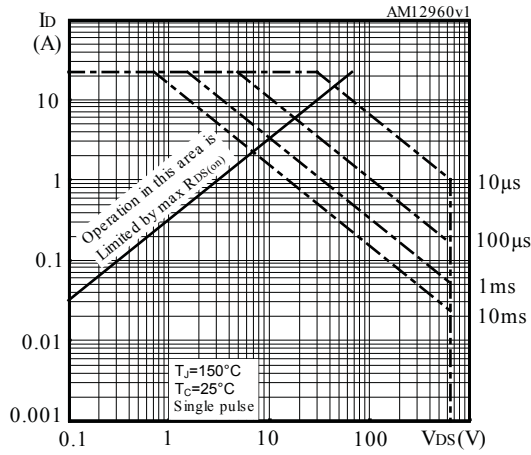
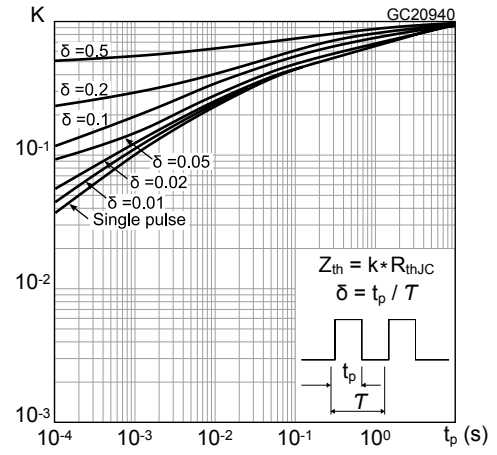
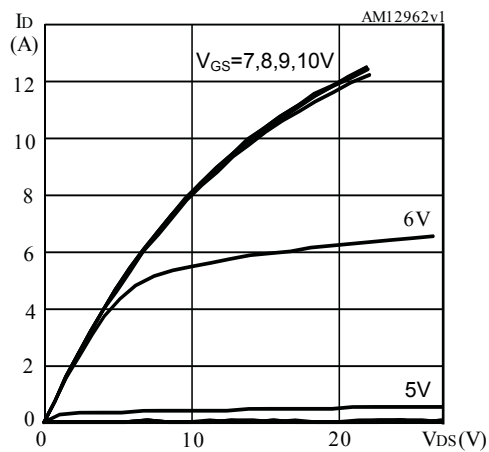
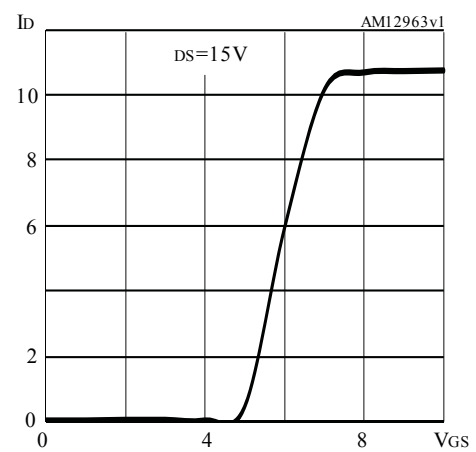
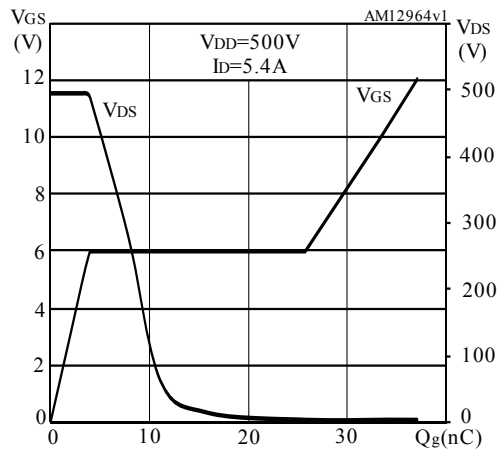
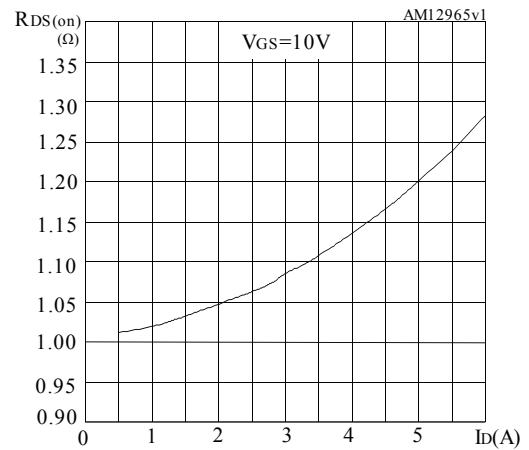
**Table 6. Switching times**

| Symbol       | Parameter           | Test conditions   | Min. | Typ. | Max. | Unit |
|--------------|---------------------|---|------|------|------|------|
| $t_{d(on)}$  | Turn-on delay time  | $V_{DD} = 325\text{ V}$ , $I_D = 2.7\text{ A}$ ,<br>$R_G = 4.7\text{ }\Omega$ , $V_{GS} = 10\text{ V}$      | -    | 14   | -    | ns   |
| $t_r$        | Rise time           |   | -    | 10   | -    | ns   |
| $t_{d(off)}$ | Turn-off delay time | (see the Figure 14. Test circuit for resistive load switching times and Figure 19. Switching time waveform) | -    | 44   | -    | ns   |
| $t_f$        | Fall time           |   | -    | 24   | -    | ns   |

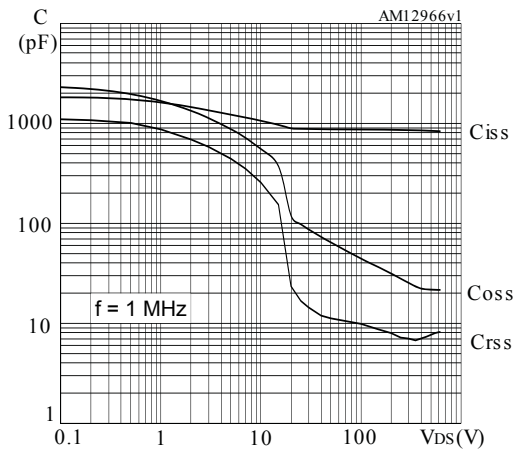
**Table 7. Source-drain diode**

| Symbol          | Parameter                     | Test conditions   | Min. | Typ. | Max. | Unit          |
|-----------------|-------------------------------|---|------|------|------|---------------|
| $I_{SD}$        | Source-drain current          |   | -    | -    | 5.4  | A             |
| $I_{SDM}^{(1)}$ | Source-drain current (pulsed) |   | -    | -    | 21.6 | A             |
| $V_{SD}^{(2)}$  | Forward on voltage            | $V_{GS} = 0\text{ V}$ , $I_{SD} = 5.4\text{ A}$   | -    | -    | 1.5  | V             |
| $t_{rr}$        | Reverse recovery time         | $I_{SD} = 5.4\text{ A}$ , $di/dt = 100\text{ A}/\mu\text{s}$ ,                          | -    | 285  | -    | ns            |
| $Q_{rr}$        | Reverse recovery charge       | $V_{DD} = 60\text{ V}$  | -    | 5.1  | -    | $\mu\text{C}$ |
| $I_{RRM}$       | Reverse recovery current      | (see the Figure 16. Test circuit for inductive load switching and diode recovery times) | -    | 14   | -    | A             |
| $t_{rr}$        | Reverse recovery time         | $I_{SD} = 5.4\text{ A}$ , $di/dt = 100\text{ A}/\mu\text{s}$ ,                          | -    | 330  | -    | ns            |
| $Q_{rr}$        | Reverse recovery charge       | $V_{DD} = 60\text{ V}$ , $T_J = 150\text{ }^\circ\text{C}$                              | -    | 2.5  | -    | $\mu\text{C}$ |
| $I_{RRM}$       | Reverse recovery current      | (see the Figure 16. Test circuit for inductive load switching and diode recovery times) | -    | 15.5 | -    | A             |

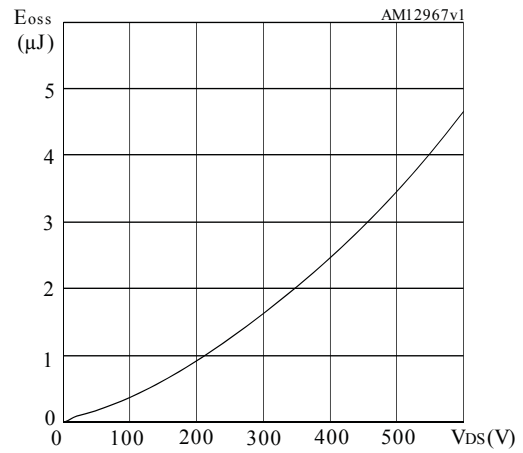
1. Pulse width is limited by safe operating area.
2. Pulse test: pulse duration = 300  $\mu\text{s}$ , duty cycle 1.5%.

**2.1 Electrical characteristics (curves)**
**Figure 1. Safe operating area**

**Figure 2. Normalized transient thermal impedance**

**Figure 3. Typical output characteristics**

**Figure 4. Typical transfer characteristics**

**Figure 5. Typical gate charge characteristics**

**Figure 6. Typical drain-source on-resistance**


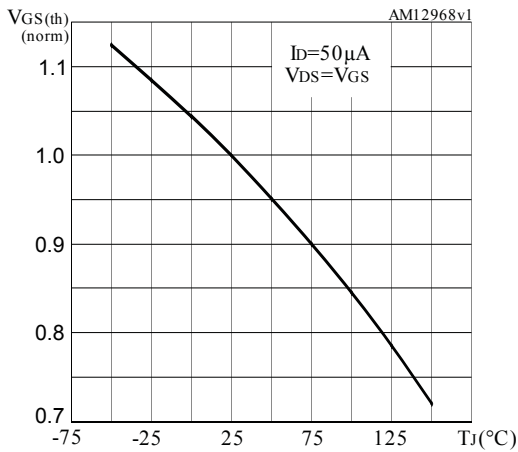
**Figure 7. Typical capacitance characteristics**



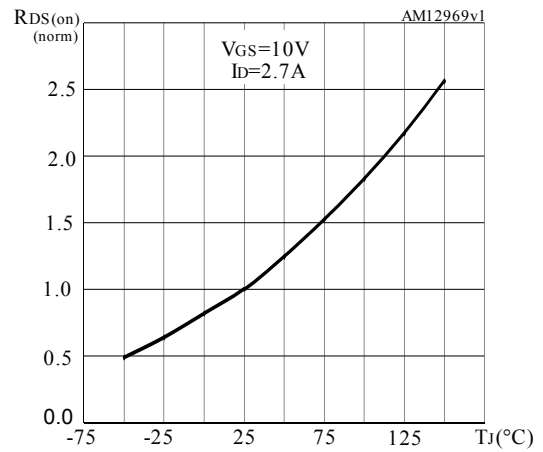
**Figure 8. Typical output capacitance stored energy**



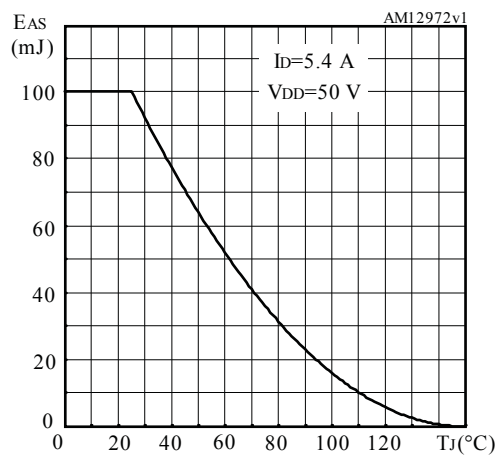
**Figure 9. Normalized gate threshold vs temperature**



**Figure 10. Normalized on-resistance vs temperature**



**Figure 11. Maximum avalanche energy vs temperature**



**Figure 12. Normalized breakdown voltage vs temperature**

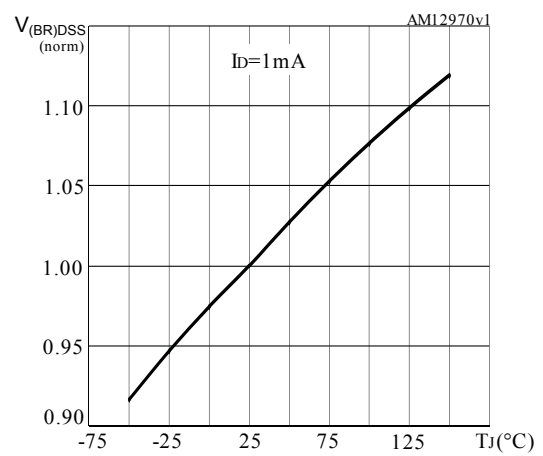
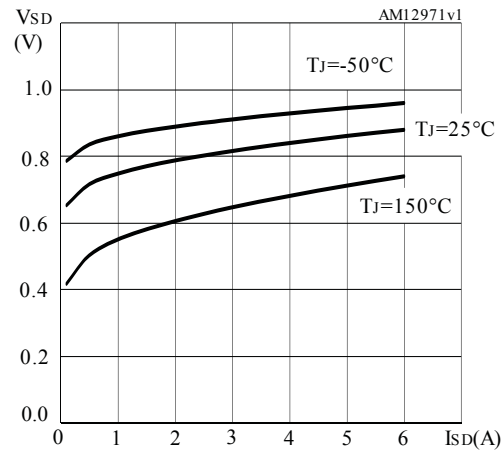
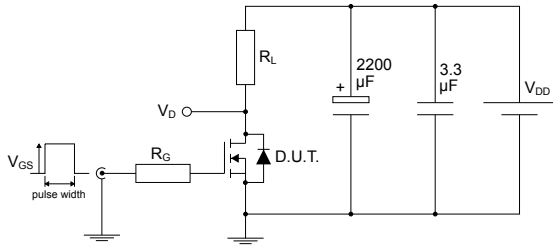


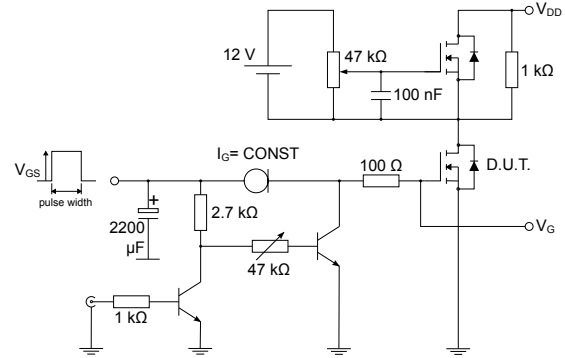
Figure 13. Typical reverse diode forward characteristics



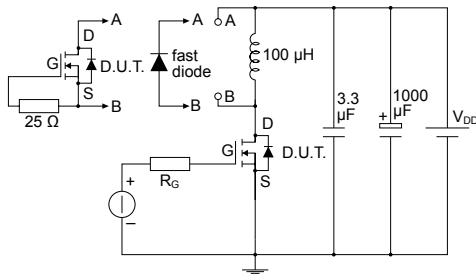
### 3 Test circuits

**Figure 14. Test circuit for resistive load switching times**


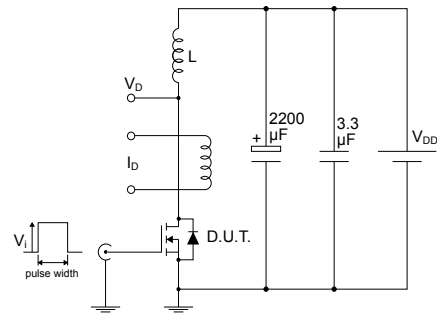
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**Figure 15. Test circuit for gate charge behavior**


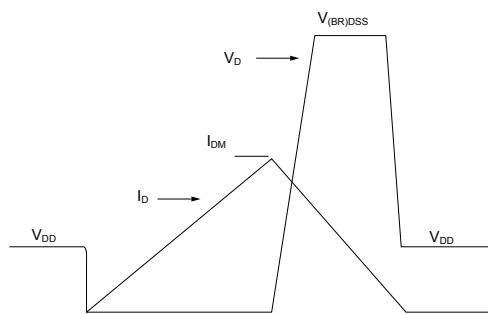
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**Figure 16. Test circuit for inductive load switching and diode recovery times**


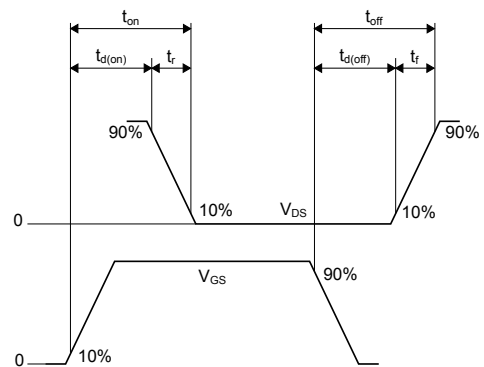
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**Figure 17. Unclamped inductive load test circuit**


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**Figure 18. Unclamped inductive waveform**


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**Figure 19. Switching time waveform**


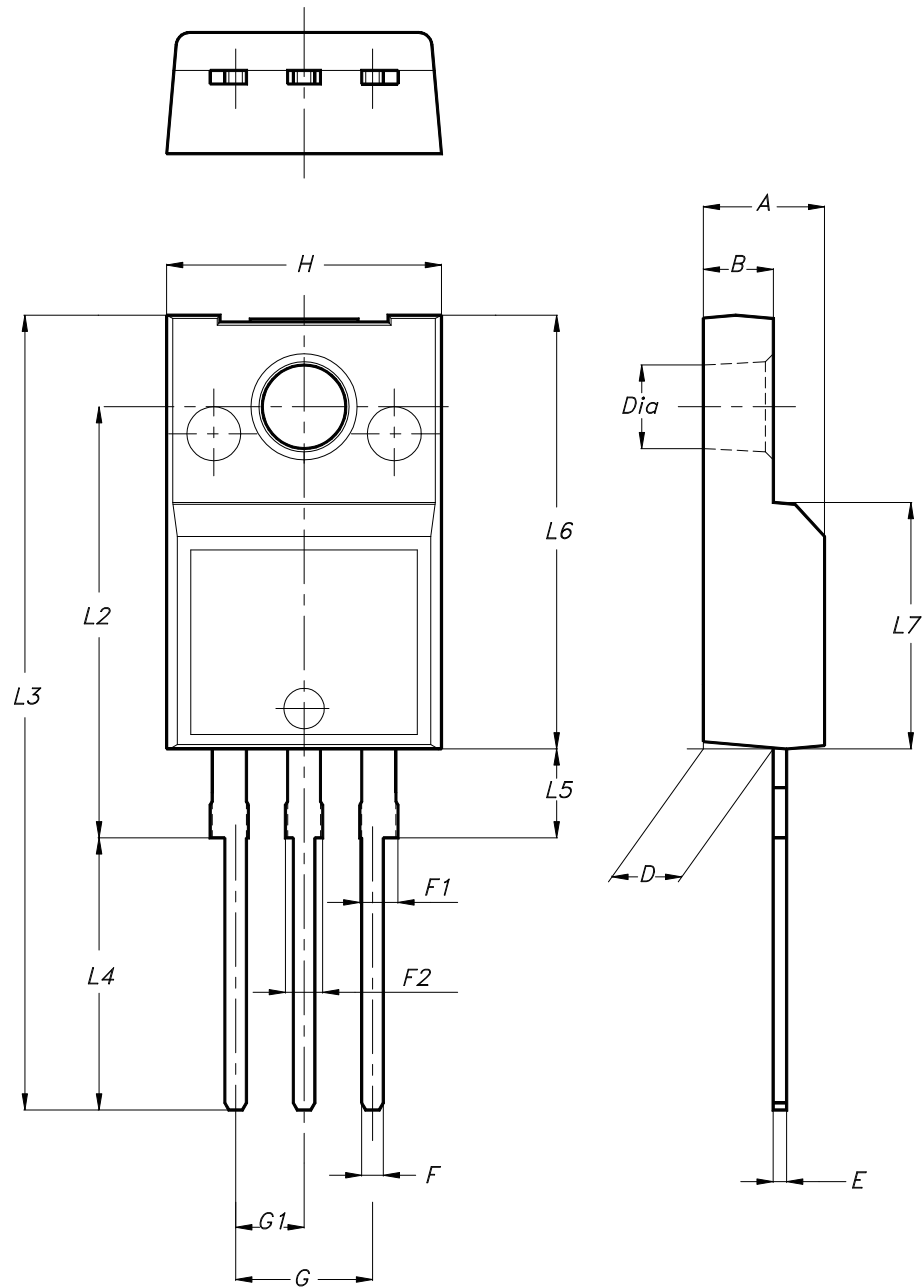
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## 4 Package information

To meet environmental requirements, ST offers these devices in different grades of **ECOPACK** packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions, and product status are available at: [www.st.com](http://www.st.com). ECOPACK is an ST trademark.

### 4.1 TO-220FP type B package information

Figure 20. TO-220FP type B package outline



7012510\_B\_rev.14

**Table 8. TO-220FP type B package mechanical data**

| Dim. | mm    |       |       |
|------|-------|-------|-------|
|      | Min.  | Typ.  | Max.  |
| A    | 4.40  |       | 4.60  |
| B    | 2.50  |       | 2.70  |
| D    | 2.50  |       | 2.75  |
| E    | 0.45  |       | 0.70  |
| F    | 0.75  |       | 1.00  |
| F1   | 1.15  |       | 1.70  |
| F2   | 1.15  |       | 1.70  |
| G    | 4.95  |       | 5.20  |
| G1   | 2.40  |       | 2.70  |
| H    | 10.00 |       | 10.40 |
| L2   |       | 16.00 |       |
| L3   | 28.60 |       | 30.60 |
| L4   | 9.80  |       | 10.60 |
| L5   | 2.90  |       | 3.60  |
| L6   | 15.90 |       | 16.40 |
| L7   | 9.00  |       | 9.30  |
| Dia  | 3.00  |       | 3.20  |

## Revision history

**Table 9. Document revision history**

| Date        | Revision | Changes  |
|-------------|----------|--|
| 05-Apr-2011 | 1        | First release.   |
| 07-Nov-2012 | 2        | Added new part numbers: STF16N65K3 in I <sup>2</sup> PAKFP package and STU6N65K3 in IPAK packages.<br><i>Section 2.1: Electrical characteristics (curves)</i> has been updated.<br>Minor text changes. |
| 27-Mar-2026 | 3        | Removed order code STF16N65K3 and STU6N65K3.<br>Updated <a href="#">Section 4: Package information</a> .<br>Minor text changes.  |

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