

MOSFET – N-Channel, POWERTRENCH®

20 V, 9 A, 18 mohm

FDME820NZT

General Description

This Single N-Channel MOSFET has been designed using onsemi's advanced Power Trench process to optimize the $R_{DS(ON)}$ @ $V_{GS} = 1.8$ V on special MicroFET™ leadframe.

Features

- Max $R_{DS(ON)} = 18$ mΩ at $V_{GS} = 4.5$ V, $I_D = 9$ A
- Max $R_{DS(ON)} = 24$ mΩ at $V_{GS} = 2.5$ V, $I_D = 7.5$ A
- Max $R_{DS(ON)} = 32$ mΩ at $V_{GS} = 1.8$ V, $I_D = 7$ A
- Low Profile – 0.55 mm maximum – in the New Package MicroFET 1.6x1.6 Thin
- HBM ESD Protection Level > 2.5 kV (Note 3)
- Free from Halogenated Compounds and Antimony Oxides
- RoHS Compliant

Applications

- Li-Ion Battery Pack
- Baseband Switch
- Load Switch
- DC-DC Conversion

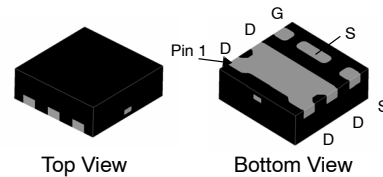
MOSFET MAXIMUM RATINGS ($T_A = 25^\circ\text{C}$, unless otherwise noted)

Symbol	Parameter	Ratings	Unit
V_{DS}	Drain to Source Voltage	20	V
V_{GS}	Gate to Source Voltage	± 12	V
I_D	Drain Current – Continuous $T_A = 25^\circ\text{C}$ (Note 1a) – Pulsed	9 40	A
P_D	Power Dissipation for Single Operation $T_A = 25^\circ\text{C}$ (Note 1a) $T_A = 25^\circ\text{C}$ (Note 1b)	2.1 0.7	W
T_J, T_{STG}	Operating and Storage Junction Temperature Range	-55 to +150	$^\circ\text{C}$

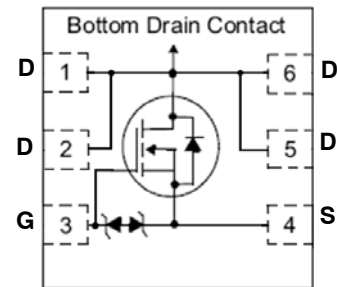
Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

THERMAL CHARACTERISTICS

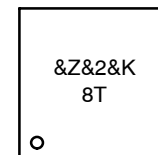
Symbol	Parameter	Ratings	Unit
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient (Note 1a)	70	$^\circ\text{C/W}$
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient (Note 1b)	190	



MicroFET
(UDFN6)
CASE 517DV



MARKING DIAGRAM



&Z = Assembly Plant Code
 &2 = 2-Digit Date Code
 &K = 2-Digits Lot Run Traceability Code
 8T = Specific Device Code

ORDERING INFORMATION

Device	Package	Shipping†
FDME820NZT	UDFN6 (Pb-Free)	5000 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, [BRD8011/D](#).

FDME820NZT

ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise noted)

Symbol	Parameter	Test Condition	Min	Typ	Max	Unit
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OFF CHARACTERISTICS

BV _{DSS}	Drain to Source Breakdown Voltage	I _D = 250 μ A, V _{GS} = 0 V	20	–	–	V
$\frac{\Delta BV_{DSS}}{\Delta T_J}$	Breakdown Voltage Temperature Coefficient	I _D = 250 μ A, Referenced to 25°C	–	20	–	mV/°C
I _{DSS}	Zero Gate Voltage Drain Current	V _{DS} = 16 V, V _{GS} = 0 V	–	–	1	μ A
I _{GSS}	Gate to Source Leakage Current	V _{GS} = $\pm$ 12 V, V _{DS} = 0 V	–	–	$\pm$ 10	μ A

ON CHARACTERISTICS

V _{GS(th)}	Gate to Source Threshold Voltage	V _{GS} = V _{DS} , I _D = 250 μ A	0.5	0.8	1.0	V
$\frac{\Delta V_{GS(th)}}{\Delta T_J}$	Gate to Source Threshold Voltage Temperature Coefficient	I _D = 250 μ A, Referenced to 25°C	–	–3	–	mV/°C
R _{DS(on)}	Drain to Source On-Resistance	V _{GS} = 4.5 V, I _D = 9 A V _{GS} = 2.5 V, I _D = 7.5 A V _{GS} = 1.8 V, I _D = 7 A, V _{GS} = 4.5 V, I _D = 9 A, T _J = 125°C	– – –	14 17 26	18 24 32	m Ω

DYNAMIC CHARACTERISTICS

C _{iss}	Input Capacitance	V _{DS} = 10 V, V _{GS} = 0 V, f = 1 MHz	–	865	–	pF
C _{oss}	Output Capacitance		–	203	–	pF
C _{rss}	Reverse Transfer Capacitance		–	190	–	pF
R _g	Gate Resistance	f = 1 MHz	–	1.0	–	Ω

SWITCHING CHARACTERISTICS

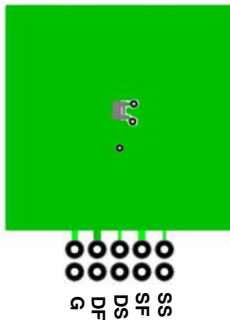
t _{d(on)}	Turn-On Delay Time	V _{DD} = 10 V, I _D = 4 A, V _{GS} = 4.5 V, R _{GEN} = 2 Ω	–	9	–	ns
t _r	Turn-On Rise Time		–	5	–	ns
t _{d(off)}	Turn-Off Delay Time		–	19	–	ns
t _f	Turn-Off Fall Time		–	5	–	ns
Q _g	Total Gate Charge	V _{DD} = 4.2 V, I _D = 3 A, V _{GS} = 4.3 V	–	8.0	–	nC
Q _g	Total Gate Charge	V _{DD} = 4.2 V, I _D = 3 A, V _{GS} = 4.5 V	–	8.5	–	nC
Q _{gs}	Gate to Source Gate Charge	V _{DD} = 10 V, I _D = 9 A	–	1.4	–	nC
Q _{gd}	Gate to Drain "Miller" Charge		–	3.2	–	nC

DRAIN-SOURCE CHARACTERISTICS

V _{SD}	Source to Drain Diode Forward Voltage	V _{GS} = 0 V, I _S = 1.6 A (Note 2) V _{GS} = 0 V, I _S = 9 A (Note 2)	–	0.7 0.8	1.2 1.2	V
t _{rr}	Reverse Recovery Time	I _F = 9 A, di/dt = 100 A/ μ s	–	18	–	ns
Q _{rr}	Reverse Recovery Charge		–	4	–	nC

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

1. R_{θJA} is determined with the device mounted on a 1 in² oz. copper pad on a 1.5 x 1.5 in. board of FR-4 material. R_{θJC} is guaranteed by design while R_{θJA} is determined by the user's board design.



a. 70°C/W when mounted on a 1 in² pad of 2 oz copper.



b. 190°C/W when mounted on a minimum pad of 2 oz copper.

2. Pulse Test: Pulse Width < 300 μ s, Duty Cycle < 2.0%.
3. The diode connected between the gate and source serves only as protection against ESD. No gate overvoltage rating is implied.

TYPICAL CHARACTERISTICS ($T_J = 25^\circ\text{C}$, unless otherwise noted)

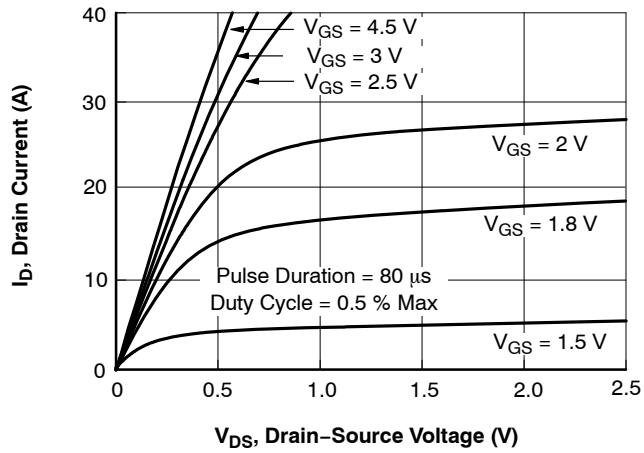


Figure 1. On-Region Characteristics

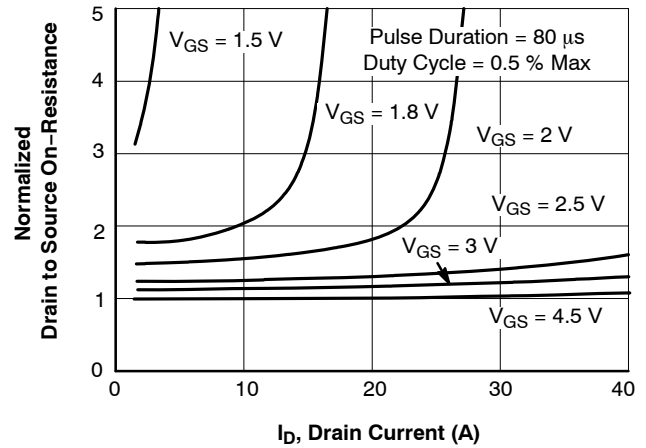


Figure 2. Normalized On-Resistance vs. Drain Current and Gate Voltage

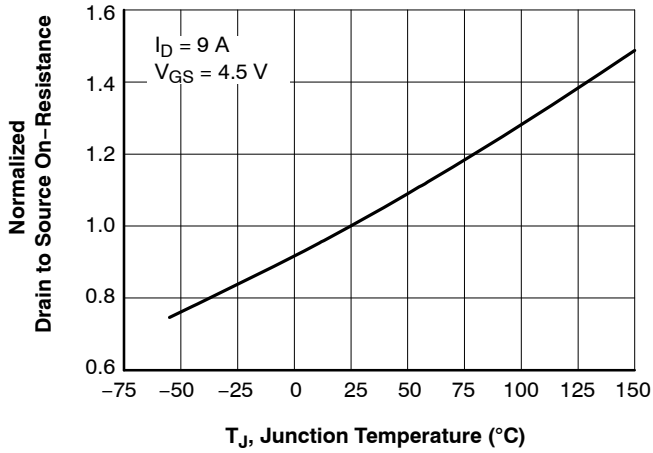


Figure 3. Normalized On-Resistance vs. Junction Temperature

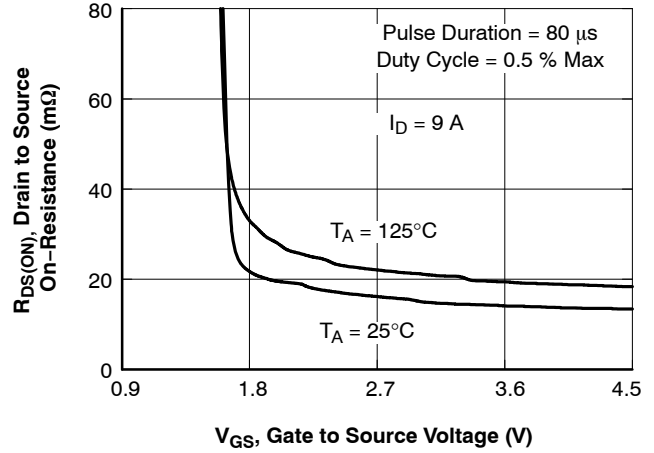


Figure 4. On-Resistance vs. Gate-to-Source Voltage

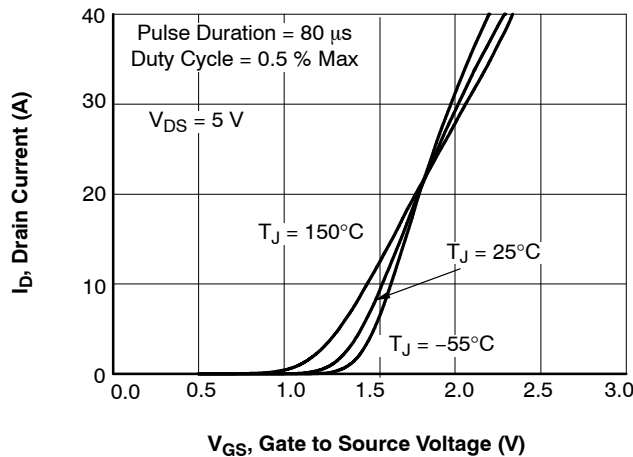


Figure 5. Transfer Characteristics

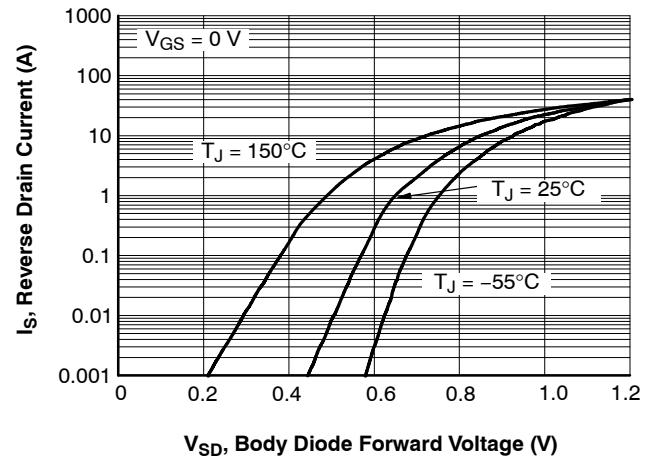


Figure 6. Source to Drain Diode Forward Voltage vs. Source Current

TYPICAL CHARACTERISTICS ($T_J = 25^\circ\text{C}$, UNLESS OTHERWISE NOTED) (CONTINUED)

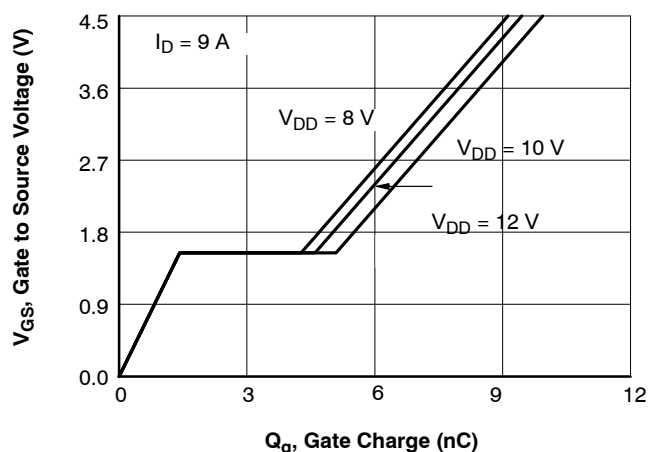


Figure 7. Gate Charge Characteristics

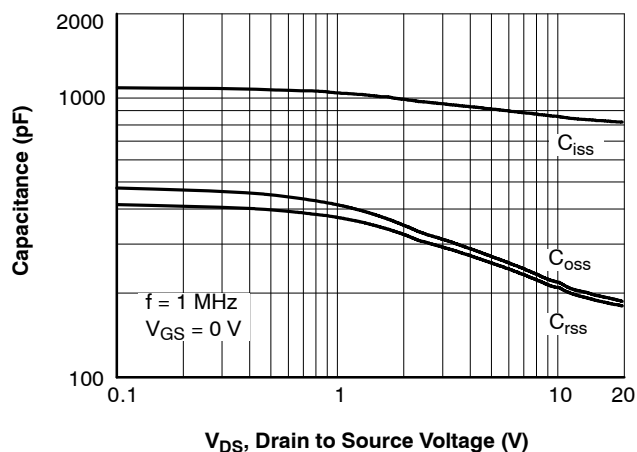


Figure 8. Capacitance vs Drain to Source Voltage

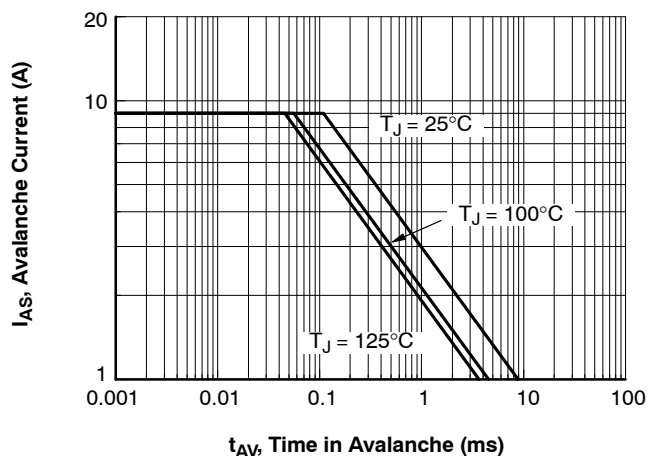


Figure 9. Unclamped Inductive Switching Capability

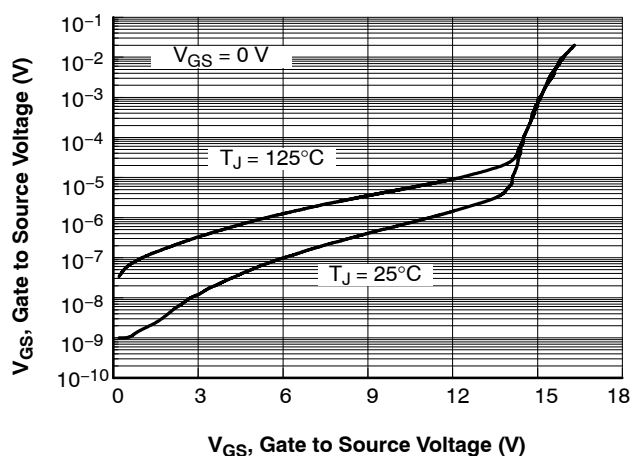


Figure 10. Gate Leakage Current vs Gate to Source Voltage

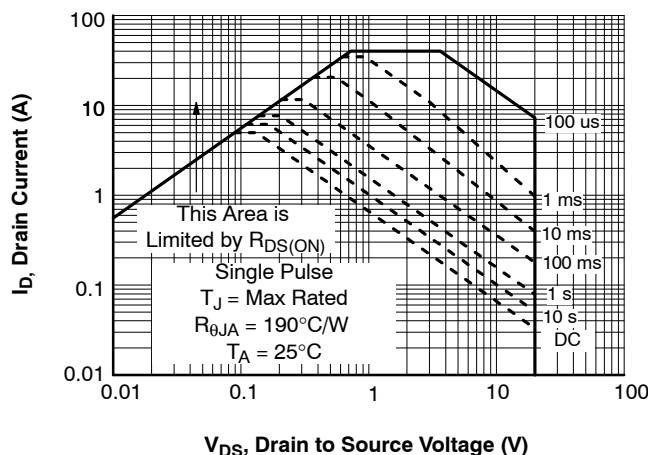


Figure 11. Forward Bias Safe Operating Area

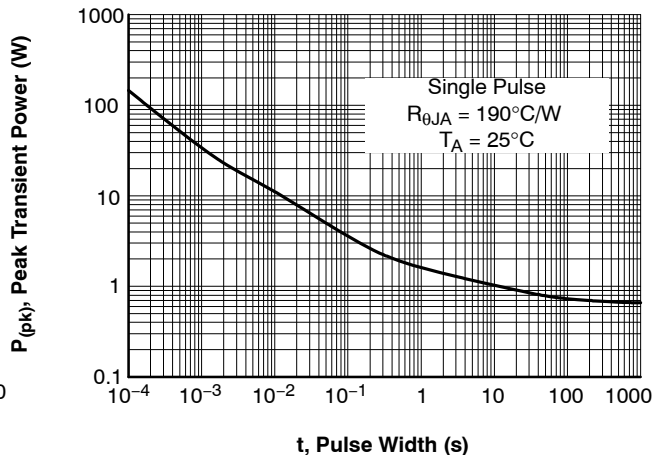


Figure 12. Single Pulse Maximum Power Dissipation

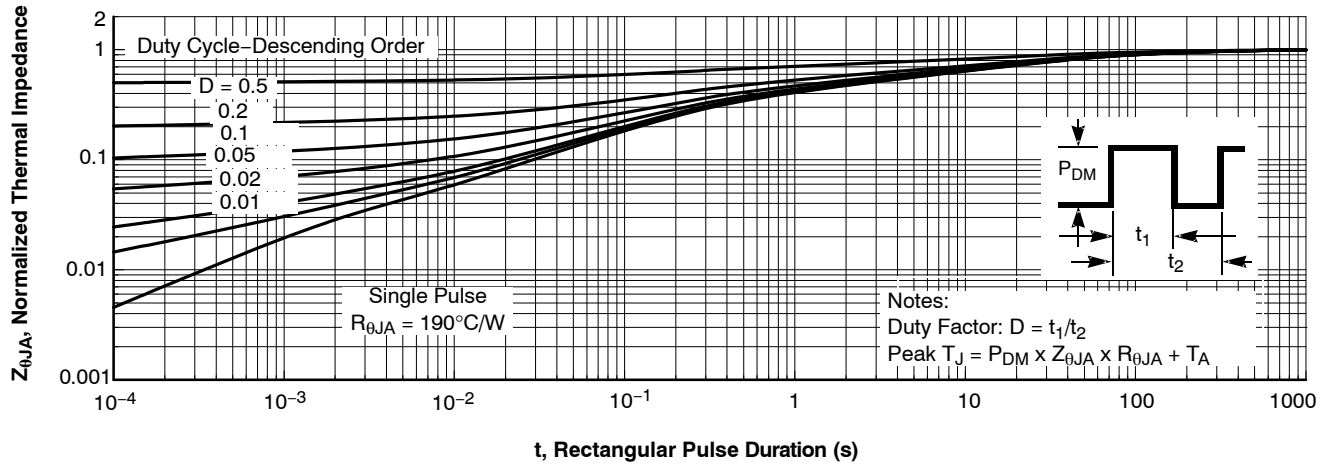
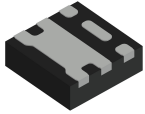
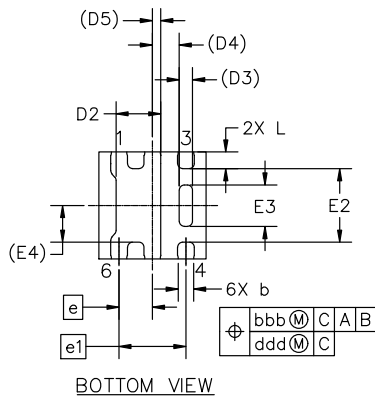
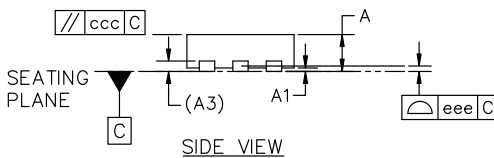
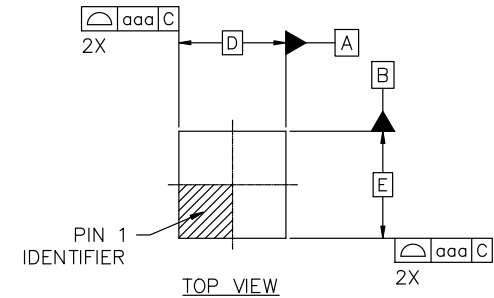


Figure 13. Junction-to-Ambient Transient Thermal Response Curve



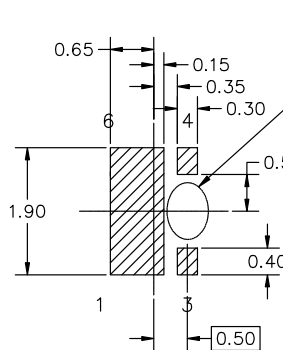
UDFN6 1.60x1.60x0.50, 0.50P
CASE 517DV
ISSUE A

DATE 31 OCT 2024

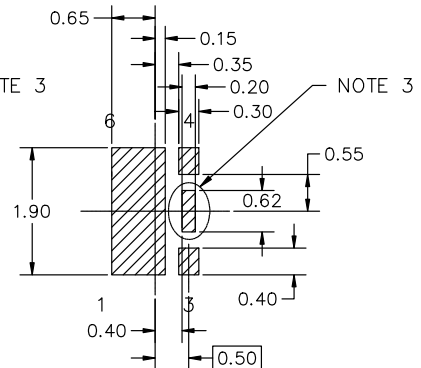


MILLIMETERS			
DIM	MIN	NOM	MAX
A	0.45	0.50	0.55
A1	0.00	0.02	0.05
A3	0.15 REF		
D	1.60 BSC		
D2	0.62	0.67	0.72
D3	0.20 REF		
D4	0.40 REF		
D5	0.125 REF		
E	1.60 BSC		
E2	1.05	1.10	1.15
E3	0.57	0.62	0.67
E4	0.55 REF		
b	0.20	0.25	0.30
e	0.50 BSC		
e1	1.00 BSC		
L	0.20	0.25	0.30

TOLERANCE FORM AND POSITION	
aaa	0.10
bbb	0.10
ccc	0.10
ddd	0.05
eee	0.08



Option 1



Option 2

NOTES:

1. DIMENSIONING AND TOLERANCING AS PER ASMEY14.5M, 2018.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. NO VIAS OR TRACES ALLOWED IN THE AREA

RECOMMENDED MOUNTING FOOTPRINT

*For additional information on our Pb-Free strategy and soldering details, please download the onsemi Soldering and Mounting Techniques Reference manual. SOLDERRM/D.

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