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FDB5800

N-Channel Logic Level PowerTrench® MOSFET

60 V, 80 A, 6 mΩ

Features

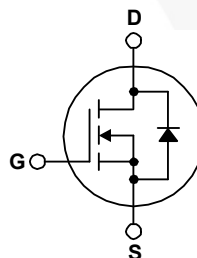
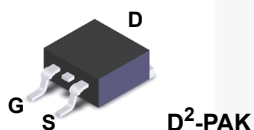
- $R_{DS(on)} = 4.6 \text{ m}\Omega$ (Typ.), $V_{GS} = 10 \text{ V}$, $I_D = 80 \text{ A}$
- High Performance Trench Technology for Externally Low $R_{DS(on)}$
- Low Gate Charge
- High Power and Current Handling Capability
- RoHs Compliant

Description

This N-Channel MOSFET is produced using Fairchild Semiconductor's advanced PowerTrench® process that has been tailored to minimize the on-state resistance while maintaining superior switching performance.

Applications

- Power tools
- Motor drives and Uninterruptible Power Supplies



Absolute Maximum Ratings $T_C = 25^\circ\text{C}$ unless otherwise noted.

Symbol	Parameter	FDB5800	Unit
V_{DSS}	Drain to Source Voltage	60	V
V_{GS}	Gate to Source Voltage	± 20	V
I_D	Drain Current		
	- Continuous ($T_C < 102^\circ\text{C}$, $V_{GS} = 10 \text{ V}$)	80	A
	- Continuous ($T_C < 90^\circ\text{C}$, $V_{GS} = 5 \text{ V}$)	80	A
	- Continuous ($T_{amb} = 25^\circ\text{C}$, $V_{GS} = 10 \text{ V}$, with $R_{\theta JA} = 43^\circ\text{C/W}$)	14	A
	- Pulsed	Figure 4	A
E_{AS}	Single Pulse Avalanche Energy (Note 1)	652	mJ
P_D	- Power Dissipation	242	W
	- Derate above 25°C	1.61	W/ $^\circ\text{C}$
T_J, T_{STG}	- Operating and Storage Temperature	-55 to 175	$^\circ\text{C}$

Thermal Characteristics

$R_{\theta JC}$	Thermal Resistance Junction to Case TO-263, Max.	0.62	$^\circ\text{C/W}$
$R_{\theta JA}$	Thermal Resistance Junction to Ambient TO-263, Max. (Note 2)	62.5	$^\circ\text{C/W}$
$R_{\theta JA}$	Thermal Resistance Junction to Ambient TO-263, 1in ² copper pad area	43	$^\circ\text{C/W}$

Package Marking and Ordering Information

Part Number	Top Mark	Package	Packing Method	Reel Size	Tape Width	Quantity
FDB5800	FDB5800	D ² -PAK	Tape and Reel	330 mm	24 mm	800 units

Electrical Characteristics T_C = 25°C unless otherwise noted.

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
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Off Characteristics

B _{VDSS}	Drain to Source Breakdown Voltage	I _D = 250 μA, V _{GS} = 0 V	60	-	-	V
I _{DSS}	Zero Gate Voltage Drain Current	V _{DS} = 48 V V _{GS} = 0 V	-	-	1	μA
I _{GSS}	Gate to Source Leakage Current	V _{GS} = ±20 V	-	-	±100	nA

On Characteristics

V _{GS(TH)}	Gate to Source Threshold Voltage	V _{GS} = V _{DS} , I _D = 250 μA	1.0	-	2.5	V
r _{DS(ON)}	Drain to Source On Resistance	I _D = 80 A, V _{GS} = 10 V	-	4.6	6.0	mΩ
		I _D = 80 A, V _{GS} = 4.5 V	-	5.8	7.2	
		I _D = 80 A, V _{GS} = 5 V	-	5.5	7.0	
		I _D = 80 A, V _{GS} = 10 V, T _J = 175°C	-	10	12.6	

Dynamic Characteristics

C _{ISS}	Input Capacitance	V _{DS} = 15 V, V _{GS} = 0 V, f = 1 MHz	-	6625	-	pF
C _{OSS}	Output Capacitance		-	628	-	pF
C _{RSS}	Reverse Transfer Capacitance		-	262	-	pF
R _G	Gate Resistance	V _{GS} = 0.5 V, f = 1 MHz	-	1.4	-	Ω
Q _{g(TOT)}	Total Gate Charge at 10V	V _{GS} = 0 V to 10 V	-	104	135	nC
Q _{g(5)}	Total Gate Charge at 5V	V _{GS} = 0 V to 5 V	-	55	72	nC
Q _{g(TH)}	Threshold Gate Charge	V _{GS} = 0 V to 1 V	-	6.0	-	nC
Q _{gs}	Gate to Source Gate Charge	V _{DD} = 30 V I _D = 80 A I _g = 1.0 mA	-	18.4	-	nC
Q _{gs2}	Gate Charge Threshold to Plateau		-	12.5	-	nC
Q _{gd}	Gate to Drain "Miller" Charge		-	20.1	-	nC

Switching Characteristics (V_{GS} = 5V)

t _{ON}	Turn-On Time	V _{DD} = 30 V, I _D = 80 A V _{GS} = 5 V, R _{GS} = 2 Ω	-	-	62.1	ns
t _{d(ON)}	Turn-On Delay Time		-	20.3	-	ns
t _r	Rise Time		-	22.0	-	ns
t _{d(OFF)}	Turn-Off Delay Time		-	27.1	-	ns
t _f	Fall Time		-	12.1	-	ns
t _{OFF}	Turn-Off Time		-	-	59.0	ns

Drain-Source Diode Characteristics

V _{SD}	Source to Drain Diode Voltage	I _{SD} = 80 A	-	-	1.25	V
		I _{SD} = 40 A	-	-	1.0	V
t _r	Reverse Recovery Time	I _{SD} = 60 A, dI _{SD} /dt = 100 A/μs	-	-	44	ns
Q _{SD}	Reverse Recovered Charge	I _{SD} = 60 A, dI _{SD} /dt = 100 A/μs	-	-	57	nC

Notes:

- 1: Starting T_J = 25°C, L = 1mH, I_{AS} = 36A, V_{DD} = 54V, V_{GS} = 10V.
2: Pulse width = 100s.

Typical Characteristics $T_C = 25^\circ\text{C}$ unless otherwise noted

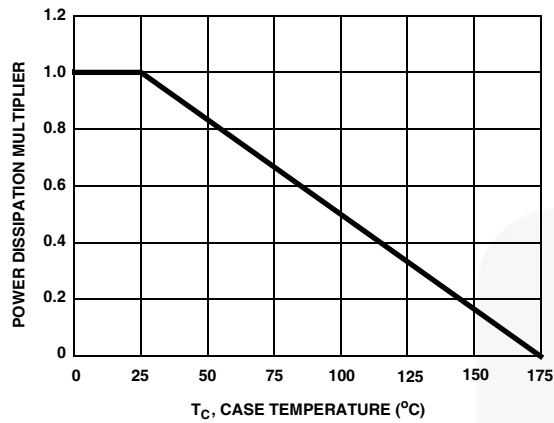


Figure 1. Normalized Power Dissipation vs Case Temperature

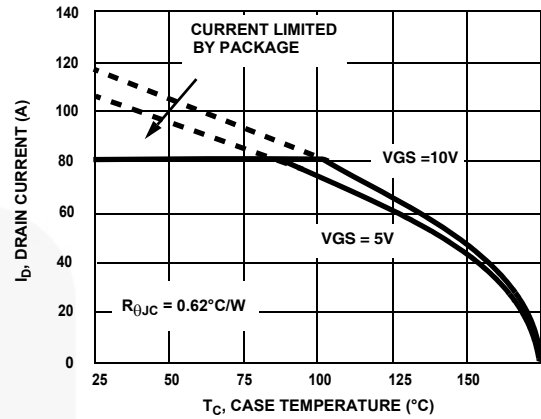


Figure 2. Maximum Continuous Drain Current vs Case Temperature

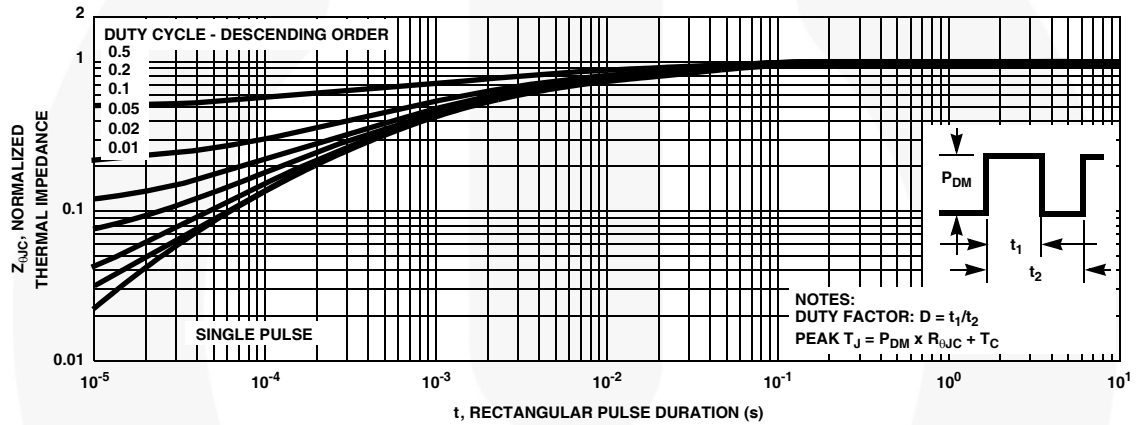


Figure 3. Normalized Maximum Transient Thermal Impedance

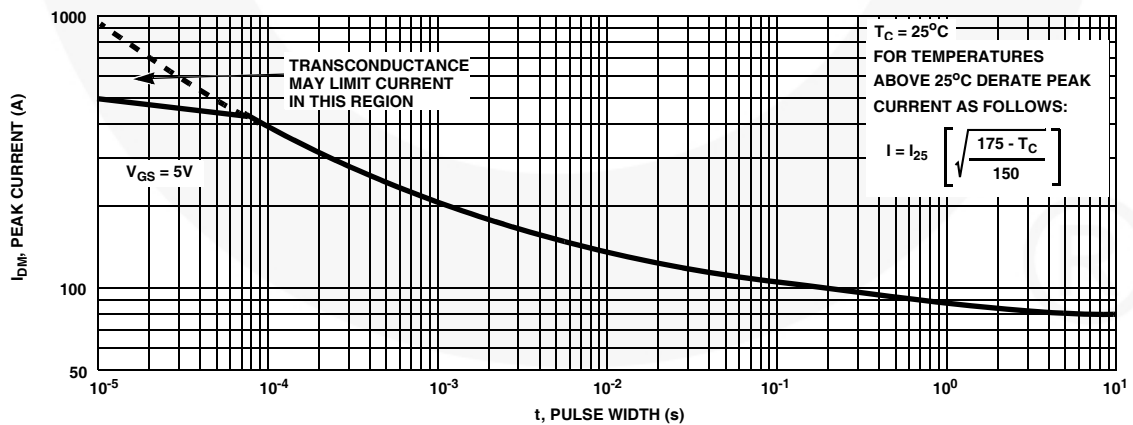


Figure 4. Peak Current Capability

Typical Characteristics $T_C = 25^\circ\text{C}$ unless otherwise noted

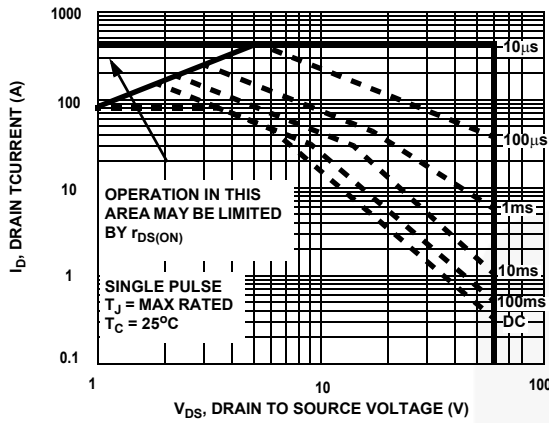
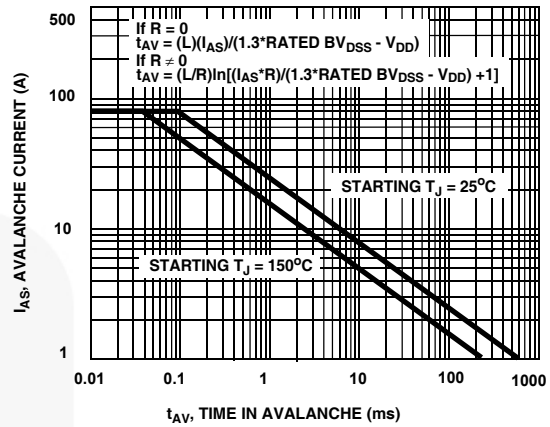


Figure 5. Forward Bias Safe Operating Area



NOTE: Refer to Fairchild Application Notes AN7514 and AN7515

Figure 6. Unclamped Inductive Switching Capability

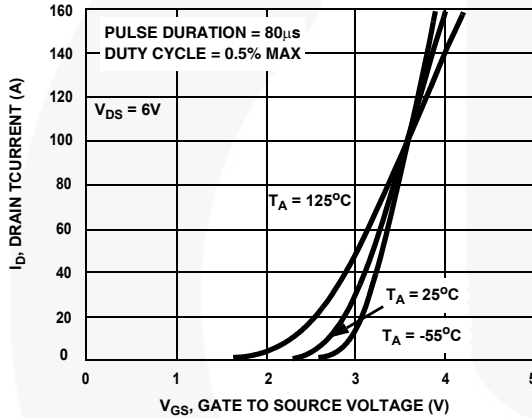


Figure 7. Transfer Characteristics

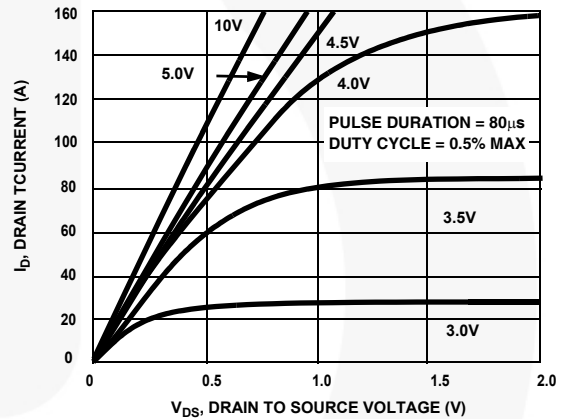


Figure 8. Saturation Characteristics

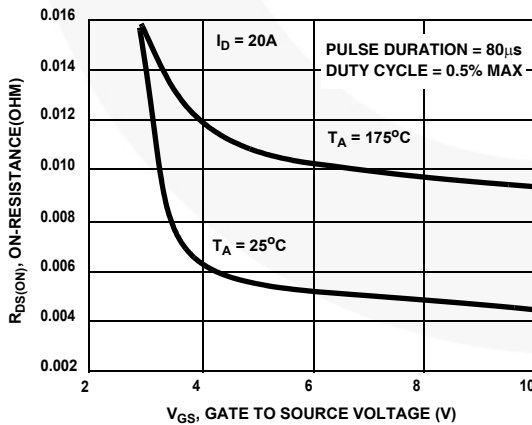


Figure 9. On-Resistance Variation vs. Gate-to-

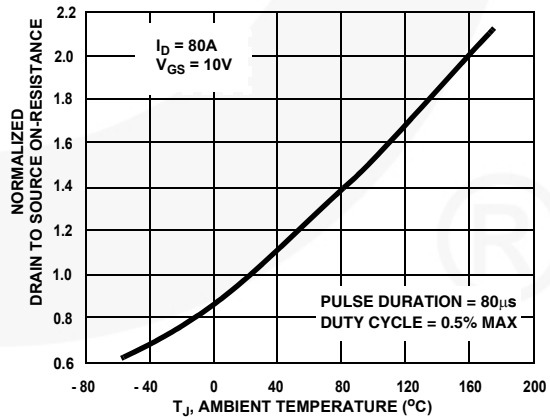


Figure 10. Normalized Drain to Source On

Typical Characteristics $T_C = 25^\circ\text{C}$ unless otherwise noted

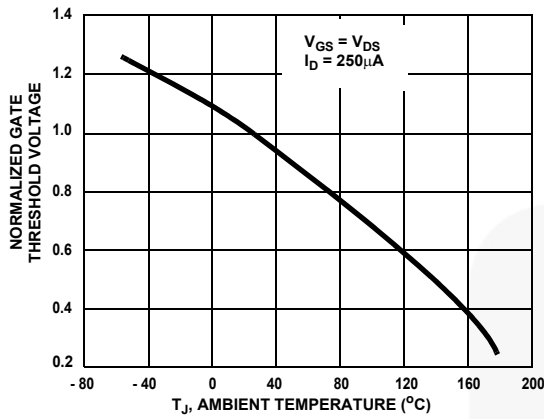


Figure 11. Normalized Gate Threshold Voltage vs Junction Temperature

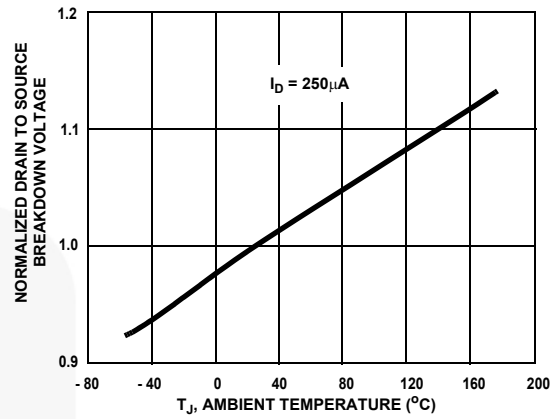


Figure 12. Normalized Drain to Source Breakdown Voltage vs Junction Temperature

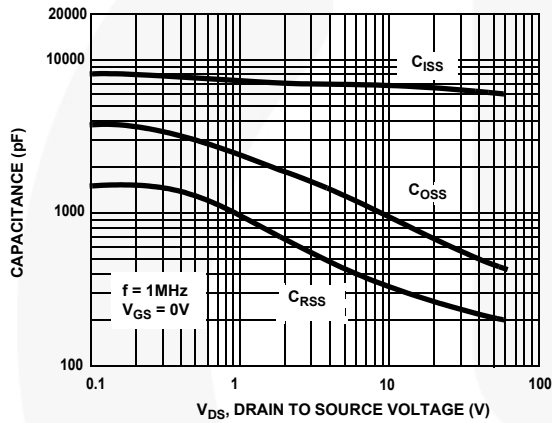


Figure 13. Capacitance vs Drain to Source Voltage

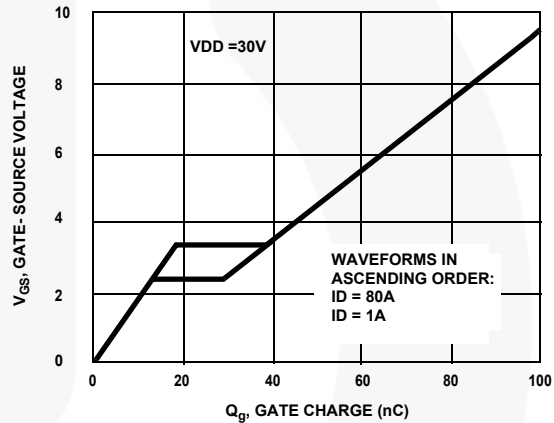
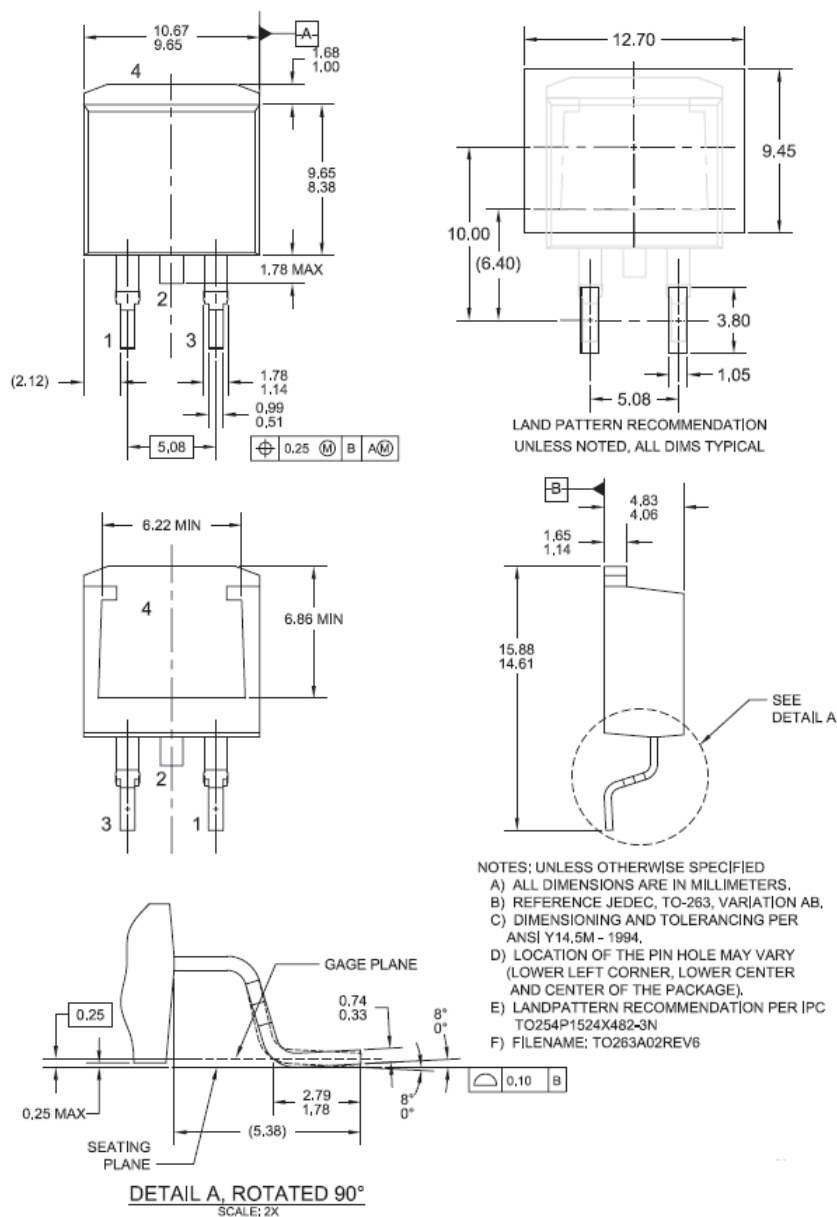


Figure 14. Gate Charge Waveforms for Constant Gate Current

Mechanical Dimensions

Figure 15. TO263 (D²PAK), Molded, 2-Lead, Surface Mount

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No Identification Needed	Full Production	Datasheet contains final specifications. Fairchild Semiconductor reserves the right to make changes at any time without notice to improve the design.
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