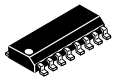
2-Phase Power Factor Controller, Interleaved

NCP1632A



SOIC−16
D SUFFIX
CASE 751B

The NCP1632A integrates a dual MOSFET driver for interleaved PFC applications. Interleaving consists of paralleling two small stages in lieu of a bigger one, more difficult to design. This approach has several merits like the ease of implementation, the use of smaller components or a better distribution of the heating.

Also, Interleaving extends the power range of Critical Conduction Mode that is an efficient and cost−effective technique (no need for low t_{rr} diodes). In addition, the NCP1632A drivers are 180° phase shifted for a significantly reduced current ripple.

Housed in a SOIC16 package, the circuit incorporates all the features necessary for building robust and compact interleaved PFC stages, with a minimum of external components.

General Features

- Near−Unity Power Factor
- Substantial 180° Phase Shift in All Conditions Including Transient Phases
- Frequency Clamped Critical Conduction Mode (**FCCrM**) i.e., Fixed Frequency, Discontinuous Conduction Mode Operation with Critical Conduction Achievable in Most Stressful Conditions
- FCCrM Operation Optimizes the PFC Stage Efficiency Over the Load Range
- Out−of−phase Control for Low EMI and a Reduced rms Current in the Bulk Capacitor
- Frequency Fold−back at Low Power to Further Improve the Light Load Efficiency
- Accurate Zero Current Detection by Auxiliary Winding for Valley Turn On
- Fast Line / Load Transient Compensation
- High Drive Capability: −500 mA / +800 mA
- Signal to Indicate that the PFC is Ready for Operation (“pfcOK” Pin)
- V_{CC} Range: from 10 V to 20 V

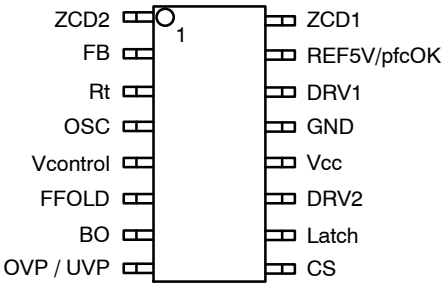
Safety Features

- Output Over and Under Voltage Protection
- Brown−Out Detection with a 50−ms Delay to Help Meet Hold−up Time Specifications
- Soft−Start for Smooth Start−up Operation
- Programmable Adjustment of the Maximum Power
- Over Current Limitation
- Detection of Inrush Currents

MARKING DIAGRAM

NCP1632AG = Device Code
A = Assembly Location
WL = Wafer Lot
Y = Year
WW = Work Week
G = Pb−Free Package

PIN ASSIGNMENT



(Top View)

ORDERING INFORMATION

Device	Package	Shipping†
NCP1632ADR2G	SOIC−16 (Pb−Free)	2500 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

Typical Applications

- Computer Power Supplies
- LCD / Plasma Flat Panels
- All Off Line Appliances Requiring Power Factor Correction

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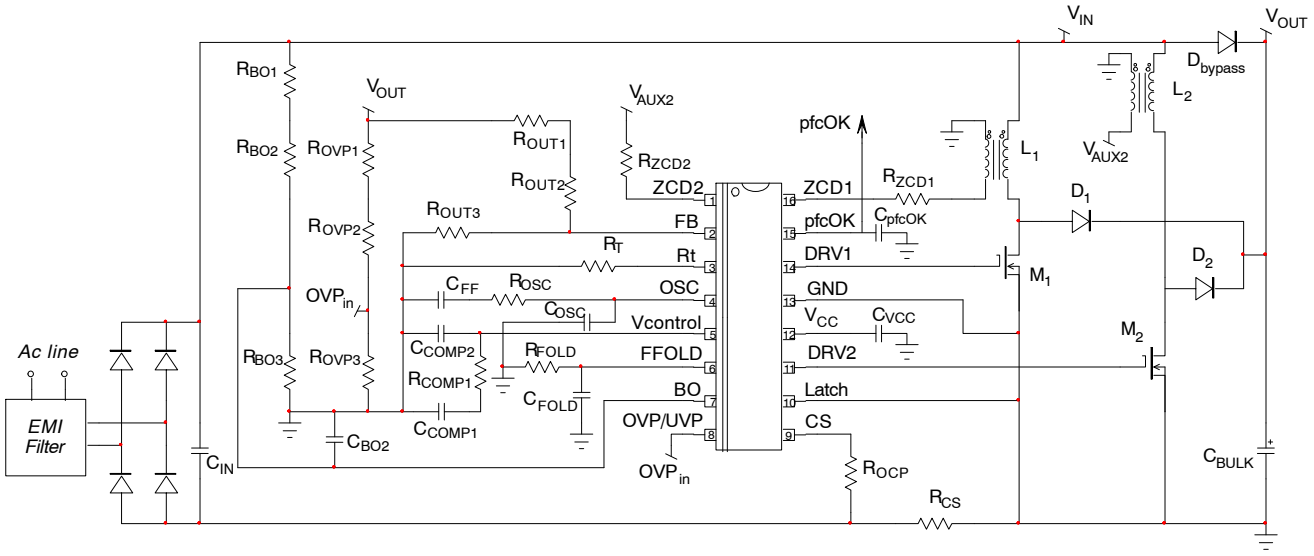


Figure 1. Typical Application Schematic

Table 1. MAXIMUM RATINGS

Symbol	Rating	Pin	Value	Unit
$V_{CC(MAX)}$	Maximum Power Supply Voltage Continuous	12	−0.3, +20	V
V_{MAX}	Maximum Input Voltage on Low Power Pins (Note 1)	1, 2, 3, 4, 6, 7, 8, 9, 10, 15, and 16	−0.3, +9.0	V
$V_{Control(MAX)}$	$V_{Control}$ Pin Maximum Input Voltage	5	−0.3, $V_{Control(clamp)}$ (Note 2)	V
P_D $R_{\theta J-A}$	Power Dissipation and Thermal Characteristics Maximum Power Dissipation @ T_A = 70°C Thermal Resistance Junction−to−Air		 550 145	 mW °C/W
T_J	Operating Junction Temperature Range		−40 to +150	°C
$T_{J(MAX)}$	Maximum Junction Temperature		150	°C
$T_{S(MAX)}$	Storage Temperature Range		−65 to +150	°C
$T_{L(MAX)}$	Lead Temperature (Soldering, 10 s)		300	°C
	ESD Capability, HBM model (Note 3)		3	kV
	ESD Capability, Machine Model (Note 3)		200	V
	ESD Capability, Charged Device Model (Note 3)		1000	V

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. These maximum ratings (−0.3 V / 9.0 V) guarantee that the internal ESD Zener diode is not turned on. More positive and negative voltages can be applied to the ZCD1 pin if the ESD Zener diode current is limited to 5 mA maximum. Typically, as detailed in the Zero Current Detection section, an external resistor is to be placed between the ZCD1 pin and its driving voltage to limit the ZCD1 source and sink currents to 5 mA or less. See Figure 2 and application note AND9654 for more details. The same is valid for the ZCD2 pin.
2. "$V_{Control(clamp)}$" is the pin5 clamp voltage.
3. This device(s) contains ESD protection and exceeds the following tests:
   Human Body Model 2000 V per JEDEC Standard JESD22−A114E
   Machine Model Method 200 V per JEDEC Standard JESD22−A115−A
   Charged Device Model Method 1000 V per JEDEC Standard JESD22−C101E
4. This device contains latch−up protection and exceeds 100 mA per JEDEC Standard JESD78F.

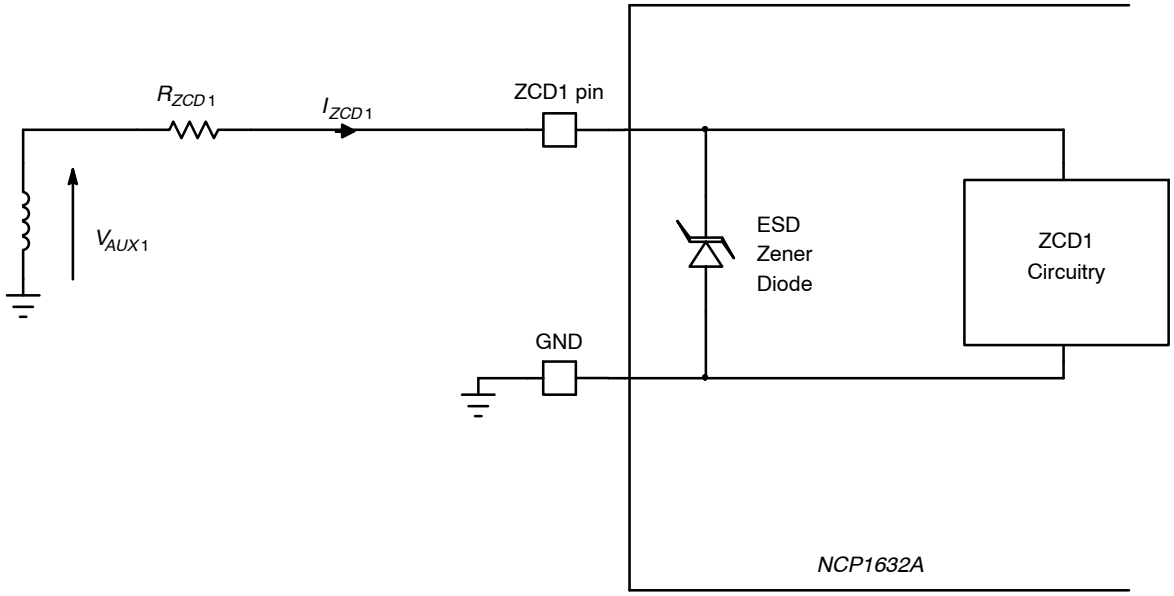


Figure 2. Limit the ZCD1 Pin Current (I_{ZCD1}) between – 5 mA and 5 mA (the Same is Valid for the ZCD2 Pin)

Table 2. TYPICAL ELECTRICAL CHARACTERISTICS TABLE

(Conditions: V_{CC} = 15 V, V_{pin7} = 2 V, V_{pin10} = 0 V, T_J from –40°C, to +125°C, unless otherwise specified)

Characteristics	Test Conditions	Symbol	Min	Typ	Max	Unit
STARTUP AND SUPPLY CIRCUITS						
Supply Voltage						V
Startup Threshold	V_{CC} increasing	$V_{CC(on)}$	11	12	13	
Minimum Operating Voltage	V_{CC} decreasing	$V_{CC(off)}$	9.4	10	10.4	
Hysteresis $V_{CC(on)} - V_{CC(off)}$		$V_{CC(hyst)}$	1.5	2.0	–	
Internal Logic Reset	V_{CC} decreasing	$V_{CC(reset)}$	4.0	6.0	7.5	
Startup Current	V_{CC} = 9.4 V	$I_{CC(start)}$	–	50	100	μA
Supply Current						mA
Device Enabled/No Output Load on Pin6	F_{sw} = 130 kHz (Note 5)	I_{CC1}	–	3.5	7.0	
Current that Discharges V_{CC} in Latch Mode	V_{CC} = 15 V, V_{pin10} = 5 V	$I_{CC(latch)}$	–	0.4	0.8	
Current that Discharges V_{CC} in OFF Mode	V_{CC} = 15 V, pin 7 grounded	$I_{CC(off)}$	–	0.4	0.8	
SKIP Mode Consumption	V_{FB} = 3 V	$I_{CC(SKIP)}$	–	–	2.6	
OSCILLATOR AND FREQUENCY FOLDBACK						
Charge Current	Pin 6 open	I_{CH}	120	140	154	μA
Maximum Discharge Current	Pin 6 open	I_{DISCH}	90	105	115	μA
I_{FFOLD} over I_{CS} Ratio	I_{CS} = 30 μA	$R_{FFOLD30}$	–	1	–	–
Pin 6 Source Current	I_{CS} = 30 μA	$I_{FFOLD30}$	28	30	32	μA
Oscillator Upper Threshold		$V_{OSC(high)}$	–	5	–	V
Oscillator Lower Threshold	V_{FFOLD} = 4.2 V, V_{FFOLD} falling	$V_{OSC(low)}$	3.6	4.0	4.4	V
	V_{FFOLD} = 3.8 V, V_{FFOLD} falling		3.6	4.0	4.4	
	V_{FFOLD} = 3.8 V, V_{FFOLD} rising		2.7	3.0	3.3	
	V_{FFOLD} = 2.0 V, V_{FFOLD} falling		1.8	2.0	2.2	
	V_{FFOLD} = 0.8 V, V_{FFOLD} falling		0.8	1.0	1.1	
Oscillator Swing (Note 6)	V_{FFOLD} = 4.2 V, V_{FFOLD} falling	$V_{OSC(swing)}$	0.90	1.00	1.05	V
	V_{FFOLD} = 3.8 V, V_{FFOLD} falling		0.90	1.00	1.05	
	V_{FFOLD} = 3.8 V, V_{FFOLD} rising		1.90	2.00	2.10	
	V_{FFOLD} = 2.0 V, V_{FFOLD} falling		2.85	3.00	3.15	
	V_{FFOLD} = 0.8 V, V_{FFOLD} falling		3.80	4.00	4.20	

Table 2. TYPICAL ELECTRICAL CHARACTERISTICS TABLE (continued)
(Conditions: V_{CC} = 15 V, V_{pin7} = 2 V, V_{pin10} = 0 V, T_J from −40°C, to +125°C, unless otherwise specified)

Characteristics	Test Conditions	Symbol	Min	Typ	Max	Unit
CURRENT SENSE						
Current Sense Voltage Offset	I_{pin9} = 100 μA I_{pin9} = 10 μA	$V_{CS(TH100)}$ $V_{CS(TH10)}$	−20 −10	0 0	20 10	mV
Current Sense Protection Threshold	T_J = 25°C T_J = −40°C to 125°C	I_{ILIM1} I_{ILIM2}	199 190	210 210	228 228	μA
Threshold for In−rush Current Detection		$I_{in-rush}$	11	14	17	μA
GATE DRIVE (Note 8)						
Drive Resistance DRV1 Sink DRV1 Source DRV2 Sink DRV2 Source	 I_{pin14} = 100 mA I_{pin14} = −100 mA I_{pin11} = 100 mA I_{pin11} = −100 mA	 R_{SNK1} R_{SRC1} R_{SNK2} R_{SRC2}	 − − − −	 7 15 7 15	 15 25 15 25	Ω
Drive Current Capability (Note 6) DRV1 Sink DRV1 Source DRV2 Sink DRV2 Source	 V_{DRV1} = 10 V V_{DRV1} = 0 V V_{DRV2} = 10 V V_{DRV2} = 0 V	 I_{SNK1} I_{SRC1} I_{SNK2} I_{SRC2}	 − − − −	 800 500 800 500	 − − − −	mA
Rise Time DRV1 DRV2	 C_{DRV1} = 1 nF, V_{DRV1} = 1 to 10 V C_{DRV2} = 1 nF, V_{DRV2} = 1 to 10 V	 t_{r1} t_{r2}	 − −	 40 40	 − −	ns
Fall Time DRV1 DRV2	 C_{DRV1} = 1 nF, V_{DRV1} = 10 to 1 V C_{DRV2} = 1 nF, V_{DRV2} = 10 to 1 V	 t_{f1} t_{f2}	 − −	 20 20	 − −	ns
REGULATION BLOCK						
Feedback Voltage Reference		V_{REF}	2.44	2.50	2.56	V
Error Amplifier Source Current Capability	@ V_{pin2} = 2.4 V	$I_{EA(SRC)}$	−	−20	−	μA
Error Amplifier Sink Current Capability	@ V_{pin2} = 2.6 V	$I_{EA(SNK)}$	−	+20	−	
Error Amplifier Gain		G_{EA}	115	200	285	μS
Pin 5 Source Current when ($V_{out(low)}$ Detect) is Activated	pfcOK high pfcOK low	$I_{Control(boost)}$	175 55	220 70	265 85	μA
Pin2 Bias Current	V_{pin2} = 2.5 V	$I_{FB(bias)}$	−500		500	nA
Pin 5 Voltage	@ V_{pin2} = 2.4 V @ V_{pin2} = 2.6 V	$V_{Control(clamp)}$ $V_{Control(MIN)}$ $V_{Control(range)}$	− − 2.8	3.6 0.6 3.0	− − 3.5	V
Ratio ($V_{out(low)}$ Detect Threshold / V_{REF}) (Note 6)	FB falling	$V_{out(low)}/V_{REF}$	95.0	95.5	96.0	%
Ratio ($V_{out(low)}$ Detect Hysteresis / V_{REF}) (Note 6)	FB rising	$H_{out(low)}/V_{REF}$	−	−	0.5	%
SKIP MODE						
Duty Cycle	V_{FB} = 3 V	D_{MIN}	−	−	0	%
RAMP CONTROL (VALID FOR THE TWO PHASES)						
Maximum DRV1 and DRV2 On−Time (FB Pin Grounded)	V_{pin7} = 1.1 V, I_{pin3} = 50 μA (Note 6) V_{pin7} = 1.1 V, I_{pin3} = 200 μA V_{pin7} = 2.2 V, I_{pin3} = 100 μA V_{pin7} = 2.2 V, I_{pin3} = 400 μA	t_{on1} t_{on2} t_{on3} t_{on4}	14.5 1.00 3.80 0.34	19.5 1.35 5.00 0.41	22.5 1.60 6.00 0.50	μs
Pin 3 Voltage	V_{BO} = V_{pin7} = 1.1 V, I_{pin3} = 50 μA V_{BO} = V_{pin7} = 1.1 V, I_{pin3} = 200 μA V_{BO} = V_{pin7} = 2.2 V, I_{pin3} = 50 μA V_{BO} = V_{pin7} = 2.2 V, I_{pin3} = 200 μA	V_{Rt1} V_{Rt2} V_{Rt3} V_{Rt4}	1.068 1.068 2.165 2.165	1.096 1.096 2.196 2.196	1.126 1.126 2.228 2.228	V
Maximum V_{ton} Voltage	Not tested	$V_{ton(MAX)}$		5		V
Pin 3 Current Capability		$I_{Rt(MAX)}$	1	−	−	mA

Table 2. TYPICAL ELECTRICAL CHARACTERISTICS TABLE (continued)
(Conditions: V_{CC} = 15 V, V_{pin7} = 2 V, V_{pin10} = 0 V, T_J from −40°C, to +125°C, unless otherwise specified)

Characteristics	Test Conditions	Symbol	Min	Typ	Max	Unit
RAMP CONTROL (VALID FOR THE TWO PHASES)						
Pin 3 Sourced Current Below which the Controller is OFF		$I_{Rt(off)}$	–	7	–	μA
Pin 3 Current Range	(Note 6)	$I_{Rt(range)}$	20		1000	μA
ZERO VOLTAGE DETECTION CIRCUIT (VALID FOR ZCD1 AND ZCD2)						
ZCD Threshold Voltage	V_{ZCD} increasing V_{ZCD} falling	$V_{ZCD(TH),H}$ $V_{ZCD(TH),L}$	0.40 0.20	0.50 0.25	0.60 0.30	V
ZCD Hysteresis	V_{ZCD} decreasing	$V_{ZCD(HYS)}$	–	0.25	–	V
Input Clamp Voltage High State Low State	 I_{pin1} = 5.0 mA I_{pin1} = −5.0 mA	 $V_{ZCD(high)}$ $V_{ZCD(low)}$	 9.0 −1.10	 11 −0.65	 13 −0.10	V
Internal Input Capacitance (Note 6)		C_{ZCD}	–	10	–	pF
ZCD Watchdog Delay		t_{ZCD}	80	200	320	μs
BROWN−OUT DETECTION						
Brown−Out Comparator Threshold		$V_{BO(TH)}$	0.97	1.00	1.03	V
Brown−Out Current Source		I_{BO}	6	7	8	μA
Brown−Out Blanking Time (Note 6)		$t_{BO(BLANK)}$	38	50	62	ms
Brown−Out Monitoring Window (Note 6)		$t_{BO(window)}$	38	50	62	ms
Pin 7 Clamped Voltage if $V_{BO} < V_{BO(TH)}$ During $t_{BO(BLANK)}$	I_{pin7} = −100 μA	$V_{BO(clamp)}$	–	965	–	mV
Current Capability of the BO Clamp		$I_{BO(clamp)}$	100	–	–	μA
Hysteresis $V_{BO(TH)} - V_{BO(clamp)}$	I_{pin7} = − 100 μA	$V_{BO(HYS)}$	10	35	60	mV
Current Capability of the BO pin Clamp PNP Transistor		$I_{BO(PNP)}$	100	–	–	μA
Pin BO Voltage when Clamped by the PNP	I_{pin7} = − 100 μA	$V_{BO(PNP)}$	0.35	0.70	0.90	V
OVER AND UNDER VOLTAGE PROTECTIONS						
Over−Voltage Protection Threshold		V_{OVP}	2.425	2.500	2.575	V
Ratio (V_{OVP} / V_{REF}) (Note 6)		V_{OVP}/V_{REF}	99.2	99.7	100.2	%
Ratio UVP Threshold over V_{REF}		V_{UVP}/V_{REF}	8	12	16	%
Pin 8 Bias Current	V_{pin8} = 2.5 V, V_{pin8} = 0.3 V	$I_{OVP(bias)}$	−500	–	500	nA
LATCH INPUT						
Pin Latch Threshold for Shutdown		V_{Latch}	2.3	2.5	2.7	V
Pin Latch Bias Current	V_{pin10} = 2.5 V	$I_{Latch(bias)}$	−500	–	500	nA
pfcOK / REF5V						
Pin 15 Voltage Low State	V_{pin7} = 0 V, I_{pin15} = 250 μA	$V_{REF5V(low)}$	–	60	120	mV
Pin 15 Voltage High State	V_{pin7} = 0 V, I_{pin15} = 5 mA	$V_{REF5V(high)}$	4.7	5.0	5.3	V
Current Capability		I_{REF5V}	5	10	–	mA
THERMAL SHUTDOWN						
Thermal Shutdown Threshold	(Note 6)	T_{SHDN}	130	140	150	°C
Thermal Shutdown Hysteresis		$T_{SHDN(HYS)}$	–	50	–	°C

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

5. DRV1 and DRV2 pulsating at half this frequency, that is, 65 kHz.
6. Not tested. Guaranteed by design.
7. Not tested. Guaranteed by design and characterization.
8. Guaranteed by design, the VCC pin can handle the double of the DRV peak source current, that is, 1 A typically.

Table 3. DETAILED PIN DESCRIPTION

Pin number	Name	Function
1	ZCD2	This is the zero current detection pin for phase 2 of the interleaved PFC stage. It is designed to monitor the voltage of an auxiliary winding to detect the inductor core reset and the valley of the MOSFET drain source voltage
2	FB	This pin receives the portion of the PFC stage output voltage for regulation. V_{FB} is also monitored by the dynamic response enhancer (DRE) which drastically speeds−up the loop response when the output voltage drops below 95.5 % of the wished level.
3	R_T	The resistor placed between pin 3 and ground adjusts the maximum on−time in both phases, and hence the maximum power that can be delivered by the PFC stage.
4	OSC	Oscillator pin. The oscillator sets the maximum switching frequency, particularly in medium− and light−load conditions when frequency foldback is engaged.
5	$V_{CONTROL}$	The error amplifier output is available on this pin for loop compensation. The capacitors and resistor connected between this pin and ground adjusts the regulation loop bandwidth that is typically set below 20 Hz to achieve high Power Factor ratios. Pin5 is grounded when the circuit is off so that when it starts operation, the power increases gradually (soft−start).
6	FFOLD (Freq. Foldback)	This pin sources a current proportional to the input current. Placing a resistor and a capacitor between the FFOLD pin and GND, we obtain the voltage representative of the line current magnitude necessary to control the frequency foldback characteristics.
7	BO (Brown−out Protection)	Apply an averaged portion of the input voltage to detect brown−out conditions when V_{BO} drops below 1 V. A 50−ms internal delay blanks short mains interruptions to help meet hold−up time requirements. When it detects a brown−out condition, the circuit stops pulsing and grounds the “pfcOK” pin to disable the downstream converter. Also an internal 7−μA current source is activated to offer a programmable hysteresis. The pin2 voltage is internally re−used for feed−forward. Ground pin 2 to disable the part.
8	OVP / UVP	The circuit turns off when $V_{pin\,8}$ goes below V_{UVP} (300 mV typically − UVP protection) and disables the drive when the pin voltage exceeds V_{OVP} (2.5 V typically − OVP protection).
9	CS (Current Sense)	The CS pin monitors a negative voltage proportional to the input current to limit the maximum current flowing in the phases. The NCP1632A also uses the CS information to prevent the PFC stage from starting operation in presence of large in−rush currents.
10	Latch	Apply a voltage higher than V_{STDWN} (2.5 V typically) to latch−off the circuit. The device is reset by unplugging the PFC stage (practically when the circuit detects a brown−out detection) or by forcing the circuit V_{CC} below V_{CC}RST (4 V typically). Operation can then resume when the line is applied back.
11	DRV2	This is the gate drive pin for phase 2 of the interleaved PFC stage. The high−current capability of the totem pole gate drive (+0.5/−0.8A) makes it suitable to effectively drive high gate charge power MOSFETs.
12	V_{CC}	This pin is the positive supply of the IC. The circuit starts to operate when V_{CC} exceeds 12 V and turns off when V_{CC} goes below 10 V (typical values). After start−up, the operating range is 10.5 V up to 20 V.
13	GND	Connect this pin to the pre−converter ground.
14	DRV1	This is the gate drive pin for phase 1 of the interleaved PFC stage. The high−current capability of the totem pole gate drive (+0.5/−0.8A) makes it suitable to effectively drive high gate charge power MOSFETs.
15	REF5V / pfcOK	The pin15 voltage is high (5 V typically) when the PFC stage is in a normal, steady state situation and low otherwise. This signal serves to “inform” the downstream converter that the PFC stage is ready and that hence, it can start operation.
16	ZCD1	This is the zero current detection pin for phase 1 of the interleaved PFC stage. It is designed to monitor the voltage of an auxiliary winding to detect the inductor core reset and the valley of the MOSFET drain source voltage.

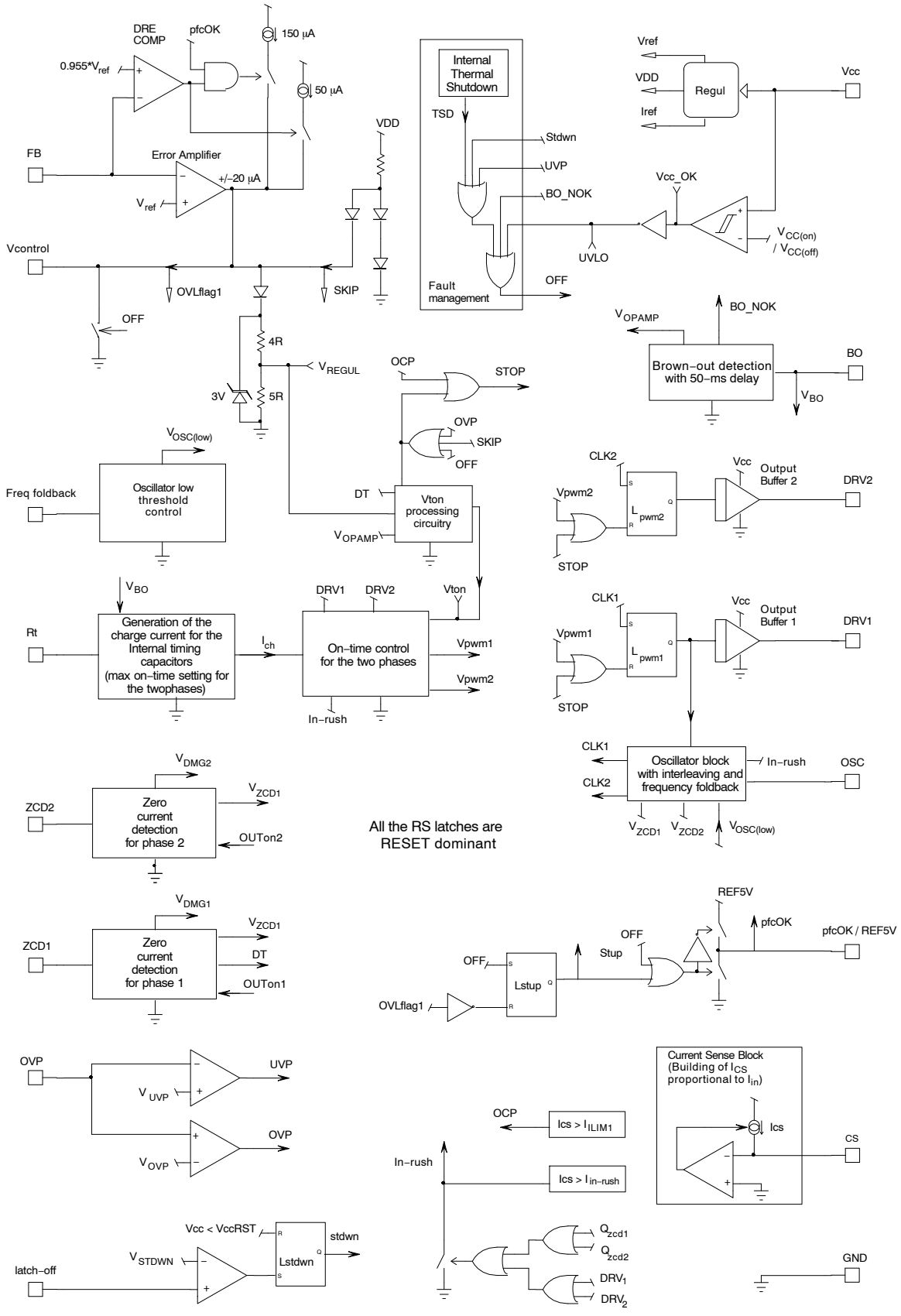


Figure 3. Block Diagram

DETAILED OPERATING DESCRIPTION

Introduction

The NCP1632A is an interleaving, 2−phase PFC controller. It is designed to operate in critical conduction mode (CrM) in heavy load conditions and in discontinuous conduction mode (DCM) with frequency foldback in light load for an optimized efficiency over the whole power range. In addition, the circuit incorporates protection features for a rugged operation. More generally, the NCP1632A functions make it the ideal candidate in systems where cost−effectiveness, reliability, low stand−by power, high−level efficiency over the load range and near−unity power factor are the key parameters:

- **Accurate and robust interleaving management**:
  The NCP1632A modulates the oscillator swing as a function of the current cycle duration to control the delay between the two branches drive pulses. This ON proprietary method is a simple but robust and stable solution to interleave the two branches. The 180−degree phase shift is ensured in all situations (including transient phases) and whatever the operation mode is (CrM or DCM).
- **Frequency fold−back and skip−cycle capability for low power stand−by**:
  The NCP1632A optimizes the efficiency of your PFC stage over the whole load range. In medium− and light−load conditions, the switching frequency can linearly decay as a function of the line current magnitude (FFOLD mode) down to about 30 kHz at very low power (depending on the OSC pin capacitor). To prevent any risk of regulation loss at no load and to further minimize the consumed power, the circuit skips cycles when the error amplifier output reaches its low clamp level.
- **Fast Line / Load Transient Compensation**:
  by essence, PFC stages are slow systems. Thus, the output voltage of PFC stages may exhibit excessive over− and under−shoots because of abrupt load or input voltage variations (e.g. at start−up). The NCP1632A incorporates a fast line / load compensation to avoid such large output voltage variations. Practically, the circuit monitors the output voltage and:
  - Disables the drive to stop delivering power as long as the output voltage exceeds the over voltage protection (OVP) level.
  - Drastically speeds−up the regulation loop (Dynamic Response Enhancer) when the output voltage is below 95.5 % of its regulation level. This function is partly disabled during the startup phase to ensure a gradual increase of the power delivery (soft−start).
- **PFC OK**: the circuit detects when the circuit is in normal situation or if on the contrary, it is in a start−up or fault condition. In the first case, the pfcOK pin is in high state and low otherwise. The pfcOK pin serves to control the downstream converter operation in response to the PFC state.
- **Output Stage Totem Pole**: the NCP1632A incorporates a −0.5 A / +0.8 A gate driver to efficiently drive most TO220 or TO247 power MOSFETs.
- **Safety Protections**: the NCP1632A permanently monitors the input and output voltages, the inductor current and the die temperature to protect the system from possible over−stresses and make the PFC stage extremely robust and reliable. In addition to the aforementioned OVP protection, one can list:
  - *Maximum Current Limit*: the circuit permanently senses the input current for over current protection and in−rush currents detection, for preventing the excessive stress suffered by the MOSFETs if they turned on when large in−rush currents take place.
  - *Zero Current Detection*: the NCP1632A prevents the MOSFET from closing until the inductor current is zero, to ensure discontinuous conduction mode operation in each branch.
  - *Under−Voltage Protection*: the circuit turns off when it detects that the output voltage goes below 12% of the OVP level (typically). This feature protects the PFC stage from starting operation in case of too low ac line conditions or in case of a failure in the OVP monitoring network (e.g., bad connection).
  - *Brown−Out Detection*: the circuit detects too low ac line conditions and stop operating in this case. This protection protects the PFC stage from the excessive stress that could damage it in such conditions.
  - *Thermal Shutdown*: an internal thermal circuitry disables the circuit gate drive and then keeps the power switch off when the junction temperature exceeds 150°C typically. The circuit resumes operation once the temperature drops below about 100°C (50°C hysteresis).

Interleaving

An interleaved PFC converter consists of two paralleled PFC stages operated out−of−phase. Each individual stage is generally termed phase, channel or branch.

If the input current is well balanced, each phase processes half the total power. The size and cost of each individual branch is hence accordingly minimized and losses are spitted between the two channels. Hence, hot spots are less likely to be encountered. Also, if the interleaving solution requires more components, they are smaller and often more standard. In addition, they can more easily fit applications with specific form−factors as required in thin flat panel TVs for instance.

Furthermore, if the two channels are properly operated out−of−phase, a large part of the switching−frequency ripple currents generated by each individual branch cancel when they add within the EMI filter and the bulk capacitors. As a result, EMI filtering is significantly eased and the bulk capacitor rms current is drastically reduced. Interleaving

therefore extends the CrM power range by sharing the task between the two phases and by allowing for a reduced input current ripple and a minimized bulk capacitor rms current.

This is why this approach which at first glance, may appear more costly than the traditional 1−phase solution can actually be extremely cost−effective and efficient for powers above 300 watts. And even less for applications like LCD and Plasma TV applications where the need for smaller components, although more numerous, helps meet the required low−profile form−factors.

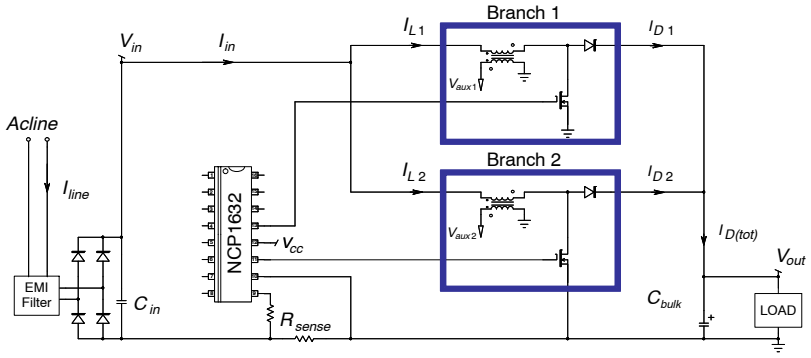


Figure 4. Interleaved PFC Stage

The NCP1632A manages the 180−degree phase shift between the two branches by modulating the oscillator swing as a function of the current cycle duration in the inductor of each individual phase. This **onsemi** proprietary technique ensures an accurate, stable and robust control of the delay between the two branches in all situations (including transient phases) and whatever the operation mode is (CrM or DCM).

The NCP1632A is a voltage mode controller. As a result, the input current is optimally shared between the two branches if they have an inductor of same value. If the inductances differ, out−of−phase operation will not be affected. Simply, the branch embedding the lowest−value inductor, will process more power as:

$$\frac{P_{branch1}}{P_{branch2}} = \frac{L_{branch2}}{L_{branch1}} \quad \text{(eq. 1)}$$

Inductor typical deviation being below ±5%, the power between 2 branches should not differ from more than 10%.

Provided its interleaving capability, the protections it features and the medium− to light−load efficiency enhancements it provides compared to traditional CrM circuits, the NCP1632A is more than recommendable for powers up to 600 W with universal mains and up to 1 kW in narrow mains applications.

NCP1632A On−time Modulation

The NCP1632A incorporates an on−time modulation circuitry to support both the critical and discontinuous conduction modes. Figure 5 portrays the inductor current absorbed in one phase of the interleaved PFC stage. The initial inductor current of each switching cycle is always zero. The inductor current ramps up when the MOSFET is *on*. The slope is (V_{IN}/L) where L is the inductor value. At the end of the on−time (t_1), the coil demagnetization phase starts. The current ramps down until it reaches zero. The duration of this phase is (t_2). The system enters then the dead−time (t_3) that lasts until the next clock is generated.

The ac line current is the averaged inductor current as the result of the EMI filter "polishing" action. Hence, the line current produced by one of the phase is:

$$I_{in} = V_{in}\frac{t_1(t_1 + t_2)}{2T\,L} \quad \text{(eq. 2)}$$

Where ($T = t_1 + t_2 + t_3$) is the switching period and V_{in} is the ac line rectified voltage.

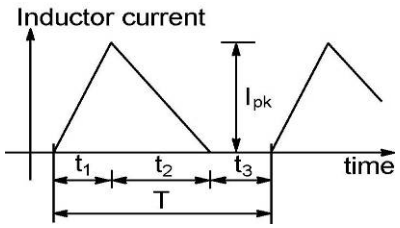


Figure 5. Current Cycle Within a Branch

Equation 2 shows that the input current is proportional to the input voltage if $\left(\frac{t_1\,(t_1 + t_2}{T}\right)$ is a constant.

This is what the NCP1632A does. Using the "Vton processing block" of Figure 5, the NCP1632A modulates t1 so that $\left(\frac{t_1\,(t_1 + t_2}{T}\right)$ remains a constant:

$$\frac{t_1(t_1 + t_2)}{T} = \frac{C_t \cdot V_{REGUL}}{I_t} \quad \text{(eq. 3)}$$

Where C_t and I_t respectively, are the capacitor and charge current of the internal ramp used to control the on−time and V_{REGUL} is the signal derived from the regulation block which adjusts the on−time. This **onsemi** proprietary technique makes the NCP1632A able to support the Frequency Clamped Critical conduction mode of operation, that is, to operate in discontinuous− or in critical−conduction mode according to the conditions, without degradation of

the power factor. Critical conduction mode is naturally obtained when the inductor current cycle is longer than the minimum period controlled by the oscillator. Discontinuous conduction mode is obtained in the opposite situation. In this case, the switching frequency is clamped.

Hence, the averaged current absorbed by one of the phase of the PFC converter:

$$I_{in(phase1)} = I_{in(phase2)} = \frac{V_{in}}{2L} \cdot \frac{C_t \cdot V_{REGUL}}{I_t} \quad \text{(eq. 4)}$$

Given the regulation low bandwidth of PFC systems, ($V_{CONTROL}$) and then (V_{REGUL}) are slow varying signals. Hence, the line current absorbed by each phase is:

$$I_{in(phase1)} = I_{in(phase2)} = k \cdot V_{in} \quad \text{(eq. 5)}$$

Where k is a constant $k = \left[C_t \cdot \frac{V_{REGULAR}}{2} \cdot L \cdot I_t \right]$.

Hence, the input current is then proportional to the input voltage and the ac line current is properly shaped.

This analysis is valid for DCM but also CrM which is just a particular case of this functioning where ($t_3 = 0$). As a result, the NCP1632A automatically adapts to the conditions and jumps from DCM and CrM (and vice versa) without power factor degradation and without discontinuity in the power delivery.

The total current absorbed by the two phases is then:

$$I_{in(total)} = \frac{C_t \cdot V_{REGUL}}{L \cdot I_t} \cdot V_{in} \quad \text{(eq. 6)}$$

This leads to the following line rms current and average input power:

$$I_{in(rms)} = \frac{C_t \cdot V_{REGUL}}{L \cdot I_t} \cdot V_{in(rms)} \quad \text{(eq. 7)}$$

$$P_{in(avg)} = \frac{C_t \cdot V_{REGUL}}{L \cdot I_t} \cdot V_{in(rms)}^2 \quad \text{(eq. 8)}$$

Feedforward:

The C_t timing capacitors (one per phase) are internal and are well matched for an optimal current balancing between the two branches of the interleaved converter.

As detailed in the brown−out section, the I_t current is internally processed to be proportional to the square of the voltage applied to the BO pin (pin 7). Since the BO pin is designed to receive a portion of the average input voltage, the I_t current is proportional to the square of the line magnitude which provides feedforward.

In a typical application, the BO pin voltage is hence:

$$V_{pin7} = \frac{2\sqrt{2}V_{in(rms)}}{\pi} \frac{R_{bo2}}{R_{bo1} + R_{bo2}} \quad \text{(eq. 9)}$$

where R_{bo1} and R_{bo2} are the scaling down resistors for BO sensing (see brown−out section)

In addition, I_t is programmed by the pin 3 resistor so that the maximum on−time obtained when V_{REGUL} is max (1.66 V) is given by:

$$T_{on,max}\ (\mu s) \cong 50 \cdot 10^{-9} \cdot \frac{R_t^2}{V_{pin7}^2} \quad \text{(eq. 10)}$$

From this, we can deduce the input current and power expressions:

$$I_{in(rms)} \cong \frac{62 \cdot 10^{-14} \cdot R_t^2}{L \cdot V_{in(rms)}} \cdot \left(1 + \frac{R_{bo1}}{R_{bo2}}\right)^2 \cdot \frac{V_{REGUL}}{V_{REGUL(max)}} \quad \text{(eq. 11)}$$

$$P_{in(avg)} \cong \frac{62 \cdot 10^{-14} \cdot R_t^2}{L} \cdot \left(1 + \frac{R_{bo1}}{R_{bo2}}\right)^2 \cdot \frac{V_{REGUL}}{V_{REGUL(max)}} \quad \text{(eq. 12)}$$

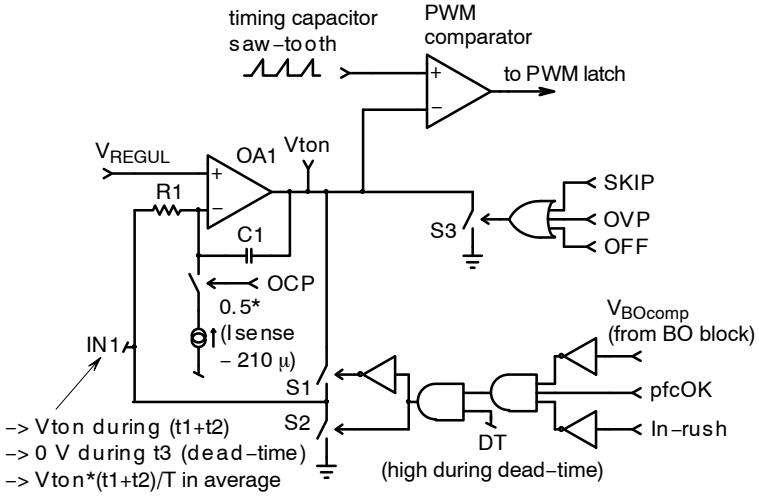


Figure 6. V_{ton} Processing Circuit

Regulation Block and Low Output Voltage Detection

A trans−conductance error amplifier with access to the inverting input and output is provided. It features a typical trans−conductance gain of 200 μS and a typical capability of ±20 μA. The output voltage of the PFC stage is typically scaled down by a resistors divider and monitored by the inverting input (feed−back pin – pin2). The bias current is minimized (less than 500 nA) to allow the use of a high impedance feed−back network. The output of the error amplifier is pinned out for external loop compensation (pin5). A type−2 compensator is generally applied between pin5 and ground, to set the regulation bandwidth in the range of 20 Hz, as need in PFC applications (refer to application note AND8407).

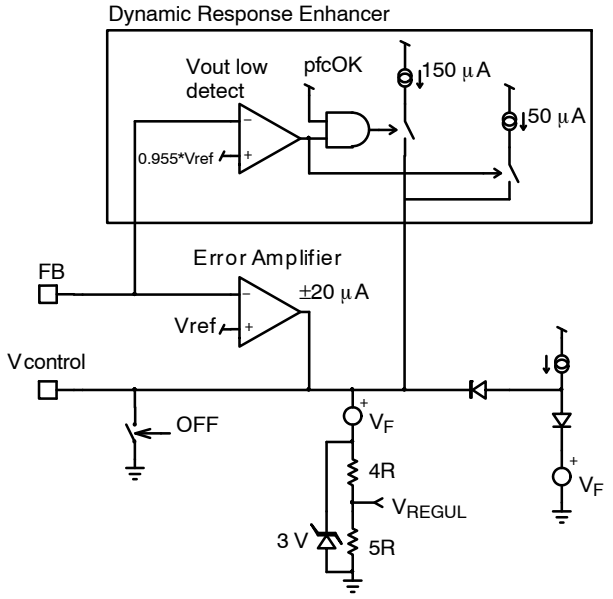


Figure 7. Regulation Block

Provided the low bandwidth of the regulation loop, sharp variations of the load, may result in excessive over and under−shoots. Over−shoots are limited by the Over−Voltage Protection (see OVP section). A dynamic Response Enhancer circuitry (DRE) is embedded to contain the under−shoots. Practically, an internal comparator monitors the feed−back signal (V_{FB}) and connects a 200 μA current source to speed−up the charge of the compensation network when V_{FB} is lower than 95.5% of its nominal value. Finally, it is like if the comparator multiplied the error amplifier gain by about 10.

One must note that a large part of the DRE current source (150 μA out of 200 μA) cannot be enabled until the converter output voltage has reached its target level (that is when the "pfcOK" signal of the block diagram, is high). This is because, at the beginning of operation, it is generally welcome that the compensation network charges slowly and gradually for a soft start−up.

The swing of the error amplifier output is limited within an accurate range:

- It is maintained above a lower value (V_F – 0.6 V typically) by the "low clamp" circuitry. When this circuitry is activated, the power demand is minimum and the NCP1632A enters skip mode (the controller stops pulsating) until the clamp is no more active.
- It is clamped not to exceed 3.0 V + the same V_F voltage drop.

Hence, V_{pin5} features a 3 V voltage swing. V_{pin5} is then offset down by (V_F) and divided by three before it connects to the "V_{ton} processing block" and the PWM section. Finally, the output of the regulation is a signal ("V_{REGUL}" of the block diagram) that varies between 0 and 1.66 V.

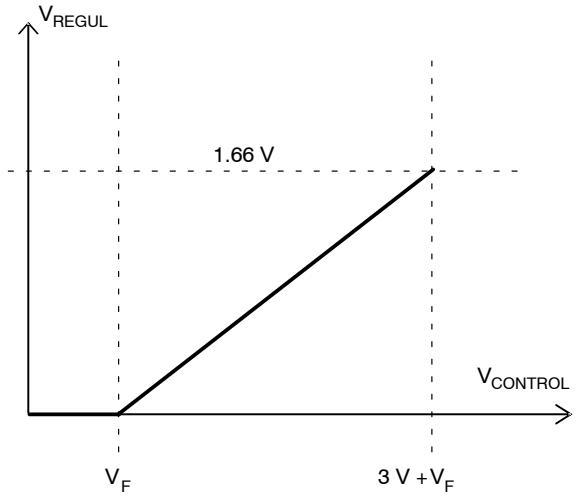


Figure 8. V_{REGUL} versus $V_{CONTROL}$

Zero Current Detection

While the on time is constant, the core reset time varies with the instantaneous input voltage. The NCP1632A detects the demagnetization completion by sensing the inductor voltage. Sensing the voltage across the inductor allows an accurate zero current detection, more specifically, by detecting when the inductor voltage drops to zero. Monitoring the inductor voltage is not an economical solution. Instead, a smaller winding is taken off of the boost inductor. This winding (called the "zero current detection" or ZCD winding) gives a scaled version of the inductor voltage that is easily usable by the controller. Furthermore, this ZCD winding is coupled so that it exhibits a negative voltage during the MOSFET conduction time (flyback configuration) as portrayed by Figure 9.

In that way, the ZCD voltage ("V_{AUX}") falls and starts to ring around zero volts when the inductor current drops to zero. The NCP1632A detects this falling edge and prevents any new current cycle until it is detected.

Figure 9 shows how it is implemented.

For each phase, a ZCD comparator detects when the voltage of the ZCD winding exceeds its upper threshold (0.5 V typically). When this is the case, the coil is in demagnetization phase and the latch L_{ZCD} is set. This latch is reset when the next driver pulse occurs. Hence the output of this latch (Q_{ZCD}) is high during the whole off−time (demagnetization time + any possible dead time). The output of the comparator is also inverted to form a signal which is AND'd with the Q_{ZCD} output so that the AND gate output (V_{ZCD}) turns high when the V_{AUX} voltage goes below zero (below the 0.25 V lower threshold of the ZCD comparator to be more specific). As a result, the ZCD circuitry detects the V_{AUX} falling edge.

It is worth noting that as portrayed by Figure 10, V_{AUX} is also representative of the MOSFET drain−source voltage ("V_{DS}"). More specifically, when V_{AUX} is below zero, V_{DS} is minimal (below the input voltage V_{IN}). That is why V_{ZCD} is used to enable the driver so that the MOSFET turns on when its drain−source voltage is low. Valley switching reduces the losses and interference.

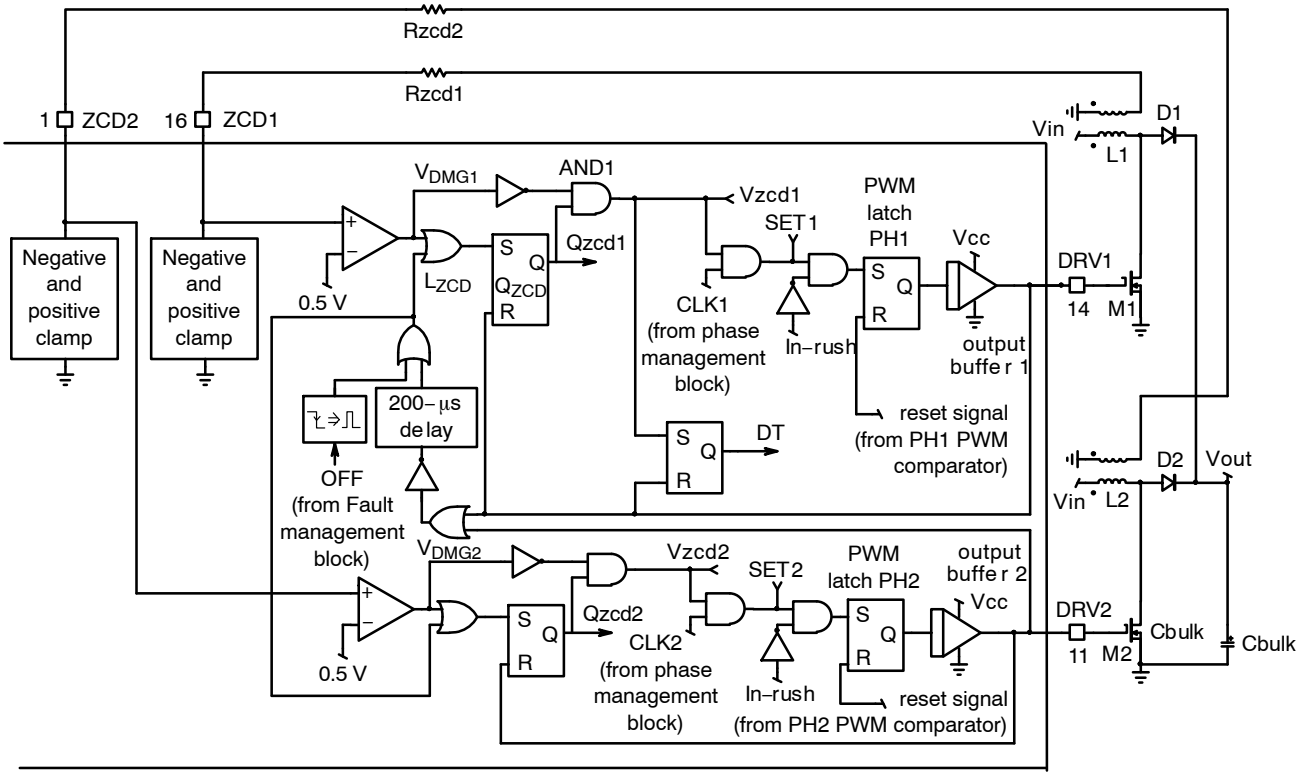


Figure 9. Zero Current Detection

At startup or after an inactive period (because of a protection that has tripped for instance), there is no energy in the ZCD winding and therefore no voltage signal to activate the ZCD comparator. This means that the driver will never turn on. To avoid this, an internal watchdog timer is integrated into the controller. If the driver remains low for more than 200 µs (typical), the timer sets the L_{ZCD} latch as the ZCD winding signal would do. Obviously, this 200 µs delay acts as a minimum off−time if there is no demagnetization winding voltage is detected.

To prevent negative voltages on the ZCD pins (ZCD1 for phase 1 and ZCD2 for phase 2), these pins are internally clamped to about 0 V when the voltage applied by the corresponding ZCD winding is negative. Similarly, the ZCD pins are clamped to $V_{ZCD(high)}$ (10 V typical), when the ZCD voltage rises too high. Because of these clamps, a resistor (R_{ZCD1} and R_{ZCD2} of Figure 9) is necessary to limit the current from the ZCD winding to the ZCD pin. The clamps are designed to respectively source and sink 5 mA. It is hence recommended to dimension R_{ZCD1} and R_{ZCD2} to limit the ZCD1 and ZCD2 pins current below 5 mA.

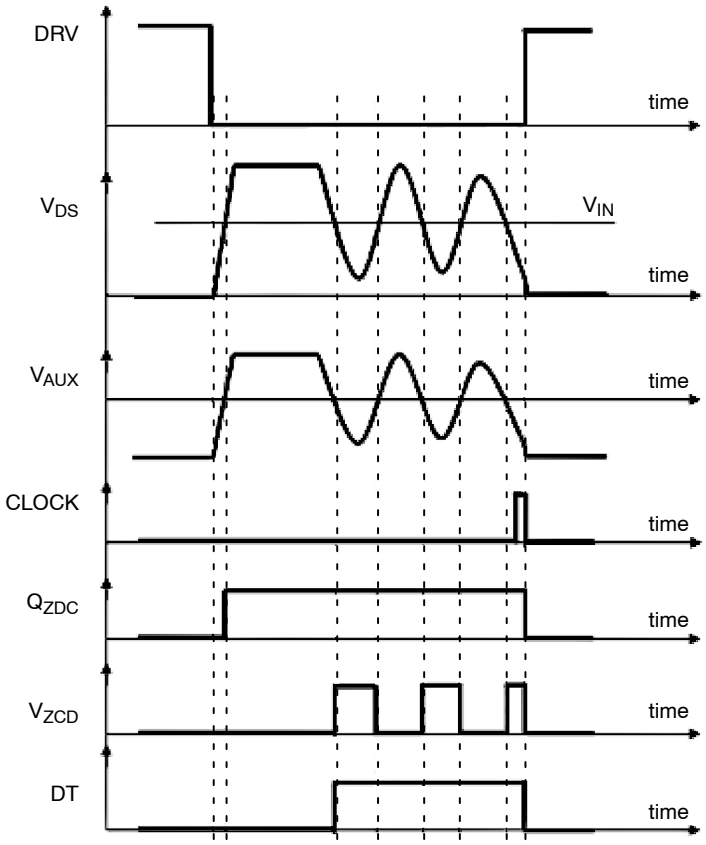


Figure 10. Zero Current Detection Timing Diagram (V_{AUX} is the Voltage Provided by the ZCD Winding)

Current Sense

The NCP1632A is designed to monitor a negative voltage proportional to the input current, i.e., the current drawn by the two interleaved branches (I_{in}). As portrayed by Figure 11, a current sense resistor (R_{CS}) is practically inserted in the return path to generate a negative voltage (V_{CS}) proportional to I_{in}.

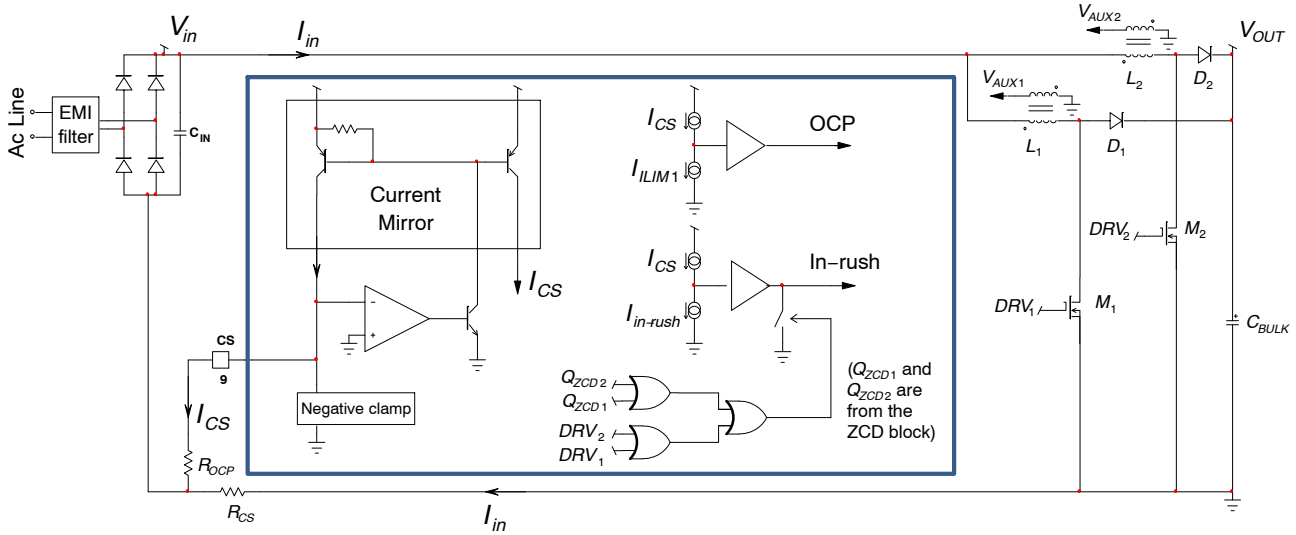


Figure 11. Current Sense Block

The NCP1632A uses V_{CS} to detect when I_{in} exceeds its maximum permissible level. To do so, as sketched by Figure 11, the circuit incorporates an operational amplifier that sources the current necessary to maintain the CS pin voltage near zero. By inserting a resistor R_{OCP} between the CS pin and R_{CS}, we adjust the current that is sourced by the CS pin (I_{CS}) as follows:

$$-\left(R_{CS} \cdot I_{in}\right) + \left(R_{OCP} \cdot I_{CS}\right) \cong 0 \qquad \text{(eq. 13)}$$

Which leads to:

$$I_{CS} = \frac{R_{CS}}{R_{OCP}} I_{in} \qquad \text{(eq. 14)}$$

In other words, the CS pin sources a current (I_{CS}) which is proportional to the input current.

Two functions use I_{CS}: the over current protection and the in−rush current detection.

Over−Current Protection (OCP)

If I_{CS} exceeds I_{ILIM1} (210 μA typical), an over−current is detected and the on−time is decreased proportionally to the difference between the sensed current I_{in} and the 210 μA OCP threshold.

The on−time reduction is done by injecting a current I_{neg} in the negative input of the "V_{TON} processing circuit" OPAMP. (See Figure 6)

$$I_{neg} = \frac{I_{CS} - I_{ILIM1}}{2} \qquad \text{(eq. 15)}$$

This current is injected each time the OCP signal is high.

The maximum coil current is:

$$I_{in(max)} = \frac{R_{OCP}}{R_{CS}} I_{ILIM1} \qquad \text{(eq. 16)}$$

In−rush Current Detection

When the PFC stage is plugged to the mains, the bulk capacitor is abruptly charged to the line voltage. The charge current (named in−rush current) can be extremely huge particularly if no in−rush limiting circuitry is implemented. The power switches should not turn on during this severe transient. If not, they may be over−stressed and finally damaged. That is why, the NCP1632A permanently monitors the input current and delays the MOSFET start of switching until (I_{in}) has vanished. This is the function of the I_{CS} comparison to the $I_{in-rush}$ threshold (14 μA typical). When I_{CS} exceeds $I_{in-rush}$, the comparator output ("In−rush") is high and prevents the PWM latches from setting (see block diagram). Hence, the two drivers (DRV1 and DRV2) cannot turn high and the MOSFETs stay off. This is to guarantee that the MOSFETs remain open as long as if the input current exceeds 10% of the maximum current limit. Again, this feature protects the MOSFETs from the possible excessive stress it could suffer from if it was allowed to turn on while a huge current flowed through the coil as it can be the case at start−up or during an over−load transient.

The propagation delay ($I_{CS} < I_{in-rush}$) to (drive outputs high) is in the range of few μs.

However when the circuit starts to operate, the NCP1632A disables this protection to avoid that the current produced by one phase and sensed by the circuit prevents the other branch from operating. Practically, some logic grounds the In−rush protection output when it detects the presence of "normal current cycles". This logic simply consists of the OR combination of the Drive and demagnetization signals as sketched by Figure 11.

Over−Voltage Protection

While PFC circuits often use one single pin for both the Over−Voltage Protection (OVP) and the feed−back, the NCP1632A dedicates one specific pin for the under−voltage and over−voltage protections. The NCP1632A configuration allows the implementation of two separate feed−back networks (see Figure 13):

1. One for regulation applied to pin 2.
2. Another one for the OVP function (pin 8).

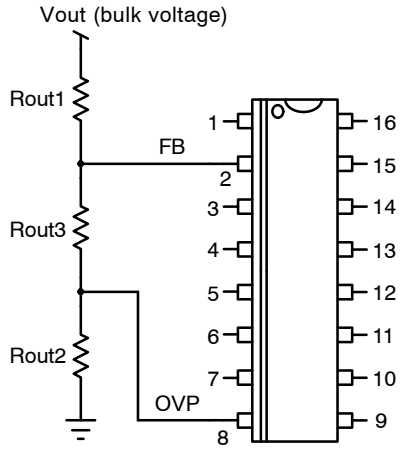


Figure 12. Configuration with One Feed−back Network for Both OVP and Regulation

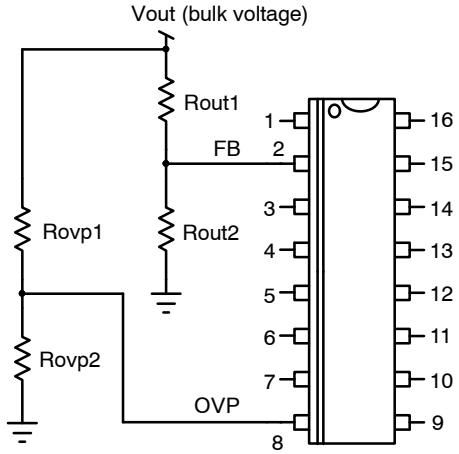


Figure 13. Configuration with Two Separate Feed−back Networks

The double feed−back configuration (Figure 13) offers some up−graded safety level as it protects the PFC stage even if there is a failure of one of the two feed−back arrangements. In this case:

The bulk regulation voltage (“$V_{out(nom)}$”) is:

$$V_{out(nom)} = \frac{R_{out1} + R_{out2}}{R_{out2}} \cdot V_{ref} \quad \text{(eq. 17)}$$

The OVP level (“$V_{out(ovp)}$”) is:

$$V_{out(ovp)} = \frac{R_{ovp1} + R_{ovp2}}{R_{ovp2}} \cdot V_{ref} \quad \text{(eq. 18)}$$

Where V_{ref} is the internal reference voltage (2.5 V typically)

Now, if wished, one single feed−back arrangement is possible as portrayed by Figure 12. The regulation and OVP blocks having the same reference voltage (V_{ref}), the resistance ratio R_{out2} over R_{out3} adjusts the OVP threshold. More specifically,

The bulk regulation voltage (“$V_{out(nom)}$”) is:

$$V_{out(nom)} = \frac{R_{out1} + R_{out2} + R_{out3}}{R_{out2} + R_{out3}} \cdot V_{ref} \quad \text{(eq. 19)}$$

The OVP level (“$V_{out(ovp)}$”) is:

$$V_{out(ovp)} = \frac{R_{out1} + R_{out2} + R_{out3}}{R_{out2}} \cdot V_{ref} \quad \text{(eq. 20)}$$

The ratio OVP level over regulation level is:

$$\frac{V_{out(ovp)}}{V_{out(nom)}} = 1 + \frac{R_{out3}}{R_{out2}} \quad \text{(eq. 21)}$$

For instance, ($V_{out(nom)}$ = 105% · $V_{out(nom)}$) leads to: (R_{out3} = 5% · R_{out2}).

When the circuit detects that the output voltage exceeds the OVP level, it maintains the power switch open to stop the power delivery.

Oscillator Section – Phase Management

The oscillator generates the clock signal that dictates the maximum switching frequency (f_{osc}) of the interleaved PFC stage. In other words, each of the two interleaved branches cannot operate above half the oscillator frequency (f_{osc}/2). The oscillator frequency (f_{osc}) is adjusted by the capacitor applied to OSC pin (pin 4). Typically, a 220 pF capacitor approximately leads to a 260 kHz oscillator operating frequency, i.e., to a 130 kHz clamp frequency for each branch.

As shown by Figure 14, a current source I_{CH} (140 μA typically) charges the OSC pin capacitor until its voltage exceeds $V_{OSC(high)}$ (5 V typically). At that moment, the oscillator enters a discharge phase for which I_{DISCH} (105 μA typ.) discharges the OSC pin capacitor. This sequence lasts until V_{OSC} goes below the oscillator low threshold V_{OSCL} and a new charging phase starts*. An internal signal (“*SYNC*” of Figure 14) is high during the discharge phase. A divider by two uses the *SYNC* information to manage the phases of the interleaved PFC: the first *SYNC* pulse sets “phase 1”, the second one, “phase 2”, the third one phase 1 again… etc.

According to the selected phase, *SYNC* sets the relevant “Clock generator latch” that will generate the clock signal (“*CLK*1” for phase 1, “*CLK*2” for phase 2) when *SYNC* drops to zero.

Actually, the drivers cannot turn on at this very moment if the inductor demagnetization is not complete. In this case, the clock signal is maintained high and the discharge time is prolonged although V_{OSC} is below V_{OSCL}, until when the core being reset, the drive pin turns high. The prolonged OSC discharge ensures a substantial 180−degree phase shift in CrM, out−of−phase operation being in essence, guaranteed in DCM. In the two conditions (CrM or DCM), the interleaved operation is stable and robust.

*As detailed in the following sections, V_{OSCL} is $V_{OSC(low)}$ − 4 V typically − by default to set the frequency clamp level used in heavy−load conditions. V_{OSCL} is varied between 1 and 3 V in FFOLD mode (frequency foldback mode) in response the FFOLD pin voltage.

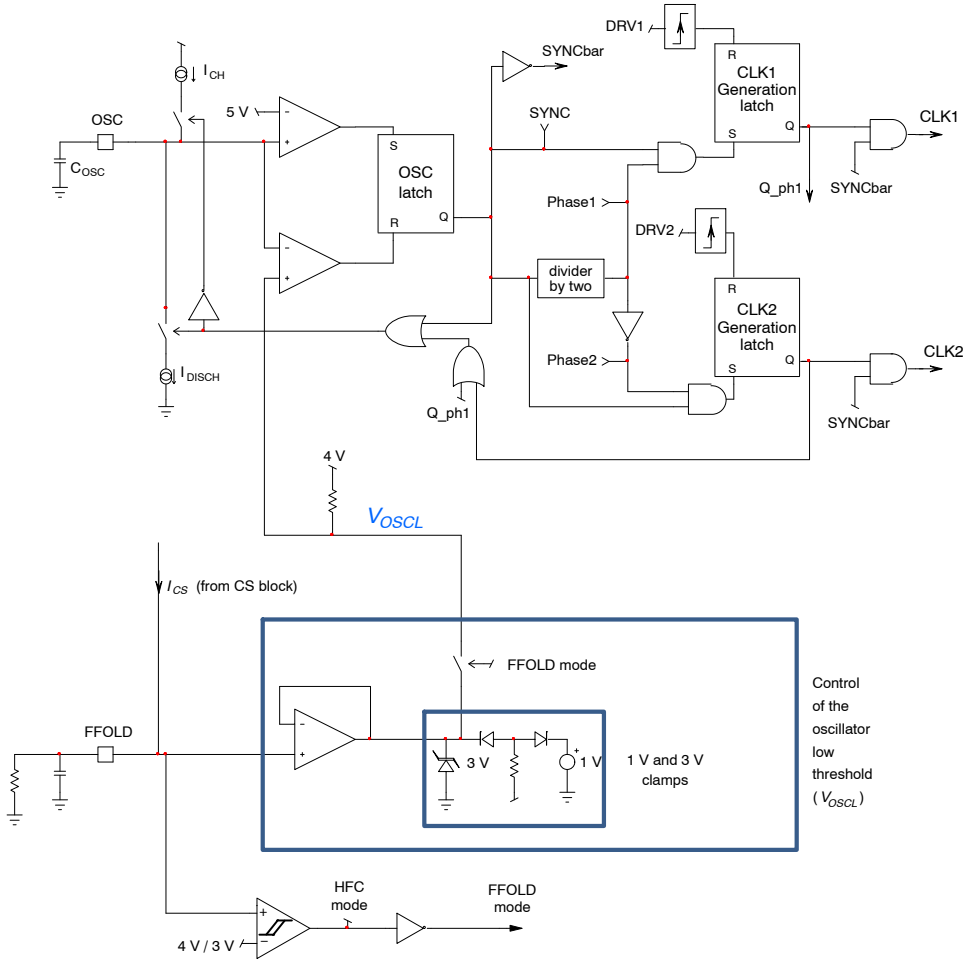


Figure 14. FFOLD Mode Management

If a capacitor C_{OSC} is applied to the OSC pin, the oscillator frequency is provided by:

$$f_{osc} \cong \frac{60 \cdot 10^{-6}}{C_{OSC} + (10 \cdot 10^{-12})} \quad \text{(eq. 22)}$$

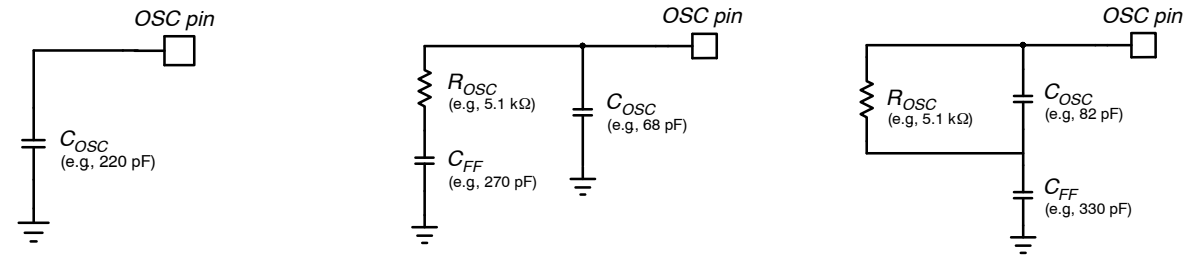
And the switching frequency of each individual branch is clamped to the following f_{clamp}:

$$f_{clamp} = \frac{f_{osc}}{2} \cong \frac{30 \cdot 10^{-6}}{C_{OSC} + (10 \cdot 10^{-12})} \quad \text{(eq. 23)}$$

Recommended Configuration

As detailed above, the circuit automatically transitions between CrM and DCM depending on the current cycle duration being longer or shorter than the clamp frequency set by the oscillator. However, these transitions can lead to small discontinuities of the line current. To avoid them, the circuit should be operated in CrM without frequency−clamp interference when the line current is high and in deep DCM when it is below a programmed level. Deep DCM means that the switching frequency is low enough to ensure a significant dead−time and prevent transitions between CrM and DCM within the input voltage sinusoid.

In Figure 15 a) configuration, a single oscillator sets a frequency clamp. For instance, C_{OSC} = 220 pF forces 120 kHz to be the maximum frequency within each branch (the FFOLD mode reduces this level in light load conditions). Such a clamp value is likely to force DCM operation in part of the input voltage sinusoid. To be able to force full CrM operation over a large working range, we would need to reduce C_{OSC} to a very low value (if not, the clamp frequency can be lower than the switching one leading to DCM operation near the line zero crossing in particular). Still however, the oscillator must keep able to keep synchronized to the current cycle for proper out−of−phase control. This requires the oscillator swing to not to exceed its 1 V to 5 V range even in heavy load conditions when the switching frequency in each individual branch generally drops below 100 kHz. This is generally not possible with a single small capacitor on the OSC pin.



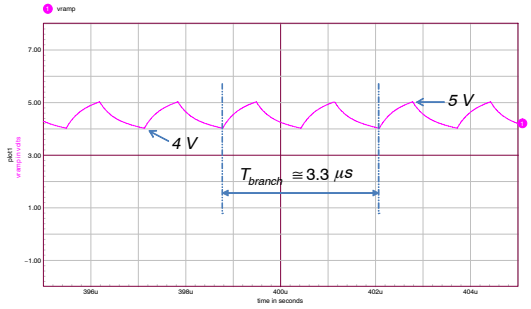
a) Basic configuration b) Option 1 c) Option 2

Figure 15. External Components Driving the OSC Pin

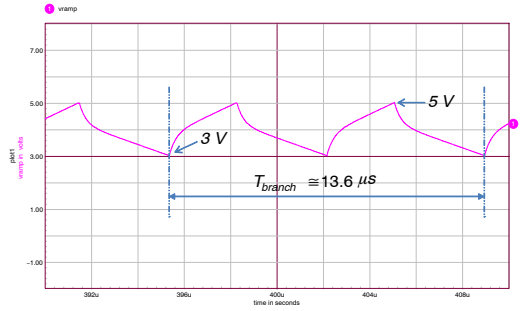
Instead, the schematic of either Figure 15 b) or Figure 15 c) is to be used where:

- C_{OSC} (which value is much less than the second capacitance C_{FF}) sets the high−frequency operation necessary for operating in CrM
- R_{OSC} limits the influence of the C_{FF} capacitor as long as the oscillator swing remains below (R_{OSC}.I_{OSC}) where I_{OSC} is the charge or discharge current depending on the sequence. The voltage across C_{OSC} being limited by R_{OSC} (to about 1 V with 5.1 kΩ), the second much−higher−value capacitor (C_{FF}) is engaged when heavy−load CrM operation imposes a larger oscillator swing.
- C_{FF} sets the frequency in light load where the frequency foldback can force deep DCM operation (deep DCM means operation with a large dead−time to be far from the zone where the circuit can transition from CrM to DCM and vice versa). As previously mentioned, C_{FF} also ensures that the oscillator voltage can stay above 1 V in deep CrM conditions.

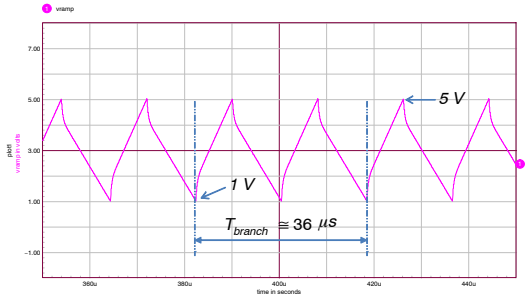
Finally, Figure 15 b) and c) configurations provide some kind of variable−capacitance oscillator. For instance, Option b) provides the following typical characteristics:



300 kHz frequency clamp in HFC mode (V_{FFOLD} > 4 V)



73 kHz frequency clamp when entering FFOLD mode (V_{FFOLD} = 3 V)



28 kHz minimum frequency clamp (deepest DCM @ V_{FFOLD} = 1 V)

Figure 16. Clamp Frequency in Each Individual Branch with the Configuration of Figure 15 b)

Figure 17 illustrates the oscillator operation at a low FFOLD voltage.

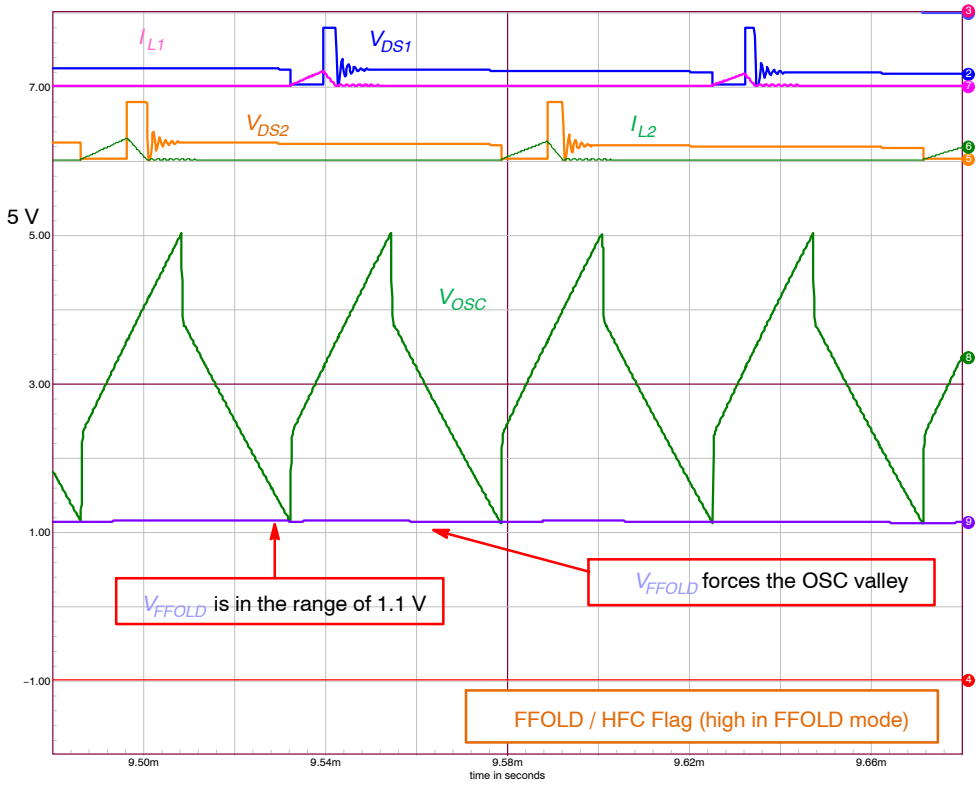


Figure 17. Operation at a Low V_{FFOLD} Value (V_{FFOLD} = 1.1 V)

HFC vs FFOLD Modes

The NCP1632A optimizes the PFC stage efficiency over the whole load range by entering the frequency foldback (FFOLD) mode when the line current magnitude is lower than a programmed level (see next section). More specifically, the circuit operates in:

- Frequency foldback (FFOLD) mode when the line current magnitude is lower than a programmed level. In this mode, the circuit frequency clamp level is reduced as a function of the FFOLD pin voltage in order to reduce the frequency in medium− and light−load operation. The frequency can decrease down to about 30 kHz at very low power (depending on the OSC pin capacitor)
- High frequency clamp (HFC) mode when the line current is high. In this mode, the clamp level of the switching frequency is set high so that the PFC stage mostly runs in critical conduction mode which is more efficient than the discontinuous conduction mode in heavy load conditions.

The transitions between the HFC and FFOLD modes and the frequency foldback characteristics are controlled by the FFOLD pin.

Frequency Foldback (FFOLD) Management

As detailed in the “current sense” section, the NCP1632A CS pin sources a current proportional to the input current (I_{CS} of Figure 14). I_{CS} is internally copied and sourced out of the FFOLD pin. This current is changed into a dc voltage by means of an external (R//C) network applied to the FFOLD pin. The obtained V_{FFOLD} voltage is proportional to the line average current. As illustrated by Figure 18, the PFC stage enters the frequency foldback mode (FFOLD mode) when V_{FFOLD} goes below 3.0 V, and recovers high−frequency clamp mode (HFC mode) when the FFOLD voltage exceeds 4 V.

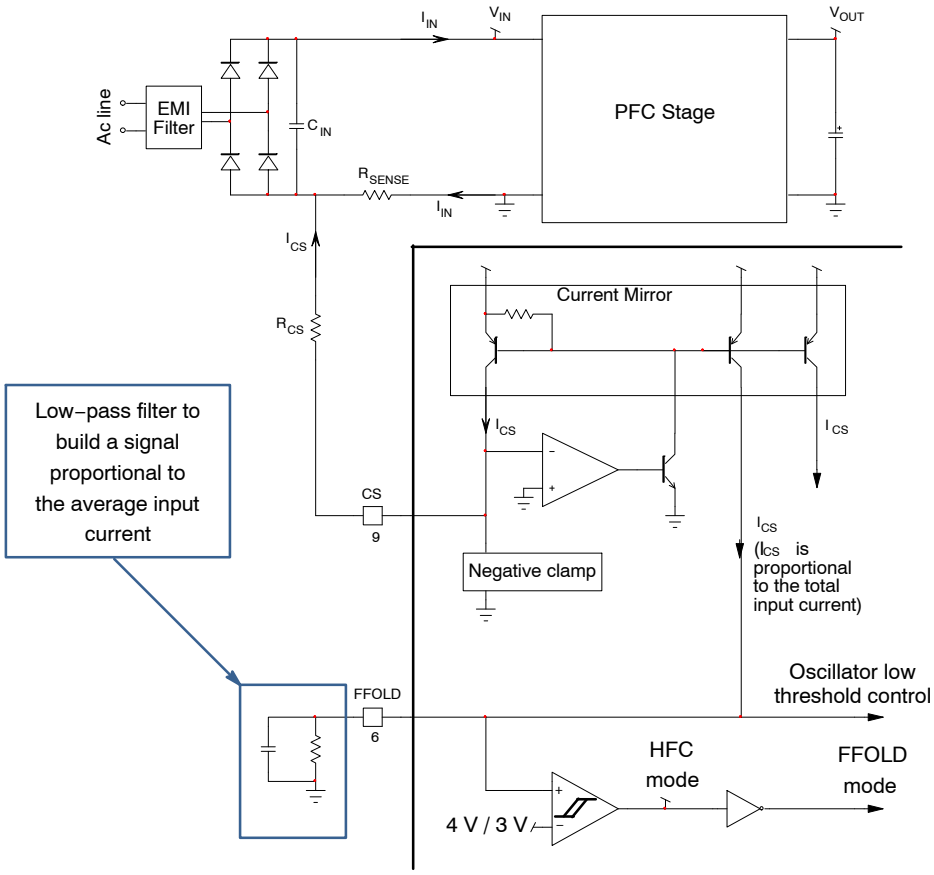


Figure 18. Frequency Foldback Control

In HFC mode, the oscillator lower threshold (V_{OSCL}) is fixed and equal to $V_{OSC(low)}$ (4 V typically).

In FFOLD mode, V_{OSCL} is modulated by the FFOLD pin voltage as follows:

- $V_{OSCL} = V_{FFOLD}$ if V_{FFOLD} is between 1 and 3 V
- V_{OSCL} = 1 V if V_{FFOLD} is below 1 V
- V_{OSCL} = 3 V if V_{FFOLD} exceeds 3 V

As an example, the FFOLD external resistor can be selected so that (V_{FFOLD} = 3 V) when the line current threshold is equal to 20% of the maximum current.

In a 90 to 270 V rms application, above criterion leads the PFC stage to enter FFOLD mode at:

- 20% load at 90 V rms
- 60% load at 270 V rms

The PFC stage will recover HFC mode (V_{FFOLD} = 4 V) at:

- 27% load at 90 V rms
- 81% load at 270 V rms

Above values assume a ripple−free V_{FFOLD} voltage. The power thresholds for transition can be shift and the hysteresis reduced by the V_{FFOLD} ripple.

At the transition between the two modes, the oscillator low threshold is 3 V. In the example of Figure 19, this leads the branch clamp frequency to be 73 kHz when entering and just before leaving the FFOLD mode.

Figure 19 shows a “natural” transition FFOLD to HFC mode.

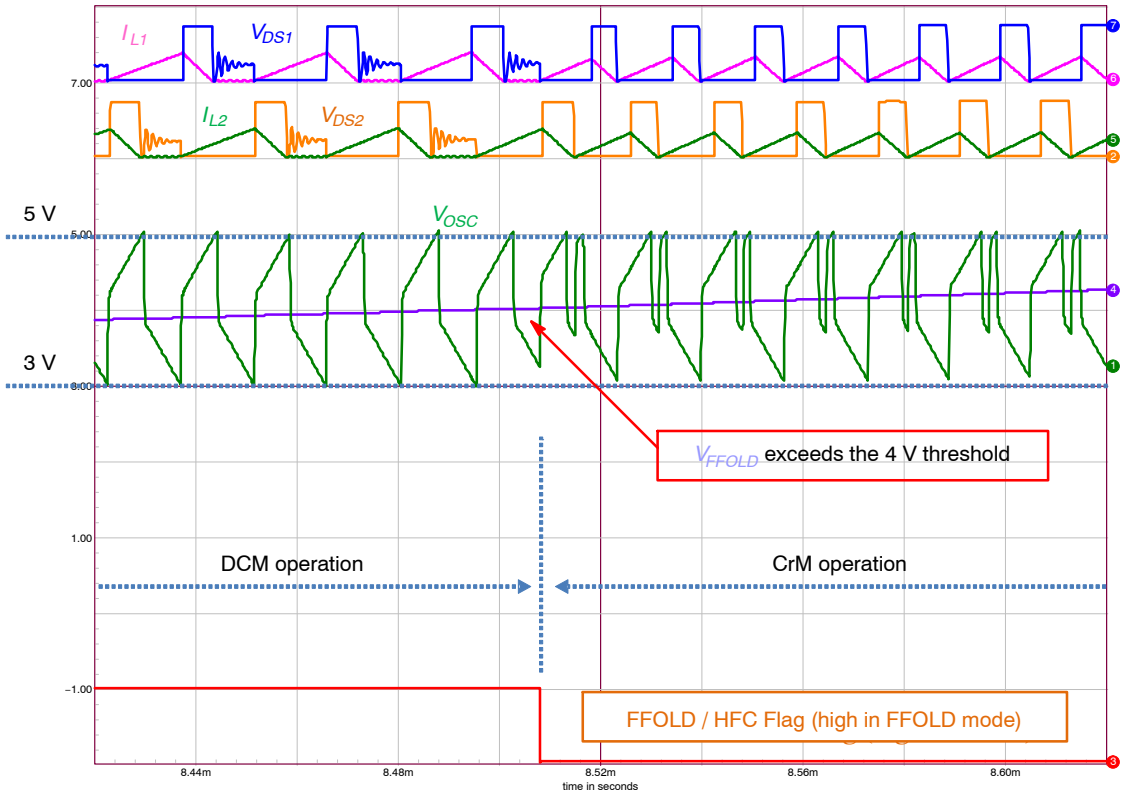


Figure 19. "Natural" Transition FFOLD to HFC Mode when V_{FFOLD} exceeds 4 V

HFC−mode Recovery

The FFOLD pin sources a current proportional to the input current. Placing a resistor and a capacitor between the FFOLD and GND pins, we obtain the voltage representative of the line current magnitude necessary to control the frequency foldback characteristics. The NCP1632A naturally leaves the FFOLD mode operation when the sensed input current being large enough, the FFOLD pin voltage (V_{FFOLD}) exceeds 4 V. Such a FFOLD to HFC transition is shown by Figure 19.

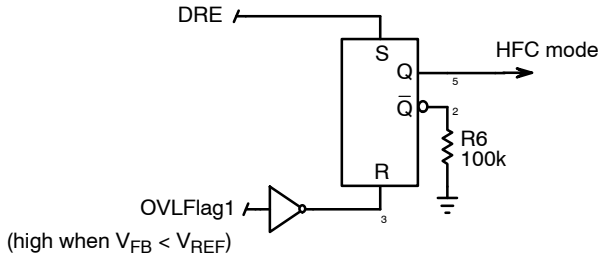


Figure 20. Easing HFC−mode Recovery

Now, the FFOLD pin is heavily filtered and this time constant may cause long V_{FFOLD} settling phases. If while in very light−load conditions, the load abruptly rises, the FFOLD pin time constant may dramatically delay the HFC−mode recovery. As a result, during the FFOLD mode of operation, the PFC stage may run in DCM and may not be able to provide the full power. To solve this, the NCP1632A forces HFC operation whenever the DRE comparator trips* and remains in HFC mode until the output voltage recovers its regulation level (that is when *OVLFlag*1 of Figure 21 turns low). At that moment, the conduction mode is normally selected as a function of the FFOLD pin voltage. See Figure 20.

*The dynamic response enhancer (DRE) comparator trips when the output voltage drops below 95.5% of its regulation level.

Skip Mode of Operation

The circuit enters skip mode when the regulation block output ($V_{CONTROL}$) drops to its 0.6 V lower clamp level. At very light load and low line conditions, on−times can be short enough no to enter the low−consumption skip mode. To prevent such an inefficient continuous operation from occurring, the NCP1632A forces a minimum on−time which corresponds to 10% the maximum on−time.

This does not mean that the PFC stage will enter skip mode when the load is less than 10% of the full load (or even much more considering the necessary headroom in the max on−time setting when selecting R_t). Since, the NCP1632A reduces the switching frequency in light load (FFOLD mode), this minimum on−time corresponds to much lower power levels, typically, in the range of 2% of the full power.

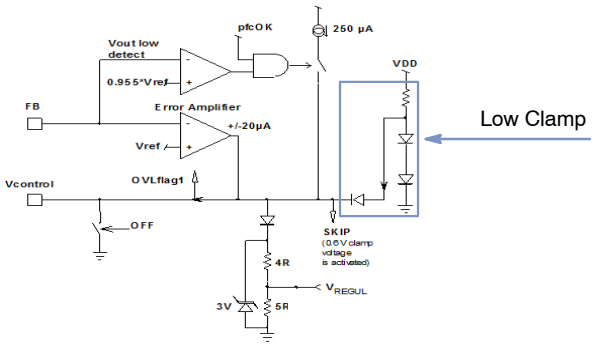


Figure 21. $V_{CONTROL}$ Low Clamp

The circuit consumption is minimized (below 1 mA) for a skipping period of time.

PfcOK / REF5V Signal

The NCP1632A can communicate with the downstream converter. The signal "pfcOK/REF5V" is high (5 V) when the PFC stage is in nominal operation and low otherwise.

More specifically, "pfcOK/REF5V" is low:

- Whenever a major fault condition is detected which turns off the circuit, i.e.:
  - Incorrect feeding of the circuit ("UVLO" high). The UVLO signal turns high when V_{CC} drops below $V_{CC(OFF)}$ (10 V typically) and remains high until V_{CC} exceeds $V_{CC(ON)}$ (12 V typically).
  - Excessive die temperature detected by the thermal shutdown.
  - Under−Voltage Protection ("UVP" high)
  - Brown−out situation ("BONOK" high)
  - Latching−off of the circuit by an external signal applied to pin 10 and exceeding 2.5 V ("STDWN" of the block diagram turns high).
  - Too low the current sourced by the R_t pin ("$R_{t(open)}$")
- During the PFC stage start−up, that is, until the output voltage reaches its regulation level. The start−up phase is detected by the latch "L_{STUP}" of the block diagram. "L_{STUP}" is in high state when the circuit enters or recovers operation after one of above major faults and resets when the error amplifier stops charging its output capacitor, that is, when the output voltage of the PFC stage has reached its desired regulation level. At that moment, "STUP" falls down to indicate the end of the start−up phase.

Finally, "pfcOK/REF5V" is high when the PFC output voltage is properly and safely regulated. "pfcOK/REF5V" should be used to allow operation of the downstream converter.

Brown−Out Protection

The brown−out pin is designed to receive a portion of the input voltage (V_{IN}). As V_{IN} is a rectified sinusoid, a capacitor must be applied to the BO pin so that V_{BO} is proportional to the average value of V_{IN}.

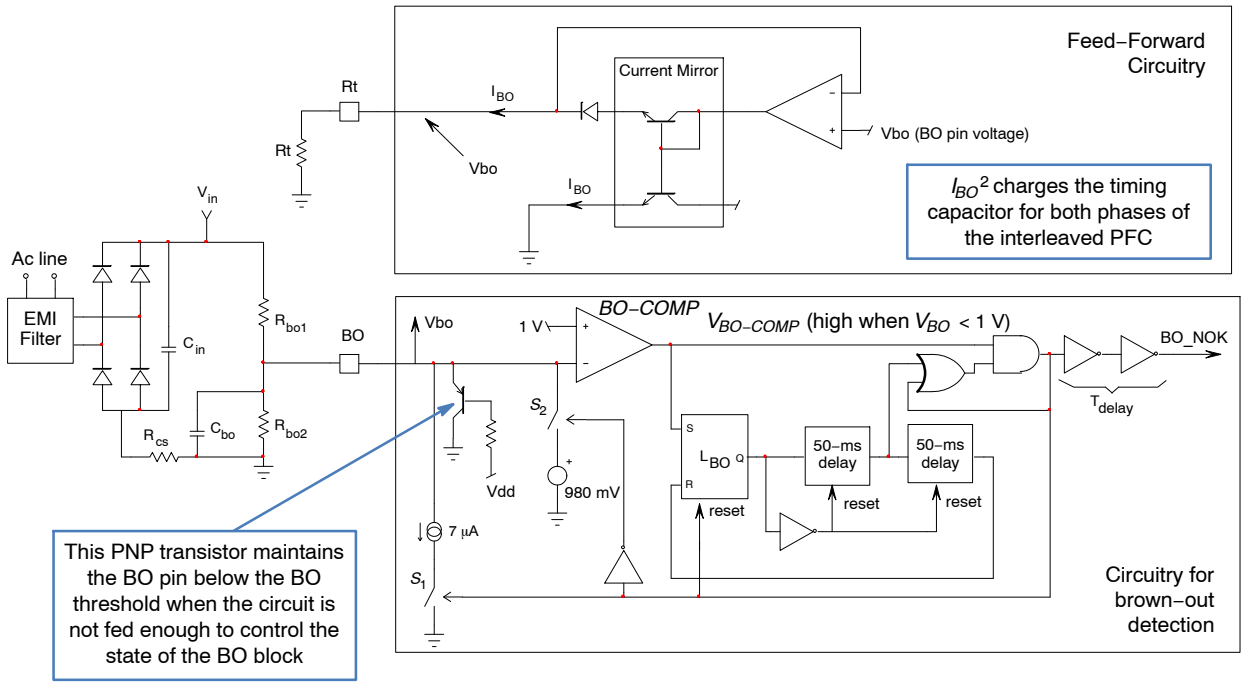


Figure 22. Brown−out Block

The BO pin voltage is used by two functions (refer to Figure 22):

- Feedforward. Generation of an internal current proportional to the input voltage average value (I_{Rt}). V_{BO} is buffered and made available on the R_t pin (pin 3). Hence, placing a resistor between pin 3 and ground, enables to adjust a current proportional to the average input voltage. This current (I_{Rt}) is internally copied and squared to form the charge current for the internal timing capacitor of each phase. Since this current is proportional to the square of the line magnitude, the conduction time is made inversely proportional to the line magnitude. This feed−forward feature makes the transfer function and the power delivery independent of the ac line level. Only the regulation output (V_{REGUL}) controls the power amount. Note that if the I_{Rt} current is too low (below 7 μA typically), the controller goes in OFF mode to avoid damaging the MOSFETs with too long conduction time. In particular, this addresses the case when the R_t pin is open.
- Brown−out protection. A 7 μA current source lowers the BO pin voltage when a brown−out condition is detected. This is for hysteresis purpose as required by this function. In traditional applications, the monitored voltage can be very different depending on the phase:
  - Before operation, the PFC stage is off and the input bridge acts as a peak detector (refer to Figure 23). As a consequence, the input voltage is approximately flat and nearly equates the ac line amplitude: $v_{in}(t) = \sqrt{2} \cdot V_{in,rms}$, where $V_{in,rms}$ is the rms voltage of the line. Hence, the voltage applied to the BO pin (pin 7) is: $V_{BO} = \sqrt{2} \cdot V_{in,rms} \cdot \frac{R_{bo2}}{R_{bo1} + R_{bo2}}$.
  - After the PFC stage has started operation, the input voltage becomes a rectified sinusoid and the voltage applied to pin7 is: $V_{BO} = \frac{2\sqrt{2} \cdot V_{in,rms}}{\pi} \cdot \frac{R_{bo2}}{R_{bo1} + R_{bo2}}$, i.e., about 64% of the previous value. Therefore, the same line magnitude leads to a V_{BO} voltage which is 36% lower when the PFC is working than when it is off. That is why a large hysteresis (in the range of 50% of the upper threshold) is required.

Other applications may require a different hysteresis amount. That is why the hysteresis is made programmable and dependent on the internal 7 μA current source. More specifically, re−using the components of Figure 22:

- The line upper BO threshold is: $(V_{in,rms})_{boH} = \frac{1}{\sqrt{2}} \cdot \frac{R_{bo1} + R_{bo2}}{R_{bo2}} \left(V_{BO(th)} + \frac{R_{bo1} \cdot R_{bo2} \cdot I_{BO}}{R_{bo1} + R_{bo2}} \right)$ where $V_{BO(th)}$ is the BO comparator threshold (1 V typically) and I_{BO}, the 7 μA current source.
- The line lower threshold is: $(V_{in,rms})_{boL} = \frac{\pi}{2\sqrt{2}} \cdot \frac{R_{bo1} + R_{bo2}}{R_{bo2}} \cdot V_{BO(th)}$

Hence the ratio upper over lower threshold is: $\frac{(V_{in,rms})_{boH}}{(V_{in,rms})_{boL}} = \frac{2}{\pi} \cdot \left(1 + \frac{R_{bo1} \cdot R_{bo2} \cdot I_{BO}}{(R_{bo1} + R_{bo2} \cdot V_{BO(th)}} \right)$

As in general R_{bo1} is large compared to R_{bo2}, the precedent equation can simplify as follows: $\frac{(V_{in,rms})_{boH}}{(V_{in,rms})_{boL}} \cong \frac{2}{\pi} \cdot \left(1 + \frac{R_{bo2} \cdot I_{BO}}{V_{BO(th)}} \right)$

Details of Operation of the Circuitry for Brown−out Detection

In nominal operation, the voltage applied to pin 7 must be higher than the 1 V internal voltage reference. In this case, the output of the comparator BO−COMP ($V_{BO-COMP}$) is low (see Figure 22). Conversely, if V_{BO} goes below 1 V, $V_{BO-COMP}$ turns high and a 980 mV voltage source is connected to the BO pin to maintain the pin level near 1 V. The high state of $V_{BO-COMP}$ is used to detect a brown−out condition. However, the brown−out detection is not immediate. First, as soon as a high level occurs, this information is stored by a latch (L_{BO} of Figure 22) and a 50 ms delay is activated. No BO fault can be detected until this time has elapsed. The main goal of the 50 ms lag is to help meet the hold−up requirements. In case of a short mains interruption, no fault is detected and hence, the “pfcOK” signal remains high and does not disable the downstream converter. In addition, the BO pin voltage being kept at 980 mV, there is almost no extra delay between the line recovery and the occurrence of the steady state V_{BO} voltage, which otherwise would exist because of the large capacitor typically placed between pin7 and ground to filter the input voltage ripple. As a result, the NCP1632A effectively “blanks” any mains interruption that is shorter than 38 ms (minimum guaranteed value of the 50 ms timer).

At the end of this 50 ms blanking delay, another timer is activated that sets a 50 ms window during which a fault can be detected. This is the role of the second 50 ms timer of Figure 22:

- If the output of OPAMP is high at the end of the first delay (50 ms blanking time) and before the second 50 ms delay time is elapsed, a brown−out fault is detected (BO_NOK is high).
- If the output of OPAMP remains low for the duration of the second delay, no fault is detected.

In any case, the L_{BO} latch and the two delays are reset at the end of the second delay.

When the “BO_NOK” signal is high, the driver is disabled, the “$V_{control}$” pin is grounded to recover operation with a soft−start when the fault has gone and the “pfcOK”

voltage turns low to disable the downstream converter. In addition, both 50 ms timers are reset, the 980 mV clamp is removed (S_2 is off) and I_{BO}, the 7 μA current source, is enabled to lower the pin7 voltage for hysteresis purpose (as explained above).

A pnp transistor ensures that the BO pin voltage remains below the 1 V threshold until V_{CC} reaches $V_{CC(on)}$. This is to guarantee that the circuit starts operation in the right state, that is, "BONOK" high. When V_{CC} exceeds $V_{CC(on)}$, the pnp transistor turns off and the circuit enables the 7 μA current source. The 7 μA current source remains on until the BO pin voltage exceeds the 1 V BO threshold.

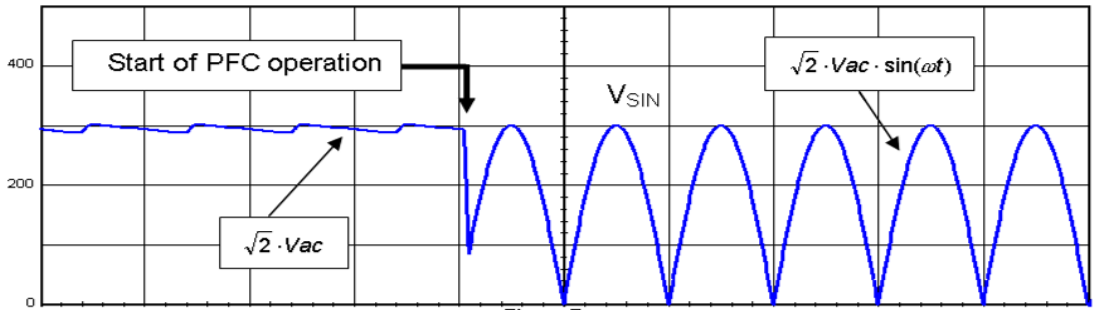


Figure 23. Typical Input Voltage of a PFC Stage

Thermal Shutdown (TSD)

An internal thermal circuitry disables the circuit gate drive and then keeps the power switch off when the junction temperature exceeds 140°C typically. The output stage is then enabled once the temperature drops below about 80°C (60°C hysteresis).

The temperature shutdown keeps active as long as the circuit is not reset, that is, as long as V_{CC} keeps higher than $V_{CC(reset)}$. The reset action forces the TSD threshold to be the upper one (140°C). This ensures that any cold start−up will be done with the right TSD level.

Under−Voltage Lockout Section

The NCP1632A incorporates an Under−Voltage Lockout block to prevent the circuit from operating when the power supply is not high enough to ensure a proper operation. An UVLO comparator monitors the pin 12 voltage (V_{CC}) to allow the NCP1632A operation when V_{CC} exceeds 12 V typically. The comparator incorporates some hysteresis (2.0 V typically) to prevent erratic operation as the V_{CC} crosses the threshold. When V_{CC} goes below the UVLO comparator lower threshold, the circuit turns off.

The circuit off state consumption is very low: < 50 μA.

This low consumption enables to use resistors to charge the V_{CC} capacitor during the start−up without the penalty of a too high dissipation.

Output Drive Section

The circuit embeds two drivers to control the two interleaved branches. Each output stage contains a totem pole optimized to minimize the cross conduction current during high frequency operation. The gate drive is kept in a sinking mode whenever the Under−Voltage Lockout (UVLO) is active or more generally whenever the circuit is off. Its high current capability (−500 mA/+800 mA) allows it to effectively drive high gate charge power MOSFET.

Reference Section

The circuit features an accurate internal reference voltage (V_{REF}). V_{REF} is optimized to be ± 2.4% accurate over the temperature range (the typical value is 2.5 V). V_{REF} is the voltage reference used for the regulation and the over−voltage protection. The circuit also incorporates a precise current reference (I_{REF}) that allows the Over−Current Limitation to feature a ± 6% accuracy over the temperature range.

Fault Mode

The following block details the function.

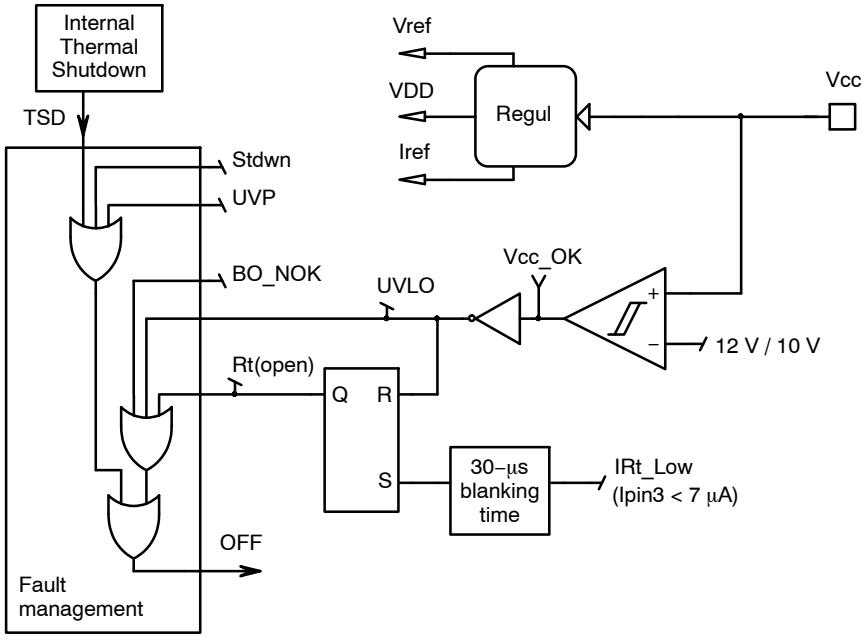


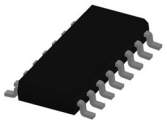
Figure 24. Fault Management Block

The circuit detects a fault if the R_t pin is open. Practically, if the pin sources less than 7 μA, the "I_{Rt_Low}" signal sets a latch that turns off the circuit if its output ($R_{t(open)}$) is high. A 30 μs blanking time avoids parasitic fault detections. The latch is reset when the circuit is in UVLO state (too low V_{CC} levels for proper operation).

When any of the following faults is detected:

- brown−out ("BO_NOK")
- Under−Voltage Protection ("UVP")
- Latch−off condition ("Stdwn")
- Die over−temperature ("TSD")
- Too low the current sourced by the R_t pin ("$R_{t(open)}$")
- "UVLO" (improper Vcc level for operation)

The circuit turns off. It recovers operation when the fault disappears.



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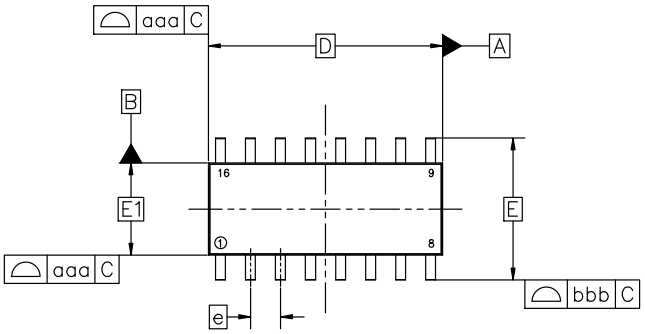
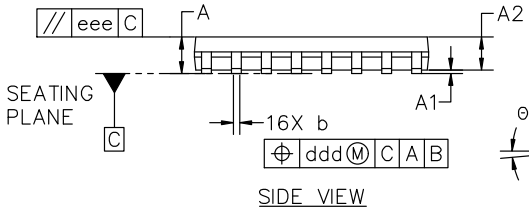
CASE 751B
ISSUE M

DATE 18 OCT 2024

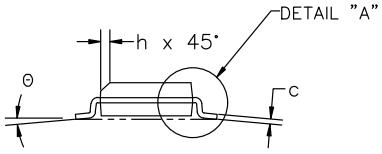
NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 2018.
2. DIMENSION IN MILLIMETERS. ANGLE IN DEGREES.
3. DIMENSIONS D AND E1 DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15mm PER SIDE.
5. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127mm TOTAL IN EXCESS OF THE b DIMENSION AT MAXIMUM MATERIAL CONDITION.



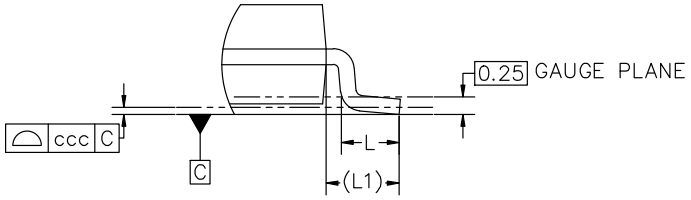
TOP VIEW



SIDE VIEW

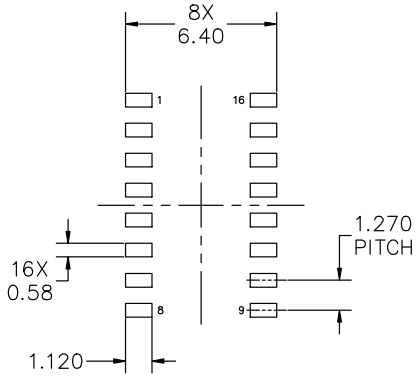


END VIEW



DETAIL "A"
Scale 3:1

MILLIMETERS			
DIM	MIN	NOM	MAX
A	1.35	1.55	1.75
A1	0.10	0.18	0.25
A2	1.25	1.37	1.50
b	0.35	0.42	0.49
c	0.19	0.22	0.25
D	9.90 BSC		
E	6.00 BSC		
E1	3.90 BSC		
e	1.27 BSC		
h	0.25	−−−	0.50
L	0.40	0.83	1.25
L1	1.05 REF		
Θ	0°	−−−	7°
TOLERANCE OF FORM AND POSITION			
aaa	0.10		
bbb	0.20		
ccc	0.10		
ddd	0.25		
eee	0.10		



RECOMMENDED MOUNTING FOOTPRINT

*FOR ADDITIONAL INFORMATION ON OUR PB−FREE STRATEGY AND SOLDERING DETAILS, PLEASE DOWNLOAD THE onsemi SOLDERING AND MOUNTING TECHNIQUES REFERENCE MANUAL, SOLDERRM/D

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DESCRIPTION:	**SOIC−16 9.90X3.90X1.37 1.27P**		**PAGE 1 OF 2**

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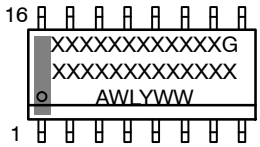
ISSUE M

DATE 18 OCT 2024

GENERIC MARKING DIAGRAM*



XXXXX = Specific Device Code
A = Assembly Location
WL = Wafer Lot
Y = Year
WW = Work Week
G = Pb−Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “▪”, may or may not be present. Some products may not follow the Generic Marking.

STYLE 1:

PIN	
1.	COLLECTOR
2.	BASE
3.	EMITTER
4.	NO CONNECTION
5.	EMITTER
6.	BASE
7.	COLLECTOR
8.	COLLECTOR
9.	BASE
10.	EMITTER
11.	NO CONNECTION
12.	EMITTER
13.	BASE
14.	COLLECTOR
15.	EMITTER
16.	COLLECTOR

STYLE 2:

PIN	
1.	CATHODE
2.	ANODE
3.	NO CONNECTION
4.	CATHODE
5.	CATHODE
6.	NO CONNECTION
7.	ANODE
8.	CATHODE
9.	CATHODE
10.	ANODE
11.	NO CONNECTION
12.	CATHODE
13.	CATHODE
14.	NO CONNECTION
15.	ANODE
16.	CATHODE

STYLE 3:

PIN	
1.	COLLECTOR, DYE #1
2.	BASE, #1
3.	EMITTER, #1
4.	COLLECTOR, #1
5.	COLLECTOR, #2
6.	BASE, #2
7.	EMITTER, #2
8.	COLLECTOR, #2
9.	COLLECTOR, #3
10.	BASE, #3
11.	EMITTER, #3
12.	COLLECTOR, #3
13.	COLLECTOR, #4
14.	BASE, #4
15.	EMITTER, #4
16.	COLLECTOR, #4

STYLE 4:

PIN	
1.	COLLECTOR, DYE #1
2.	COLLECTOR, #1
3.	COLLECTOR, #2
4.	COLLECTOR, #2
5.	COLLECTOR, #3
6.	COLLECTOR, #3
7.	COLLECTOR, #4
8.	COLLECTOR, #4
9.	BASE, #4
10.	EMITTER, #4
11.	BASE, #3
12.	EMITTER, #3
13.	BASE, #2
14.	EMITTER, #2
15.	BASE, #1
16.	EMITTER, #1

STYLE 5:

PIN	
1.	DRAIN, DYE #1
2.	DRAIN, #1
3.	DRAIN, #2
4.	DRAIN, #2
5.	DRAIN, #3
6.	DRAIN, #3
7.	DRAIN, #4
8.	DRAIN, #4
9.	GATE, #4
10.	SOURCE, #4
11.	GATE, #3
12.	SOURCE, #3
13.	GATE, #2
14.	SOURCE, #2
15.	GATE, #1
16.	SOURCE, #1

STYLE 6:

PIN	
1.	CATHODE
2.	CATHODE
3.	CATHODE
4.	CATHODE
5.	CATHODE
6.	CATHODE
7.	CATHODE
8.	CATHODE
9.	ANODE
10.	ANODE
11.	ANODE
12.	ANODE
13.	ANODE
14.	ANODE
15.	ANODE
16.	ANODE

STYLE 7:

PIN	
1.	SOURCE N-CH
2.	COMMON DRAIN (OUTPUT)
3.	COMMON DRAIN (OUTPUT)
4.	GATE P-CH
5.	COMMON DRAIN (OUTPUT)
6.	COMMON DRAIN (OUTPUT)
7.	COMMON DRAIN (OUTPUT)
8.	SOURCE P-CH
9.	SOURCE P-CH
10.	COMMON DRAIN (OUTPUT)
11.	COMMON DRAIN (OUTPUT)
12.	COMMON DRAIN (OUTPUT)
13.	GATE N-CH
14.	COMMON DRAIN (OUTPUT)
15.	COMMON DRAIN (OUTPUT)
16.	SOURCE N-CH

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