IS31FL3237

36-CHANNEL LED DRIVER WITH 16-BIT PWM

May 2026

GENERAL DESCRIPTION

The IS31FL3237 is an LED driver with 36 constant current channels. Each channel can be pulse width modulated (PWM) by 16 bits for smooth LED brightness control. In addition, each channel has an 8-bit output current control register which allows fine tuning the current for rich RGB color mixing, e.g., a pure white color LED application. The maximum output current of each channel is 38mA, which can be adjusted by one 8-bit global control register.

Proprietary programmable technology is used to minimize audible noise caused by MLCC decoupling capacitors. All registers can be programmed via a high speed I2C (1MHz).

The IS31FL3237 can be shut down with minimum current consumption by either pulling the SDB pin low or by using the software shutdown feature.

The IS31FL3237 is available in QFN-44 (5mm×5mm) package. It operates from 2.7V to 5.5V over the temperature range of -40°C to +125°C.

FEATURES

- 2.7V to 5.5V VCC supply
- Pin to pin with IS31FL3236/IS31FL3236A (QFN-44, 5mm×5mm)
- 1MHz I2C interface, automatic address increment function with readout function
- Four selectable I2C addresses
- Accurate color rendition
  - Selectable 8-bit/10-bit/12-bit/16-bit PWM
  - 8-bit dot correction
  - 8-bit global current adjust
- Open/Short detect function
- 62kHz PWM frequency (8-bit PWM)
- Temperature detect function
- EMI Reduction Technology
  - Spread spectrum
  - Selectable Phase Delay
  - Selectable 180 degree Clock Phase
- -40°C to +125°C temperature range
- QFN-44 (5mm×5mm) package
- RoHS & Halogen-Free Compliance
- TSCA Compliance

APPLICATIONS

- AI-speakers and smart home devices
- LED in home appliances
- LED display for hand-held devices

TYPICAL APPLICATION CIRCUIT

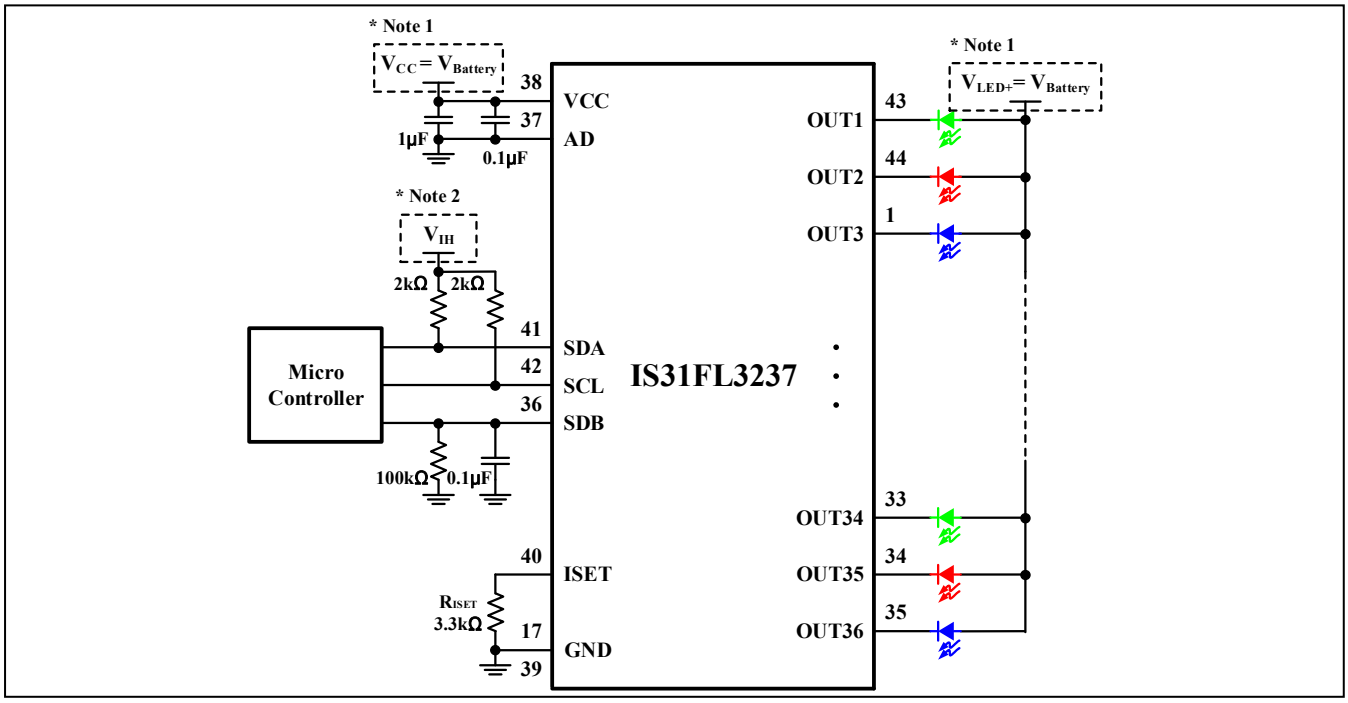


Figure 1 Typical Application Circuit

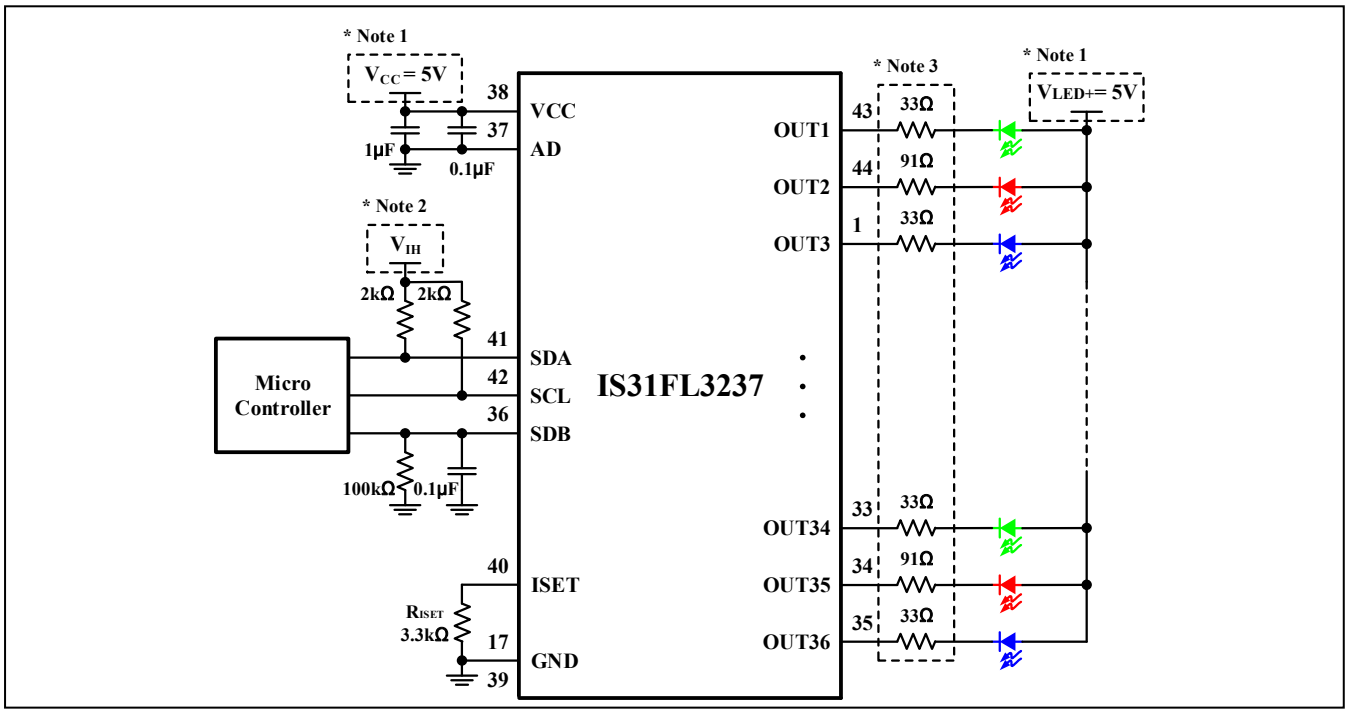


Figure 2 Typical Application Circuit (V_{CC}=5V)

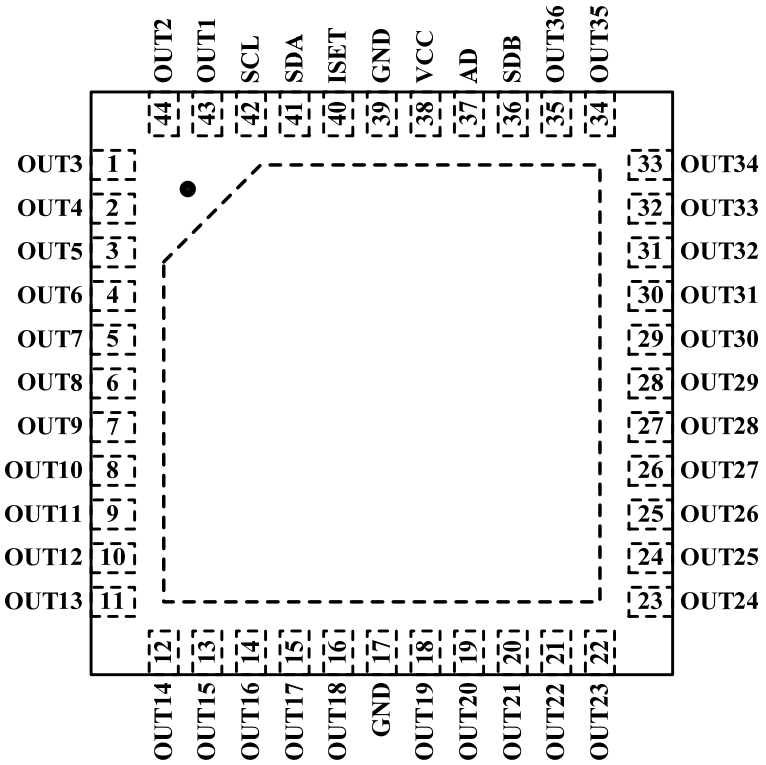
Note 1: V_{LED+} can be higher than VCC voltage, for example, V_{LED}+=5V, V_{CC}=3.3V.

Note 2: V_{IH} is the high level voltage for IS31FL3237, which is usually same as V_{CC} of Micro Controller, e.g. if V_{CC} of Micro Controller is 3.3V, V_{IH}= 3.3V. If V_{CC}= 5V and V_{IH} is lower than 2.8V, recommend to add a level shift circuit.

Note 3: These optional resistors are for offloading the thermal dissipation ($P=I^2R$) away from the IS31FL3237.

Note 4: The output current is set up to 23mA when R_{ISET}= 3.3kΩ. The maximum global output current can be set by external resistor, R_{ISET}. Please refer to the detail application information in R_{ISET} section.

PIN CONFIGURATION

Package	Pin Configuration (Top View)
QFN-44	

PIN DESCRIPTION

No.	Pin	Description
1~16	OUT3 ~ OUT18	Output channel 3~18 for LEDs.
17, 39	GND	Ground.
18~35	OUT19 ~ OUT36	Output channel 19~36 for LEDs.
36	SDB	Shutdown the chip when pulled low.
37	AD	I2C address setting.
38	VCC	Power supply.
40	ISET	Input terminal used to connect an external resistor. This regulates the global output current. When R_{ISET}=3.3kΩ, I_{OUT}=23mA.
41	SDA	I2C serial data.
42	SCL	I2C serial clock.
43,44	OUT1, OUT2	Output channel 1, 2 for LEDs.
	Thermal Pad	Need to connect to GND.

ORDERING INFORMATION

Industrial Range: -40°C to +125°C

Order Part No.	Package	QTY/Reel
IS31FL3237-QFLS4-TR	QFN-44, Lead-free	2500

ABSOLUTE MAXIMUM RATINGS

Supply voltage V_{CC}, OUT1 to OUT36	-0.3V ~ +6.0V
Voltage at SCL, SDA, SDB, AD	-0.3V ~ V_{CC}+0.3V
Maximum junction temperature, T_{JMAX}	+150°C
Storage temperature range, T_{STG}	-65°C ~ +150°C
Operating temperature range, T_A=T_J	-40°C ~ +125°C
Package thermal resistance, junction to ambient (4-layer standard test PCB based on JESD 51-2A), θ_{JA}	32.6°C/W
ESD (HBM) ESD (CDM)	±8kV ±750V

Note 5: Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other condition beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

Typical values are T_A = 25°C, V_{CC} = 5V.

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
V_{CC}	Supply voltage		2.7		5.5	V
I_{OUT}	Maximum output current	V_{OUT}= 0.8V, R_{ISET}= 2kΩ, GCC= 0xFF, Scaling= 0xFF (Note 6)		38		mA
	Output current	V_{OUT}= 0.6V, R_{ISET}= 3.3kΩ, GCC= 0xFF, Scaling= 0xFF	21.39	23	24.61	mA
ΔI_{MAT}	Channel mismatch	R_{ISET}= 3.3kΩ, GCC= 0xFF, Scaling= 0xFF, I_{OUT}= 23mA	-7		7	%
V_{HR}	Headroom voltage	R_{ISET}= 3.3kΩ, GCC= 0xFF, Scaling= 0xFF, I_{OUT}= 23mA		0.3	0.5	V
I_{CC}	Quiescent power supply current	R_{ISET}= 3.3kΩ, GCC= 0xFF, Scaling= 0xFF, I_{OUT}= 23mA, PWM= 0x00, V_{CC}=3.6V		4.7	7	mA
		R_{ISET}= 3.3kΩ, GCC= 0xFF, Scaling= 0xFF, I_{OUT}= 23mA, PWM= 0x00, V_{CC}=5V		5.7	8	mA
I_{SD}	Shutdown current	R_{ISET}= 3.3kΩ, V_{SDB}= 0V or software shutdown, V_{CC}= 3.6V		0.8	1.6	μA
		R_{ISET}= 3.3kΩ, V_{SDB}= 0V or software shutdown, V_{CC}= 5V		1.8	3	μA
f_{OUT}	PWM frequency of output	OSC= 8MHz, PWM Resolution= 8bit		31.5		kHz
T_{SD}	Thermal shutdown	(Note 7)		165		°C
T_{SD_HY}	Thermal shutdown hysteresis	(Note 7)		20		°C
V_{OD}	OUTx pin open detect threshold	V_{CC}=5V, R_{ISET}=6.8kΩ, I_{OUT}≥0.1mA, measured at OUTx	0.08	0.18	0.26	V
V_{SD}	LED short detect threshold	V_{CC}=5V, R_{ISET}=6.8kΩ, I_{OUT}≥0.1mA, measured at (V_{CC}-V_{OUTx})	0.7	1.3	1.5	V
Logic Electrical Characteristics (SDA, SCL, SDB, AD)						
V_{IL}	Logic "0" input voltage	V_{CC}= 2.7V~5.5V			0.4	V
V_{IH}	Logic "1" input voltage	V_{CC}= 2.7V~5.5V	1.4			V
I_{IL}	Logic "0" input current	V_{INPUT}= 0V (Note 7)		5		nA
I_{IH}	Logic "1" input current	V_{INPUT}= V_{CC} (Note 7)		5		nA

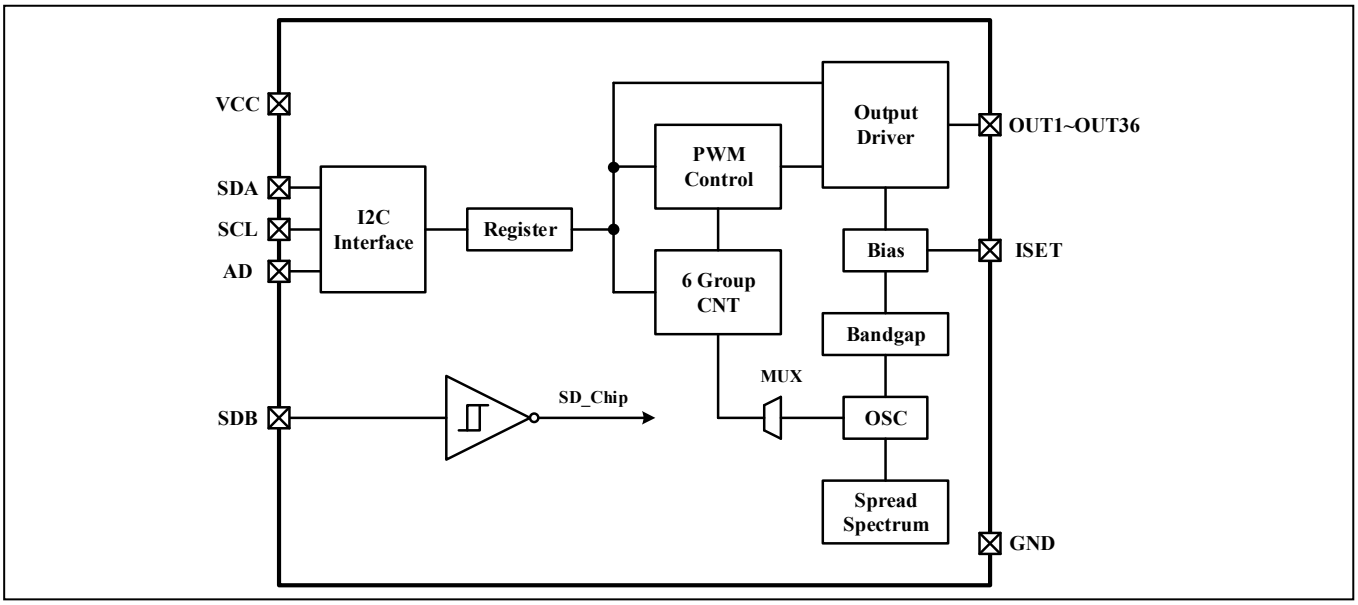
DIGITAL INPUT SWITCHING CHARACTERISTICS (NOTE 7)

Symbol	Parameter	Fast Mode			Fast Mode Plus			Units
		Min.	Typ.	Max.	Min.	Typ.	Max.	
f_{SCL}	Serial-clock frequency	-		400	-		1000	kHz
t_{BUF}	Bus free time between a STOP and a START condition	1.3		-	0.5		-	μs
$t_{HD, STA}$	Hold time (repeated) START condition	0.6		-	0.26		-	μs
$t_{SU, STA}$	Repeated START condition setup time	0.6		-	0.26		-	μs
$t_{SU, STO}$	STOP condition setup time	0.6		-	0.26		-	μs
$t_{HD, DAT}$	Data hold time	-		-	-		-	μs
$t_{SU, DAT}$	Data setup time	100		-	50		-	ns
t_{LOW}	SCL clock low period	1.3		-	0.5		-	μs
t_{HIGH}	SCL clock high period	0.7		-	0.26		-	μs
t_R	Rise time of both SDA and SCL signals, receiving	-		300	-		120	ns
t_F	Fall time of both SDA and SCL signals, receiving	-		300	-		120	ns

Note 6: The recommended minimum value of R_{ISET} is 2kΩ.

Note 7: Guaranteed by design.

FUNCTIONAL BLOCK DIAGRAM



DETAILED DESCRIPTION

I2C INTERFACE

The IS31FL3237 uses a serial bus, which conforms to the I2C protocol, to control the chip's functions with two wires: SCL and SDA. The IS31FL3237 has a 7-bit slave address (A7:A1), followed by the R/W bit, A0. Set A0 to "0" for a write command and set A0 to "1" for a read command. The value of bits A1 and A2 are decided by the connection of the AD pin. The complete slave address is:

Table 1 Slave Address (Write Only):

Bit	A7:A3	A2:A1	A0
Value	01101	AD	0

AD connected to GND, AD = 00;
AD connected to VCC, AD = 11;
AD connected to SCL, AD = 01;
AD connected to SDA, AD = 10;

The SCL line is uni-directional. The SDA line is bi-directional (open-drain) with a pull-up resistor (typically 2kΩ). The maximum clock frequency specified by the I2C standard is 1MHz. In this discussion, the master is the microcontroller and the slave is the IS31FL3237.

The timing diagram for the I2C is shown in Figure 3. The SDA is latched in on the stable high level of the SCL. When there is no interface activity, the SDA line should be held high.

The "START" signal is generated by lowering the SDA signal while the SCL signal is high. The start signal will alert all devices attached to the I2C bus to check the incoming address against their own chip address.

The 8-bit chip address is sent next, most significant bit first. Each address bit must be stable while the SCL level is high.

After the last bit of the chip address is sent, the master checks for the IS31FL3237's acknowledge. The master releases the SDA line high (through a pull-up resistor). Then the master sends an SCL pulse. If the IS31FL3237 has received the address correctly, then it holds the SDA line low during the SCL pulse. If the SDA line is not low, then the master should send a "STOP" signal (discussed later) and abort the transfer.

Following acknowledge of IS31FL3237, the register address byte is sent, most significant bit first. IS31FL3237 must generate another acknowledge indicating that the register address has been received.

Then 8-bit of data byte are sent next, most significant bit first. Each data bit should be valid while the SCL level is stable high. After the data byte is sent, the IS31FL3237 must generate another acknowledge to indicate that the data was received.

The "STOP" signal ends the transfer. To signal "STOP", the SDA signal goes high while the SCL signal is high.

ADDRESS AUTO INCREMENT

To write multiple bytes of data into IS31FL3237, load the address of the data register that the first data byte is intended for. During the IS31FL3237 acknowledge of receiving the data byte, the internal address pointer will increment by one. The next data byte sent to IS31FL3237 will be placed in the new address, and so on. The auto increment of the address will continue as long as data continues to be written to IS31FL3237 (Figure 6).

READING OPERATION

Most of the registers can be read.

To read the register, after I2C start condition, the bus master must send the IS31FL3237 device address with the R/ bit set to "0", followed by the register address which determines which register is accessed. Then restart I2C, the bus master should send the IS31FL3237 device address with the R/ bit set to "1". Data from the register defined by the command byte is then sent from the IS31FL3237 to the master (Figure 7).

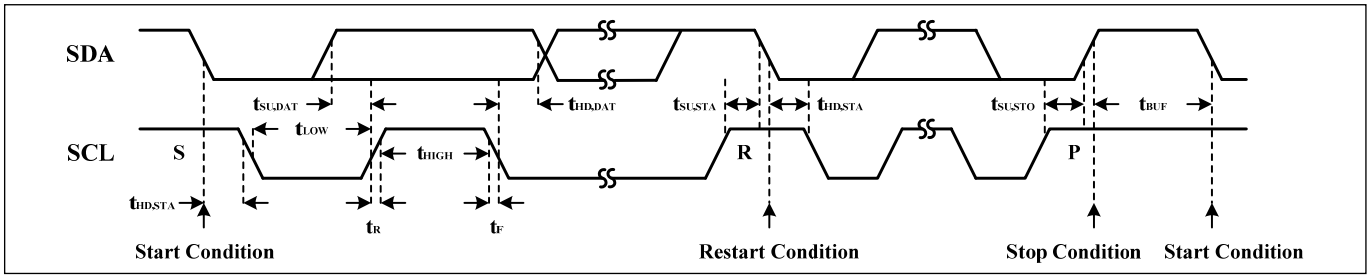


Figure 3 Interface Timing

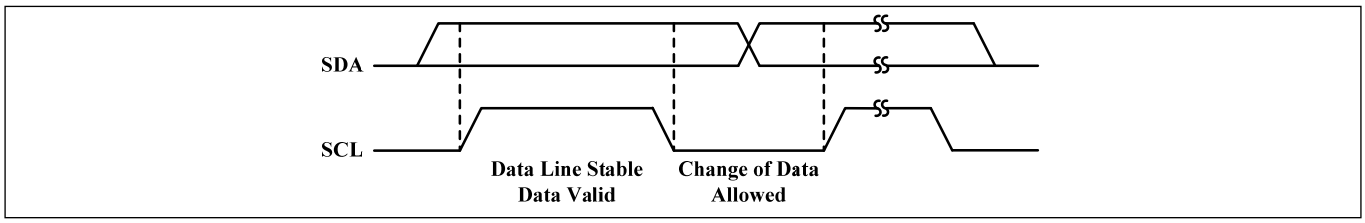


Figure 4 Bit Transfer

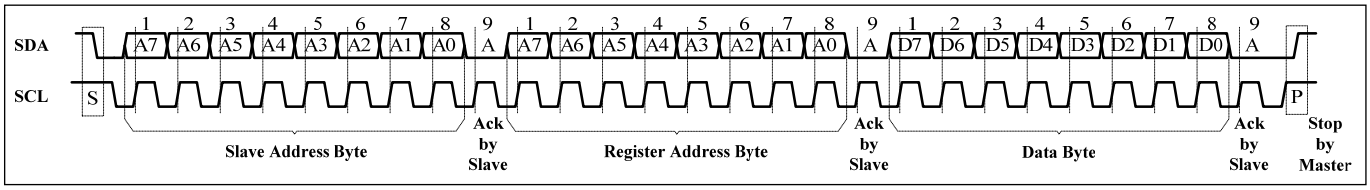


Figure 5 Writing to IS31FL3237 (Typical)

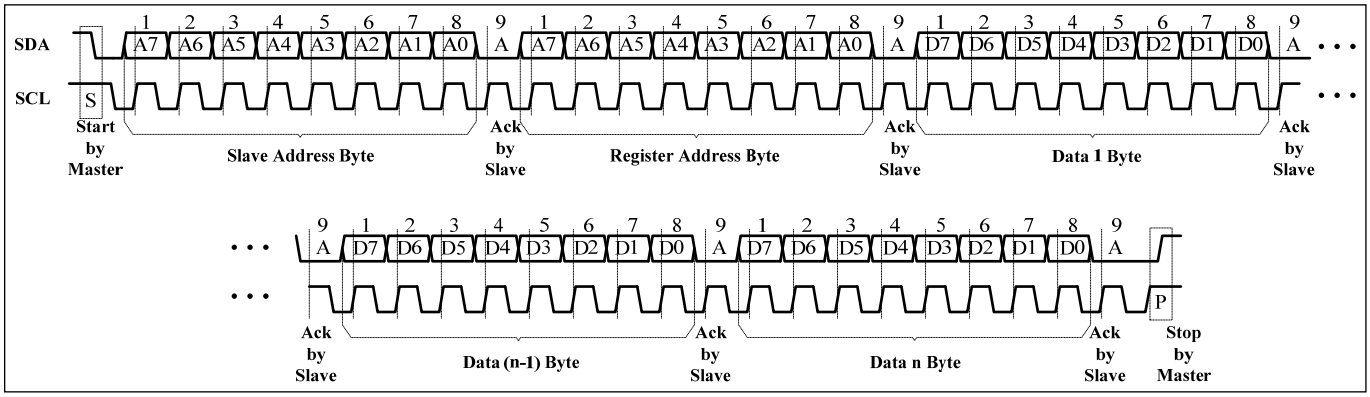


Figure 6 Writing to IS31FL3237 (Automatic Address Increment)

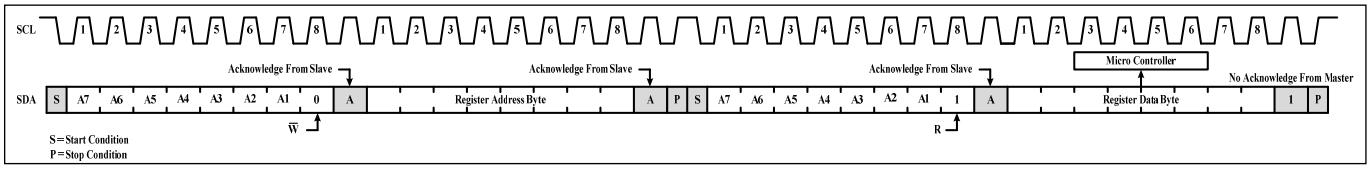


Figure 7 Reading from IS31FL3237

REGISTER DEFINITIONS

Table 2 Register Function

Address	Name	Function	R/W	Table	Default
00h	Control Register	Power control register	R/W	3	0000 0000
01h~48h	PWM Register	Channel [36:1] PWM register byte	R/W	5	
49h	Update Register	Update the PWM data	W	-	
4Ah~6Dh	LED Scaling Register	Control each channel's DC current	R/W	7	
6Eh	Global Current Control Register	Control Global DC current/SSD	R/W	8	
70h	Phase Delay and Clock Phase Register	Phase Delay and Clock Phase	R/W	9	
71h	Open Short Detect Enable Register	Open short detect enable	R/W	10	
72h~76h	LED Open/Short Register	Open short information	R/W	11	
77h	Temperature Sensor Register	Temperature information	R/W	12	
78h	Spread Spectrum Register	Spread spectrum control register	R/W	13	
7Fh	Reset Register	Reset all registers	W	-	

Table 3 00h Control Register

Bit	D7	D6:D4	D3	D2:D1	D0
Name	-	OSC	-	PMS	SSD
Default	0	000	0	00	0

The Control Register sets software shutdown mode, internal oscillator clock frequency and PWM resolution. The internal oscillator clock frequency and the PWM resolution will decide the output PWM frequency. Recommend selecting PWM frequency lower than 300Hz or higher than 20kHz to avoid MLCC audible noise as shown in Table 4.

SSD Software Shutdown Enable
0 Software shutdown mode
1 Normal operation

PMS PWM Resolution
00 N=256, 8-bit
01 N=1024, 10-bit
10 N=4096, 12-bit
11 N=65536, 16-bit

OSC Oscillator Clock Frequency Selection
000 16MHz
001 8MHz
010 1MHz
011 500kHz
100 250kHz
101 125kHz
110 62kHz
111 31kHz

Table 4 PWM Frequency

PWM Resolution	16M	8M	1M	500k	250k	125k	62k	31k
8-bit	62k	32k	4k	2k	1k	0.5k	244	122
10-bit	16k	8k	1k	0.5k	244	122	NA	NA
12-bit	4k	2k	244	122	NA	NA	NA	NA
16-bit	244	122	NA	NA	NA	NA	NA	NA

Table 5 01h~48h PWM Register

Reg	02h (04h, 06h…)	01h (03h, 05h…)
Bit	D7:D0	D7:D0
Name	PWM_H	PWM_L
Default	0000 0000	0000 0000

Each output has 2 bytes to modulate the PWM duty in 256/1024/4096/65536 steps. If using 8 bits PWM resolution, only PWM_L bits need to be set.

The value of the SL (Scaling Register) decides the peak current of each LED noted as I_{OUT}.

I_{OUT} and the value of the PWM Registers decide the average current of each LED noted as I_{LED}.

I_{OUT} is computed by Formula (1):

$$I_{OUT} = I_{OUT\,(MAX)} \times \frac{GCC}{256} \times \frac{SL}{256} \qquad (1)$$

I_{LED} computed by Formula (2):

$$I_{LED} = \frac{PWM}{N} \times I_{OUT} \qquad (2)$$

N=256: $PWM = \sum_{n=0}^{7} D[n] \cdot 2^n$

N=1024: $PWM = \sum_{n=0}^{9} D[n] \cdot 2^n$

N=4096: $PWM = \sum_{n=0}^{11} D[n] \cdot 2^n$

N=65536: $PWM = \sum_{n=0}^{15} D[n] \cdot 2^n$ (3)

Where $I_{OUT(MAX)}$ is the maximum output current decided by R_{ISET} (Check R_{ISET} section for more information), GCC is the global current setting (6Eh), and SL is the scaling of each output (4Ah~6Dh), N=256/1024/4096/65536(8/10/12/16 bits PWM resolution).

For example: R_{ISET}=3.3kΩ, GCC=0xFF, SL=0xFF, PMS= "11" (16-bit PWM resolution), PWM_H=0xFF, PWM_L=0xFF, $I_{OUT(MAX)}$= 23.18mA.

$$I_{OUT} = I_{OUT(MAX)} \times \frac{255}{256} \times \frac{255}{256} = 23\,mA \quad (1)$$

$$PWM = \sum_{n=0}^{15} D[n] \cdot 2^n = 65535 \quad (3)$$

N= 65536

$$I_{LED} = \frac{65535}{65536} \times 23\,mA = 23\,mA \quad (2)$$

Where $I_{OUT(MAX)}$ is the maximum output current decided by R_{ISET} (Check R_{ISET} section for more information)

The I_{OUT} of each channel is set by the SL bits of LED Scaling Register (4Ah~6Dh). Please refer to the detail information in Table 7.

If R_{ISET}=3.3kΩ, GCC=0xFF, SL=0xFF, PMS= "00" (8-bit PWM resolution, only use the PWM_L, the PWM_H will be ignored), PWM_H=0x77, PWM_L=0xAA, $I_{OUT(MAX)}$ = 23.18mA

$$I_{OUT} = I_{OUT(MAX)} \times \frac{255}{256} \times \frac{255}{256} = 23\,mA \quad (1)$$

$$PWM = \sum_{n=0}^{7} D[n] \cdot 2^n = 170 \quad (3)$$

N= 256

$$I_{LED} = \frac{170}{256} \times 23\,mA \quad (2)$$

Table 6 PWM and Scaling Register Map

OUT	PWM		SL
	PWM_H	PWM_L	
1	02h	01h	4Ah
2	04h	03h	4Bh
3	06h	05h	4Ch
4	08h	07h	4Dh
5	0Ah	09h	4Eh
6	0Ch	0Bh	4Fh
7	0Eh	0Dh	50h
8	10h	0Fh	51h
9	12h	11h	52h
10	14h	13h	53h
11	16h	15h	54h
12	18h	17h	55h
13	1Ah	19h	56h
14	1Ch	1Bh	57h
15	1Eh	1Dh	58h
16	20h	1Fh	59h
17	22h	21h	5Ah
18	24h	23h	5Bh
19	26h	25h	5Ch
20	28h	27h	5Dh
21	2Ah	29h	5Eh
22	2Ch	2Bh	5Fh
23	2Eh	2Dh	60h
24	30h	2Fh	61h
25	32h	31h	62h
26	34h	33h	63h
27	36h	35h	64h
28	38h	37h	65h
29	3Ah	39h	66h
30	3Ch	3Bh	67h
31	3Eh	3Dh	68h
32	40h	3Fh	69h
33	42h	41h	6Ah
34	44h	43h	6Bh
35	46h	45h	6Ch
36	48h	47h	6Dh

49h Update Register

When SDB= “H” and SSD= “1”, a writing of “0000 0000” to 49h will update the PWM register (01h~48h) values.

Table 7 4Ah~6Dh LED Scaling Register

Bit	D7:D0
Name	SL
Default	0000 0000

Each output has 8 bits to modulate DC current in 256 steps.

The value of the SL Registers decides the DC peak current of each LED noted by I_{OUT}.

I_{OUT} is computed by Formula (1):

$$I_{OUT} = I_{OUT(MAX)} \times \frac{GCC}{256} \times \frac{SL}{256} \qquad (1)$$

$$SL = \sum_{n=0}^{7} D[n] \cdot 2^n \qquad (4)$$

Where $I_{OUT(MAX)}$ is the maximum output current decided by R_{ISET}, GCC is the global current setting (6Eh).

4Ah~6Dh don’t need to be updated by writing to 49h, each register will be updated immediately when it is written.

Table 8 6Eh Global Current Control Register

Bit	D7:D0
Name	GCC
Default	0000 0000

GCC and SL registers control I_{OUT} as shown in Formula (1).

$$GCC = \sum_{n=0}^{7} D[n] \cdot 2^n \qquad (5)$$

If GCC=0xFF, SL=0xFF, $I_{OUT}=I_{OUT(MAX)}$

If GCC=0x01, SL=0xFF,

$$I_{OUT} = I_{OUT(MAX)} \times \frac{1}{256} \times \frac{255}{256}$$

Where $I_{OUT(MAX)}$ is the maximum output current decided by R_{ISET} (Check R_{ISET} section for more information).

Table 9 70h Phase Delay and Clock Phase Register

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	PDE	-	PS6	PS5	PS4	PS3	PS2	PS1
Default	0	0	0	0	0	0	0	0

The PDE bit is for enabling channel group delay to minimize peak load current draw from the LED power supply rail.

PDE	Phase Delay Enable
0	Phase delay disable
1	Phase delay enable

PS[n]	Clock Phase Select
0	All outputs work as scheme of Clock Phase 1
1	Outputs OUT[2+(n-1)×6], OUT[4+(n-1)×6], OUT[6+(n-1)×6] work as scheme of Clock Phase 2

Phase Delay separates 36 outputs as 6 groups, OUT1~OUT6 as group 1, OUT7~OUT12 as group 2…OUT31~OUT36 as group 6. When Phase Delay is enabled, group 2 has a $1/(6\times f_{OUT})$ time delay than group 1, group 3 also has a $1/(6\times f_{OUT})$ time delay than group 2, group 4 also has a $1/(6\times f_{OUT})$ time delay than group 3, and so on.

For each group of 6 outputs there is a Clock Phase option PS[n](n=1~6), when PSn is set to “1”, OUT[1+(n-1)×6], OUT[3+(n-1)×6], OUT[5+(n-1)×6] keep the phase, phase 1, the turning on edge of the PWM pulse is fixed from starting of PWM cycle, but OUT[2+(n-1)×6], OUT[4+(n-1)×6], OUT[6+(n-1)×6] change to phase 2, the turning off edge of the PWM pulse is fixed from ending of PWM cycle as below, the rising and falling edges will cancel the power ripple.

Phase Delay feature and Clock Phase options can work together to minimize the voltage ripple of LED power supply.

Table 10 71h Open Short Detect Enable Register

Bit	D7:D2	D1:D0
Name	-	OSDE
Default	0000 00	00

OSDE enables the open and/or short LED channel detection with the result stored in 72h~76h, note either open or short information is saved not both.

OSDE	Open/Short Detect Enable
00	Detect disable
01	Detect disable
10	Short detect enable
11	Open detect enable

Table 11-1 72h~75h LED Open/Short Register

72h	D7:D0
Name	OP/ST[8:1]
Default	0000 0000

Table 11-2 76h LED Open/Short Register

Bit	D7:D4	D3:D0
Name	-	OP/ST[36:33]
Default	0000	0000

Open or short status is stored in 72h to 76h.

OP[36:1] Open Information of OUT36:OUT1
0 Open not detected
1 Open detected

ST[36:1] Short Information of OUT36:OUT1
0 Short not detected
1 Short detected

Table 12 77h Temperature Sensor Register

Bit	D7:D6	D5	D4	D3:D2	D1:D0
Name	TROF	-	T_Flag	-	TS
Default	00	0	0	00	00

TS stores the temperature/thermal roll-off point. TROF stores percentage of output current of the thermal roll-off function.

T_Flag=1 indicates die temperature exceeds the temperature set point (TS). Before each reading of 77h register, TROF and TS must be re-written.

TROF Thermal roll off percentage of output current
00 100%
01 75%
10 55%
11 30%

TS Temperature Point, Thermal roll off start point
00 140°C
01 120°C
10 100°C
11 90°C

T_Flag Temperature Flag
0 Temperature point not exceeded
1 Temperature point exceeded

Table 13 78h Spread Spectrum Register

Bit	D7:D5	D4	D3:D2	D1:D0
Name	DCPWM	SSP	RNG	CLT
Default	000	0	00	00

When DCPWM is set to “0”, the PWM outputs are decided by 01h~48h, and the PWM range is 0/256~255/256(8-bit PWM, 0/1024~1023/1024 for 10 bit PWM, 0/4096~4095/4096 for 12 bit PWM, 0/65536~65535/65536 for 16 bit PWM), still the 1/256(8-bit PWM, 1/1024 for 10 bit PWM, 1/4096 for 12 bit PWM, 1/65536 for 16 bit PWM), can’t be turned on. When the DCPWM is set to “1”, PWM dimming is disabled and dimming will be done by current adjust GCC and SL registers.

Spread spectrum register configures the spread spectrum function, adjust the cycle time and range.

DCPWM Setting the output to work in DC mode
xx0 Output 1~12 PWM data set by registers 01h~18h
xx1 Output 1~12 set to turn on (PWM is disabled)
x0x Output 13~24 PWM data set by registers 19h~30h
x1x Output 13~24 set to turn on (PWM is disabled)
0xx Output 25~36 PWM data set by registers 31h~48h
1xx Output 25~36 set to turn on (PWM is disabled)

SSP Spread Spectrum Enable
0 Disable
1 Enable

CLT Spread Spectrum Cycle Time
00 1980μs
01 1200μs
10 820μs
11 660μs

RNG Spread Spectrum Range
00 ±5%
01 ±15%
10 ±24%
11 ±34%

7Fh Reset Register

When power on, all registers values are reset to 0x00 (default). A write of “0000 0000” to 7Fh will also reset all registers to their default values.

APPLICATION INFORMATION

R_{ISET}

The maximum output current $I_{OUT(MAX)}$ for OUT1~OUT36 can be adjusted by the external resistor, R_{ISET}, as described in Formula (6).

$$I_{OUT\,(MAX)} = x \cdot \frac{V_{ISET}}{R_{ISET}} \qquad (6)$$

x = 58.84, V_{ISET} = 1.3V.

The recommended minimum value of R_{ISET} is 2kΩ.

When R_{ISET}=3.3kΩ, $I_{OUT(MAX)}$=23.18mA

When R_{ISET}=2kΩ, $I_{OUT(MAX)}$=38.25mA

R_{ISET} should be close to the chip and the ground side should well connect to the GND plane.

CURRENT SETTING

The maximum output current is set by the external resistor R_{ISET}. The Global Current Control register GCC can be used to set a lower current than set by R_{ISET}. The 8-bit SL registers (4Ah~6Dh) control the individual currents for each of the outputs.

Some applications may require the IOUT of each channel to be adjusted independently. For example, if OUT1 drives 1 LED and OUT2 drives 2 parallel LEDs, and they should have the same average current like 18mA, we can set the $I_{OUT(MAX)}$ to 36mA, and GCC=0xFF, 4Ah=0x80 for OUT1, 4Bh=0xFF for OUT2. The result is OUT1 will sink 18mA and OUT2 will sink 36mA which will be 18mA through each of the parallel LEDs.

Another example, OUT1, OUT2 and OUT3 drive an RGB LED, OUT1 is Red LED, OUT2 is Green LED and OUT 3 is Blue LED. If GCC and SL bits are the same, then the RGB LED may appear a pinkish, or not so white. The SL bits can be used to adjust the IOUTx current so the RGB LED appears closer to a pure white color. We call this SL bit adjustment by another name: white balance registers.

PWM CONTROL

The PWM Registers (01h~48h) can modulate the LED brightness of each of the 36 channels with 256/1024/4096/65536 steps. For example, if the data in PWM_H Register is “0000 0000” and in PWM_L Register is “0000 0100”, then the PWM is the fourth step. The greater the step count, the more accurate the RGB color mixing.

Writing new data continuously to the registers can modulate the brightness of the LEDs to achieve a breathing effect.

PWM FREQUENCY SELECT

The IS31FL3237 output channels operate with a default 8 bits PWM resolution and the PWM frequency of 62kHz (oscillator frequency is 16MHz). Because all the OUTx channels are synchronized, the DC power supply will experience large instantaneous current surges when the OUTx channels turn ON. These current surges will generate an AC ripple on the power supply which cause stress to the decoupling capacitors. When the AC ripple is applied to a monolithic ceramic capacitor chip (MLCC) it will expand and contract causing the PCB to flex and generate audible hum in the range of between 20Hz to 20kHz, to avoid this hum, there are many countermeasures, such as selecting the capacitor type and value which will not cause the PCB to flex and contract.

An additional option for avoiding audible hum is to set the IS31FL3237’s output PWM frequency above the audible frequency range. The Control Register (00h) can be used to set the switching frequency to 122Hz~62kHz as shown in Table 4. Combination settings of the OSC and PMS bits will result in different PWM frequency, select a value higher than 20kHz to avoid the audible frequency range.

PHASE DELAY and CLOCK PHASE

To reduce audible noise due to PWM switching, the IS31FL3237 features Phase Delay and Clock Phase schemes. When Phase Delay and Clock Phase are disabled (default) all of the outputs turn on simultaneously causing large current draw from the ceramic capacitors and pausible audible noise.

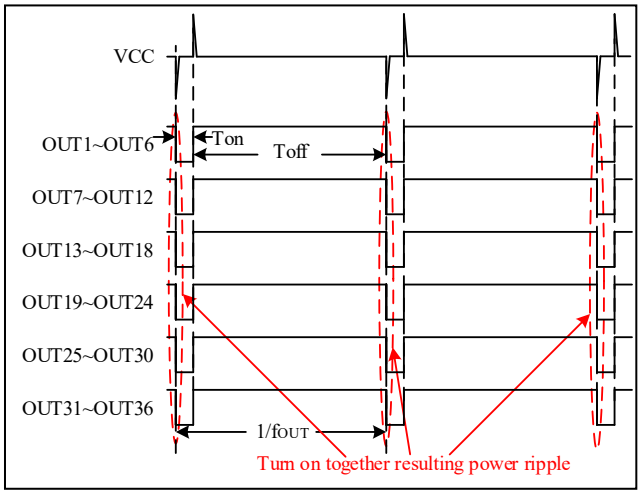


Figure 8 Phase Delay and Clock Phase disable

The PDE bit of register 70h will enable the Phase Delay function so at power-on the OUTx channel will not all turn on at the same time to minimize peak load current, resulting in reduced voltage ripple on the LED power supply rail. Phase Delay separates the 36 outputs as 6 groups, OUT1~OUT6 as group 1, OUT7~OUT12 as group 2…OUT31~OUT36 as group 6, when Phase Delay is enabled, group 2 will have a 1/(6×f_{OUT}) time delay than group 1, group 3 will also have a 1/(6×f_{OUT}) time delay than group 2, and so on.

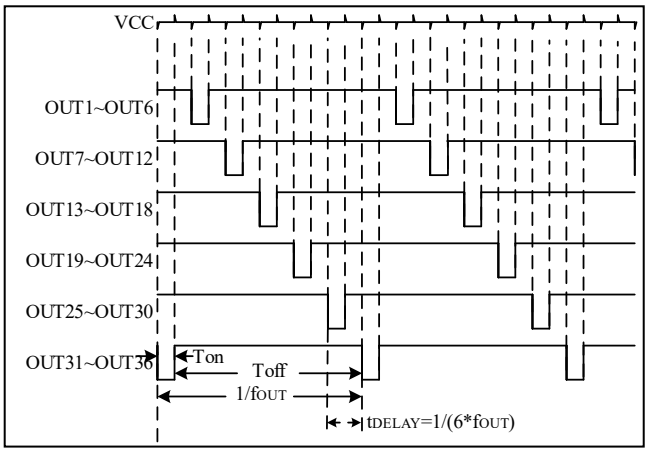


Figure 9 PDE= "1" Phase Delay Enable

Also in each group of outputs, there is a Clock Phase option PS[n](n=1~6), when PSn of 71h register is set to "0" (default), all outputs in group n keep the phase 1.

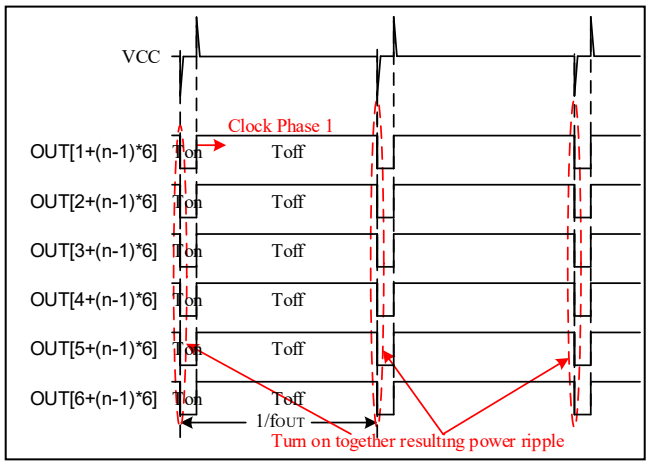


Figure 10 PSn= "0" Clock Phase disable

When PSn is set to "1", OUT[1+(n-1)×6], OUT[3+(n-1)×6], OUT[5+(n-1)×6] will keep the phase 1, the turning on edge of the PWM pulse is fixed from starting of PWM cycle as below, but OUT[2+(n-1)×6], OUT[4+(n-1)×6], OUT[6+(n-1)×6] will change to phase 2, the turning off edge of the PWM pulse is fixed from ending of PWM cycle as below, the rising and falling edges will cancel the power ripple.

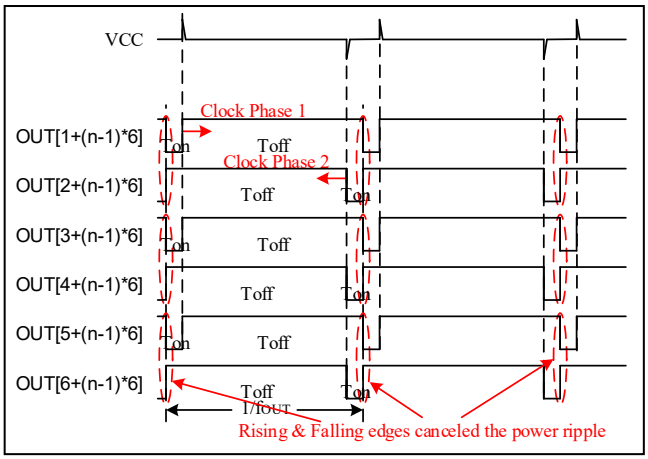


Figure 11 PSn= "1" Clock Phase enable

Phase Delay feature and Clock Phase options can work together to minimize the voltage ripple of LED power supply.

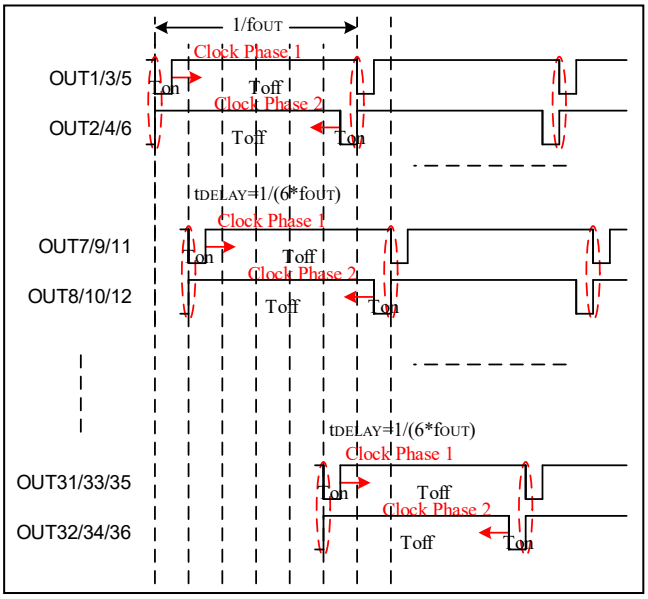


Figure 12 PDE= "1" Phase Delay enable, PSn= "1" (n=1~6) Clock Phase Enable

OPEN/SHORT DETECT FUNCTION

IS31FL3237 has open and short detect bit for each LED. See Open (VOD) and Short (VSD) detection thresholds in the Electrical Characteristics table.

By setting the OSDE bit of Open Short Detect Enable Register (71h) from "00" to "10" (store short information) or "11" (store open information), the LED Open/Short Register will store the open/short information immediately the MCU can get the open/short information by reading the 72h~76h.

SPREAD SPECTRUM FUNCTION

PWM current switching of LED outputs can be particularly troublesome when the EMI is concerned. To optimize the EMI performance, the IS31FL3237 includes a spread spectrum function. By setting the RNG bit of Spread Spectrum Register (78h), Spread Spectrum range can be chosen from ±5% /±15% /±24% /±34%. The spread spectrum function will lower the total electromagnetic emitting energy by spreading the energy into a wider range to significantly degrades the peak energy of EMI. With spread spectrum, the EMI test is easier to pass with a smaller size and lower cost filter circuit.

OPERATING MODE

IS31FL3237 can operate in PWM Mode. The brightness of each LED can be modulated with 256/1024/4096/65536 steps by PWM registers. For example, if N=256, the data in PWM Register is "0000 0100", then the PWM is the fourth step.

Writing new data continuously to the registers can modulate the brightness of the LEDs to achieve a breathing effect.

SHUTDOWN MODE

Shutdown mode can be used as a means of reducing power consumption. During shutdown mode all registers retain their data.

Software Shutdown

By setting the SSD bit of the Control Register (00h) to "0", the IS31FL3237 will operate in software shutdown mode. When the IS31FL3237 is in software shutdown, all current sources are switched off, so the LEDs are OFF but all registers remain accessible. Typical current consumption is 0.8μA (V_{CC}=3.6V).

Hardware Shutdown

The IS31FL3237 enters hardware shutdown when it's SDB pin is pulled low. All analog circuits are disabled during hardware shutdown, typical current consumption is 0.8μA (V_{CC}=3.6V).

The chip releases hardware shutdown when the SDB pin is pulled high. The rising edge of SDB pin will reset the I2C module, but the register information is retained. During hardware shutdown the registers are accessible.

If the VCC supply drops below 1.75V but remains above 0.1V while SDB is pulled low, please re-initialize all Function Registers before SDB pulled high.

LAYOUT

The IS31FL3237 can consume lots of power so good PCB layout will help improve the reliability of the chip. Please consider below factors when layout the PCB.

R_{ISET}

R_{ISET} should be close to the chip and the ground side should well connect to the GND plane.

Power Supply Lines

When designing the PCB layout pattern, the first step should consider about the supply line and GND connection, especially those traces with high current, also the digital and analog blocks' supply line and GND should be separated to avoid the noise from digital block affect the analog block.

At least one 0.1μF capacitor, if possible with a 1μF capacitor is recommended to connected to the ground at power supply pin of the chip, and it needs to close to the chip and the ground net of the capacitor should be well connected to the GND plane.

Thermal Consideration

The over temperature of the chip may result in deterioration of the properties of the chip. The thermal pad of IS31FL3237 should connect to GND net and need to use 9 or 16 vias connect to GND copper area, the GND area should be as large area as possible to help radiate the heat from the IS31FL3237.

Current Rating Example

For a R_{ISET}=3.3kΩ application, the current rating for each net is as follows:

• VCC pin maximum current is 8mA when V_{CC}=5V, but the VLED+ net is provided total current of all outputs, its current can as much as 23mA×36=828mA, recommend trace width for VCC pin: 0.20mm~0.3mm, recommend trace width for VLED+ net: 0.30mm~0.5mm,

• Output pins=23mA, recommend trace width is 0.2mm~0.254mm

• All other pins<3mA, recommend trace width is 0.15mm~0.254mm

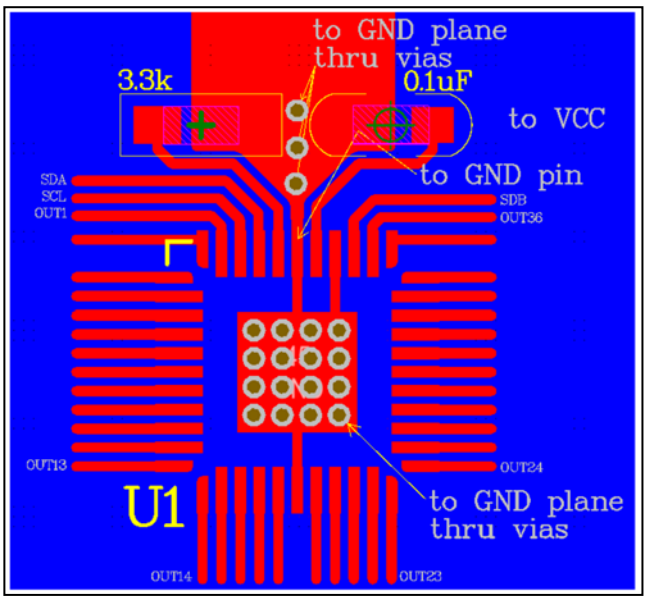


Figure 13 Layout Example

CLASSIFICATION REFLOW PROFILES

Profile Feature	Pb-Free Assembly
Preheat & Soak Temperature min (Tsmin) Temperature max (Tsmax) Time (Tsmin to Tsmax) (ts)	150°C 200°C 60-120 seconds
Average ramp-up rate (Tsmax to Tp)	3°C/second max.
Liquidous temperature (TL) Time at liquidous (tL)	217°C 60-150 seconds
Peak package body temperature (Tp)*	Max 260°C
Time (tp)** within 5°C of the specified classification temperature (Tc)	Max 30 seconds
Average ramp-down rate (Tp to Tsmax)	6°C/second max.
Time 25°C to peak temperature	8 minutes max.

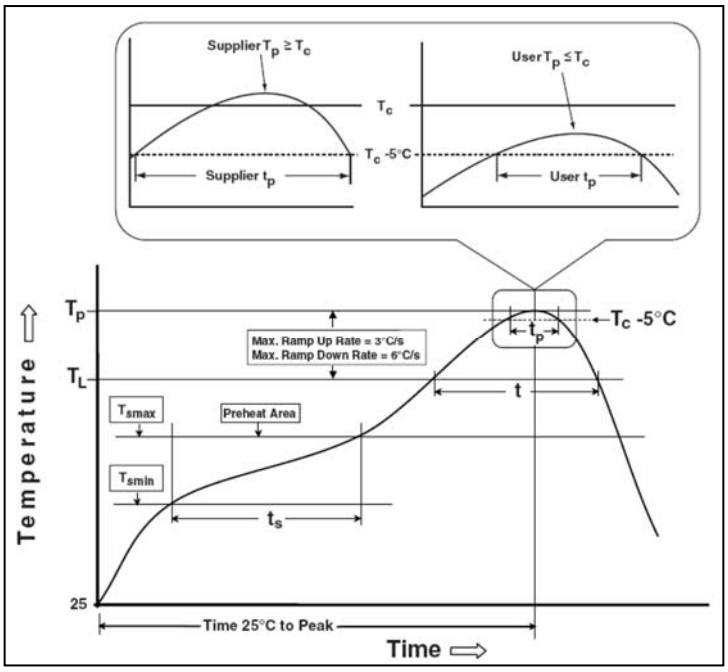
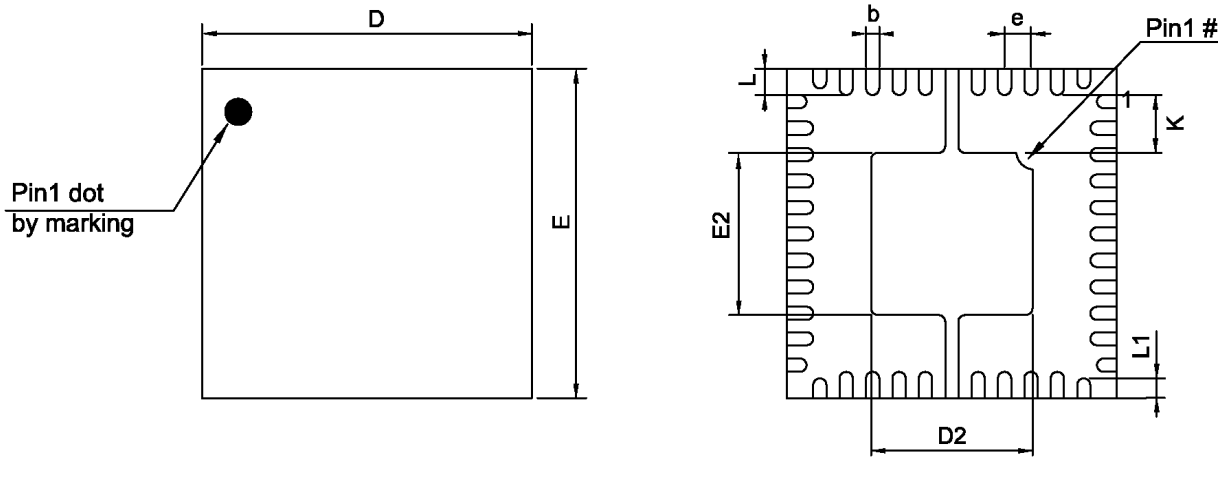


Figure 14 Classification Profile

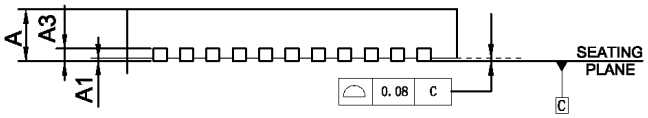
PACKAGE INFORMATION

QFN-44



TOP VIEW

BOTTOM VIEW



SIDE VIEW

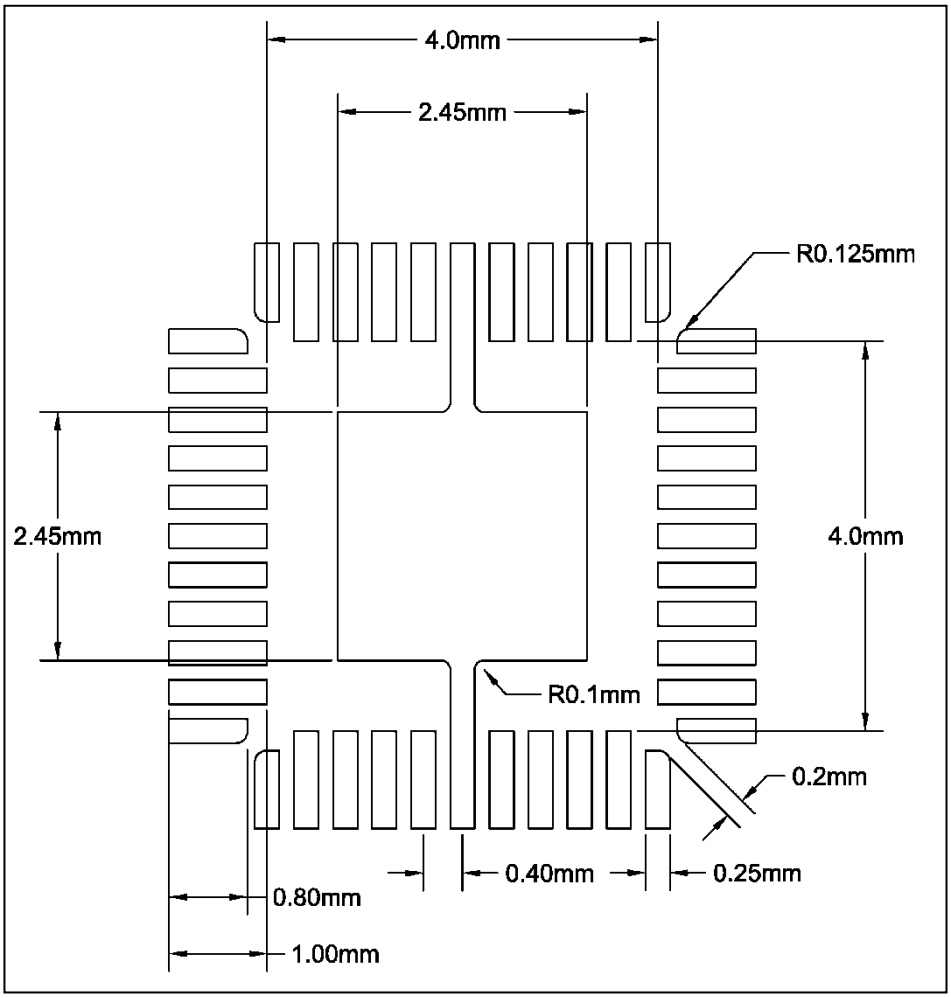
SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	0.70	0.75	0.80
A1	0.00	—	0.05
A3	0.20REF		
D	4.90	5.00	5.10
E	4.90	5.00	5.10
E2	2.30	2.45	2.55
D2	2.30	2.45	2.55
b	0.15	0.20	0.25
L	0.30	0.40	0.50
L1	0.20	0.30	0.40
K	0.20	—	—
e	0.40BSC		

NOTES:
1.CONTROLLING DIMENSION:MM
2.REFERENCE DOCUMENT:NA CLOSE TOOL
3.THE PIN'S SHARP AND THERMAL PAD SHOWS DIFFERENT SHARP AMONG DIFFERENT FACTORIES.

233-570-288 Rev. A

RECOMMENDED LAND PATTERN

QFN-44



Note:
1. Land pattern complies to IPC-7351.
2. All dimensions in MM.
3. This document (including dimensions, notes & specs) is a recommendation based on typical circuit board manufacturing parameters. Since land pattern design depends on many factors unknown (eg. User's board manufacturing specs), user must determine suitability for use.

REVISION HISTORY

Revision	Detail Information	Date
0A	Initial release.	2017.12.27
0B	1. Update ELECTRICAL CHARACTERISTICS table 2. Add Table 6 PWM and Scaling Register Map	2018.05.10
A	1. Update Figure 1 2. Correct Table 4 3. Update PCB LAYOUT section 4. Update ELECTRICAL CHARACTERISTICS table. 5. Update land pattern	2018.10.10
B	Add R/W information for Table 2	2018.12.17
C	Correct OSC definition and Table 4	2019.04.26
D	1. Add figure 1: Typical Application Circuit (V_{CC}=$V_{Battery}$) 2. Add V_{OD}/V_{SD} (open/short threshold) in ELECTRICAL CHARACTERISTICS table 3. Add PHASE DELAY and CLOCK PHASE section in Application Information 4. Add 16-bit PWM feature in title	2020.01.06
E	1. Update land pattern 2. Update note 1 and correct OUT1-OUT36 ABSOLUTE MAXIMUM RATINGS	2021.10.15
F	Update land pattern thermal pad size	2022.02.21
G	Update to new Lumissil logo and add RoHS	2024.10.08
H	Update the 49h Function Information in Table 2	2026.05.06