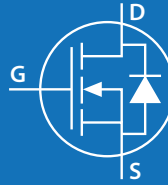


EPC2216 – Automotive 15 V (D-S) Enhancement Mode Power Transistor

 $V_{DS}, 15\text{ V}$
 $R_{DS(on)}, 26\text{ m}\Omega$
 $I_D, 3.4\text{ A}$

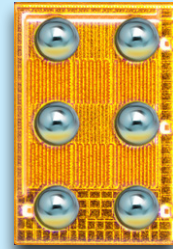
AEC-Q101



Revised April 25, 2025

Gallium Nitride's exceptionally high electron mobility and low temperature coefficient allows very low $R_{DS(on)}$, while its lateral device structure and majority carrier diode provide exceptionally low Q_G and zero Q_{RR} . The end result is a device that can handle tasks where very high switching frequency, and low on-time are beneficial as well as those where on-state losses dominate.

Questions:
Ask a GaN
Expert



Die size: 0.85 x 1.2 mm

EPC2216 eGaN® FETs are supplied only in passivated die form with solder bumps

Applications

- High speed DC-DC conversion
- Lidar/pulsed power applications
- Lidar for augmented reality applications

Benefits

- Ultra high efficiency
- Ultra low $R_{DS(on)}$
- Ultra low Q_G
- Ultra small footprint

Scan QR code or click link below for more information including reliability reports, device models, demo boards!


<https://l.ead.me/EPC2216>

Maximum Ratings

PARAMETER		VALUE	UNIT
V_{DS}	Drain-to-Source Voltage (Continuous)	15	V
	Drain-to-Source Voltage (up to 10,000 5 ms pulses at 150°C)	18	
I_D	Continuous ($T_A = 25^\circ\text{C}$)	3.4	A
	Pulsed (25°C , $T_{PULSE} = 300\ \mu\text{s}$)	28	
V_{GS}	Gate-to-Source Voltage	6	V
	Gate-to-Source Voltage	-4	
T_J	Operating Temperature	-55 to 150	°C
T_{STG}	Storage Temperature	-55 to 150	

Thermal Characteristics

PARAMETER		TYP	UNIT
$R_{\theta JC}$	Thermal Resistance, Junction-to-Case	5.7	°C/W
$R_{\theta JB}$	Thermal Resistance, Junction-to-Board	39	
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient (Note 1)	97	

Note 1: $R_{\theta JA}$ is determined with the device mounted on one square inch of copper pad, single layer 2 oz copper on FR4 board. See https://epc-co.com/epc/documents/product-training/Appnote_Thermal_Performance_of_eGaN_FETs.pdf for details

Static Characteristics ($T_J = 25^\circ\text{C}$ unless otherwise stated)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT	
BV_{DSS}	Drain-to-Source Voltage	$V_{GS} = 0\text{ V}$, $I_D = 0.1\text{ mA}$	15		V	
I_{DSS}	Drain-Source Leakage	$V_{GS} = 0\text{ V}$, $V_{DS} = 15\text{ V}$	0.01	0.1	mA	
I_{GSS}	Gate-to-Source Forward Leakage	$V_{GS} = 5\text{ V}$	0.004	0.5	mA	
	Gate-to-Source Forward Leakage [#]	$V_{GS} = 5\text{ V}$	0.02	1	mA	
	Gate-to-Source Reverse Leakage	$V_{GS} = -4\text{ V}$	0.01	0.1	mA	
$V_{GS(TH)}$	Gate Threshold Voltage	$V_{DS} = V_{GS}$, $I_D = 1\text{ mA}$	0.7	1	2.5	V
$R_{DS(on)}$	Drain-Source On Resistance	$V_{GS} = 5\text{ V}$, $I_D = 1.5\text{ A}$	20	26	mΩ	
V_{SD}	Source-Drain Forward Voltage [#]	$V_{GS} = 0\text{ V}$, $I_S = 0.5\text{ A}$	1.9		V	

[#] Defined by design. Not subject to production test.

All measurements were done with substrate connected to source.

Dynamic Characteristics# ($T_J = 25^\circ\text{C}$ unless otherwise stated)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
C_{ISS}	Input Capacitance	$V_{GS} = 0\text{ V}, V_{DS} = 7.5\text{ V}$		98	118	pF
C_{RSS}	Reverse Transfer Capacitance			20		
C_{OSS}	Output Capacitance			66	99	
$C_{OSS(ER)}$	Effective Output Capacitance, Energy Related (Note 2)	$V_{GS} = 0\text{ V}, V_{DS} = 0\text{ to }7.5\text{ V}$		69		
$C_{OSS(TR)}$	Effective Output Capacitance, Time Related (Note 3)			71		
R_G	Gate Resistance			0.5		Ω
Q_G	Total Gate Charge	$V_{GS} = 5\text{ V}, V_{DS} = 7.5\text{ V}, I_D = 1.5\text{ A}$		0.87	1.1	nC
Q_{GS}	Gate-to-Source Charge	$V_{DS} = 7.5\text{ V}, I_D = 1.5\text{ A}$		0.21		
Q_{GD}	Gate-to-Drain Charge			0.13		
$Q_{G(TH)}$	Gate Charge at Threshold			0.16		
Q_{OSS}	Output Charge	$V_{GS} = 0\text{ V}, V_{DS} = 7.5\text{ V}$		0.53	0.8	
Q_{RR}	Source-Drain Recovery Charge			0		

Defined by design. Not subject to production test.

All measurements were done with substrate connected to source.

Note 2: $C_{OSS(ER)}$ is a fixed capacitance that gives the same stored energy as C_{OSS} while V_{DS} is rising from 0 to 50% BV_{DSS} .

Note 3: $C_{OSS(TR)}$ is a fixed capacitance that gives the same charging time as C_{OSS} while V_{DS} is rising from 0 to 50% BV_{DSS} .

Figure 1: Typical Output Characteristics at 25°C

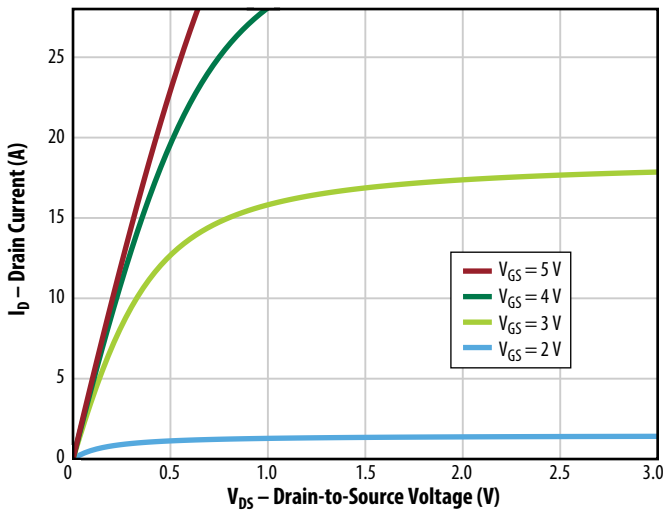


Figure 2: Typical Transfer Characteristics

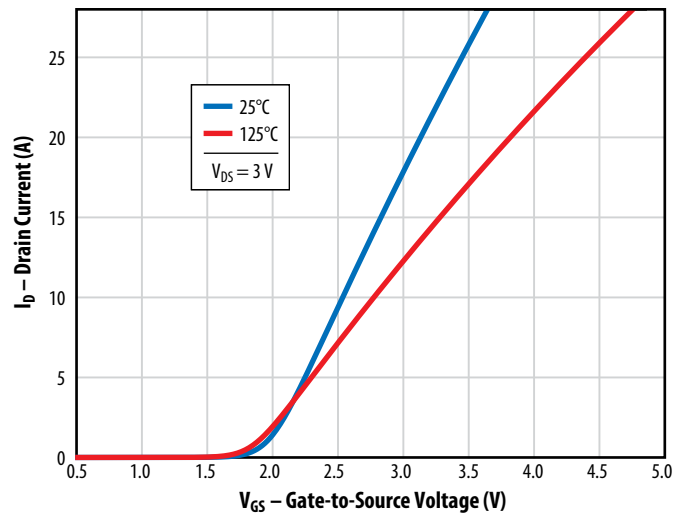


Figure 3: Typical $R_{DS(on)}$ vs. V_{GS} for Various Drain Currents

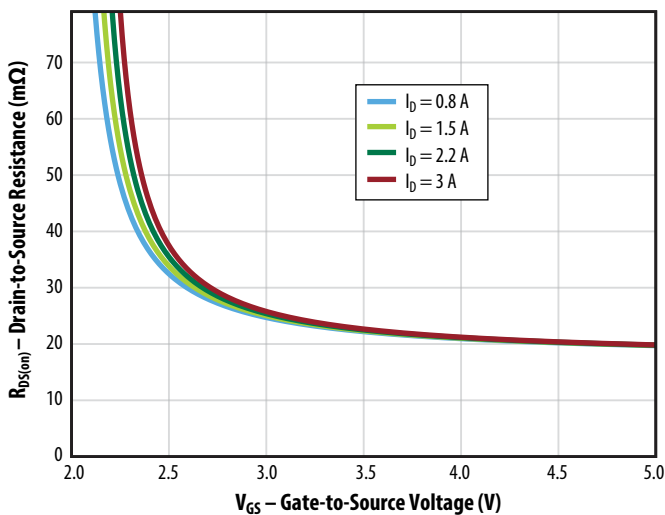


Figure 4: Typical $R_{DS(on)}$ vs. V_{GS} for Various Temperatures

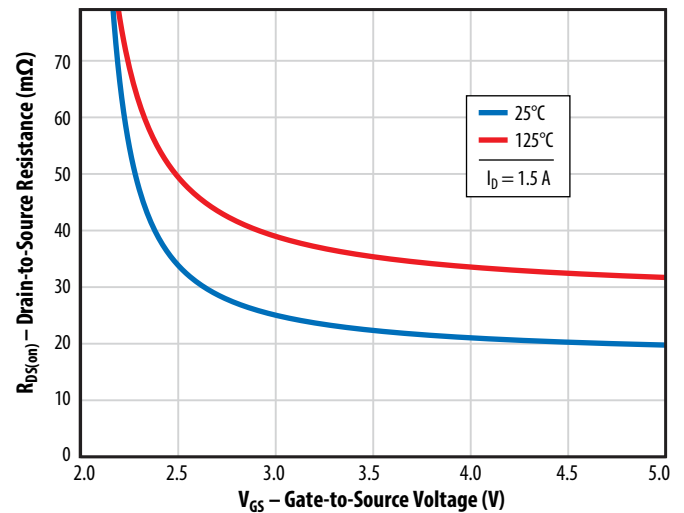


Figure 5a: Typical Capacitance (Linear Scale)

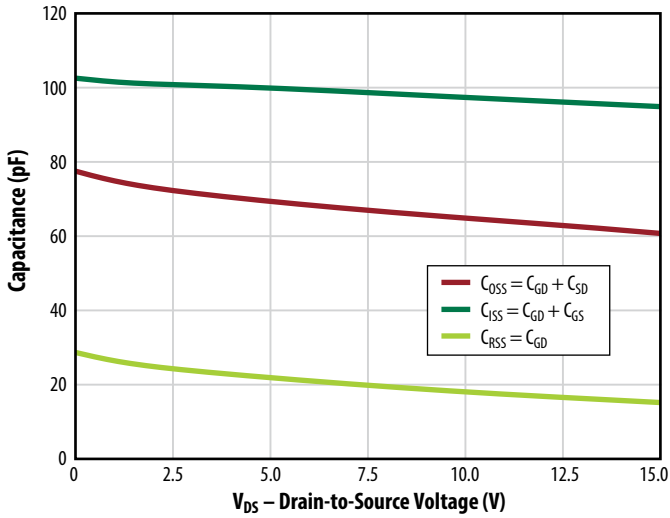


Figure 5b: Typical Capacitance (Log Scale)

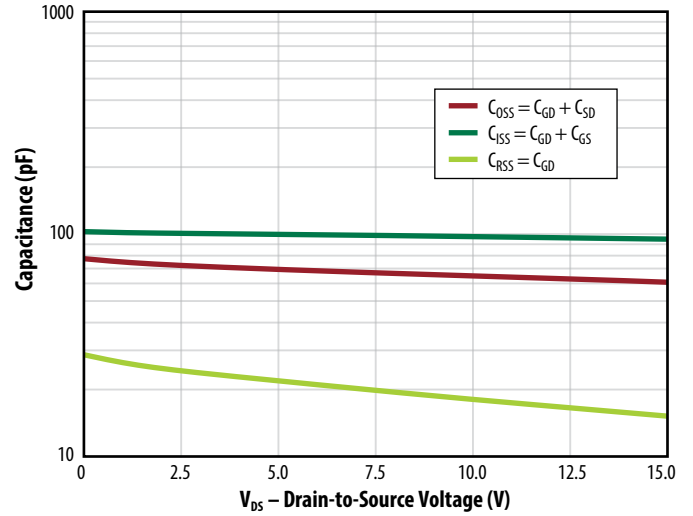


Figure 6: Typical Output Charge and C_OSS Stored Energy

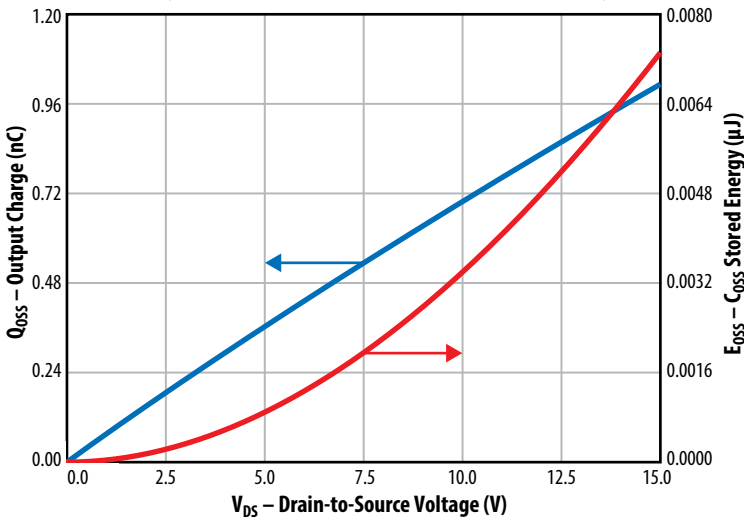


Figure 7: Typical Gate Charge

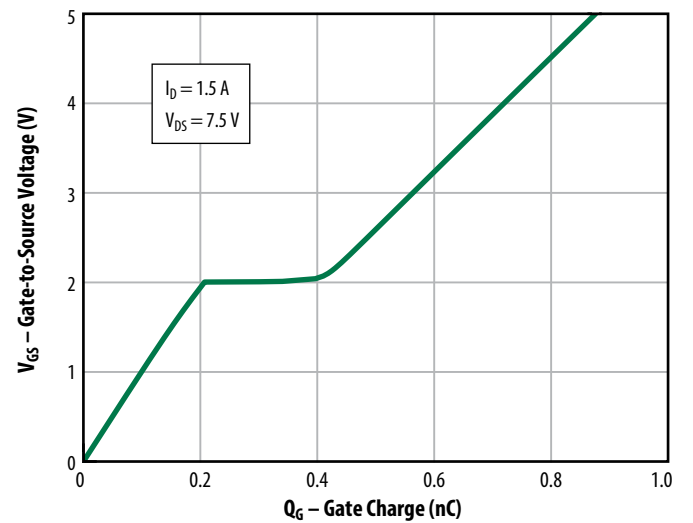
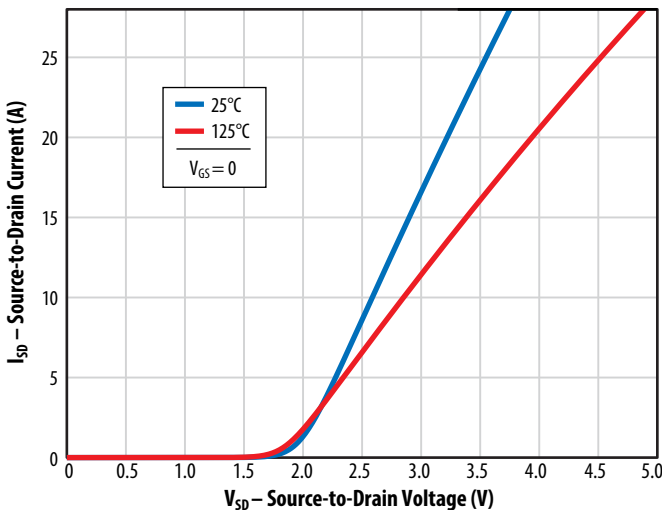


Figure 8: Typical Reverse Drain-Source Characteristics



Note: Negative gate drive voltage increases the reverse drain-source voltage.
EPC recommends 0 V for OFF.

Figure 9: Typical Normalized On-State Resistance vs. Temp.

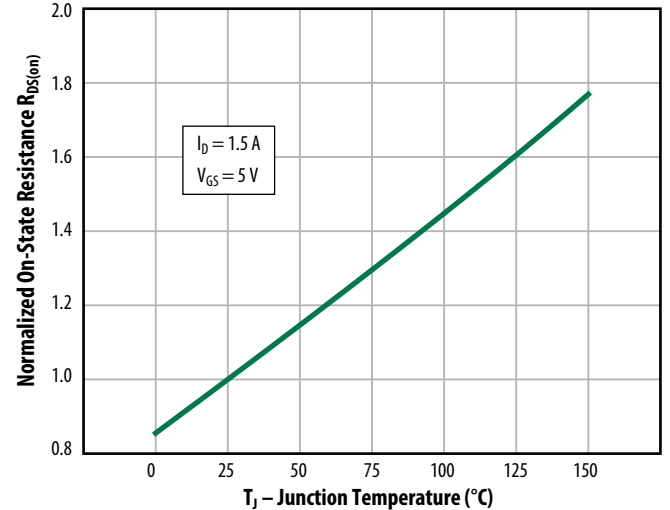


Figure 10: Typical Normalized Threshold Voltage vs. Temp.

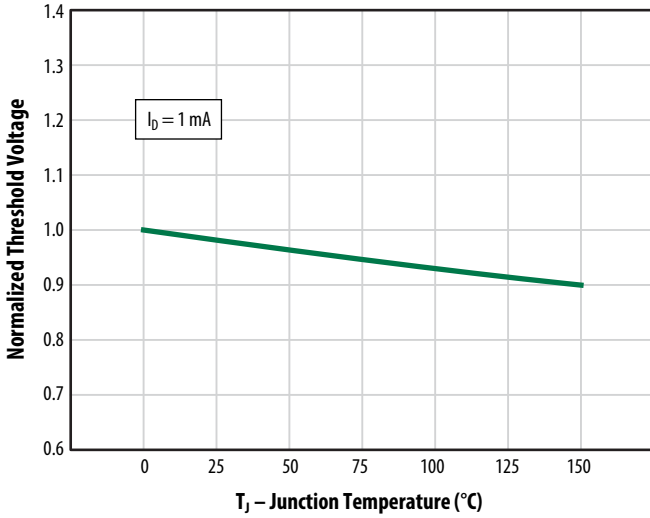


Figure 11: Safe Operating Area

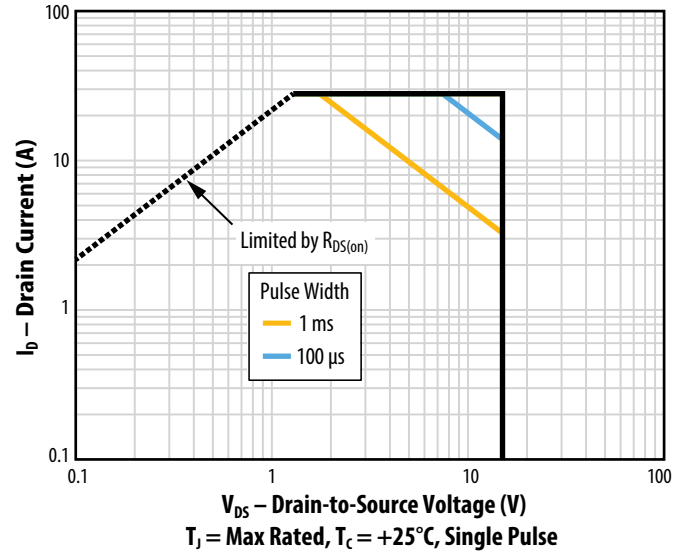
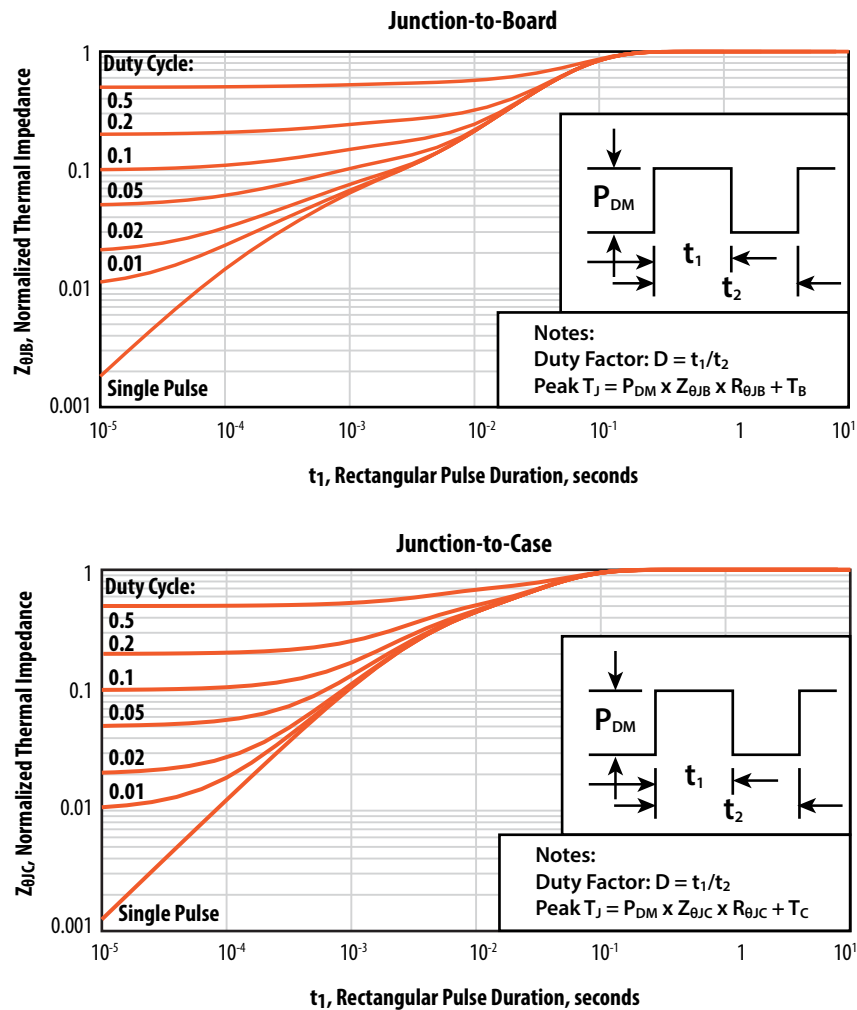
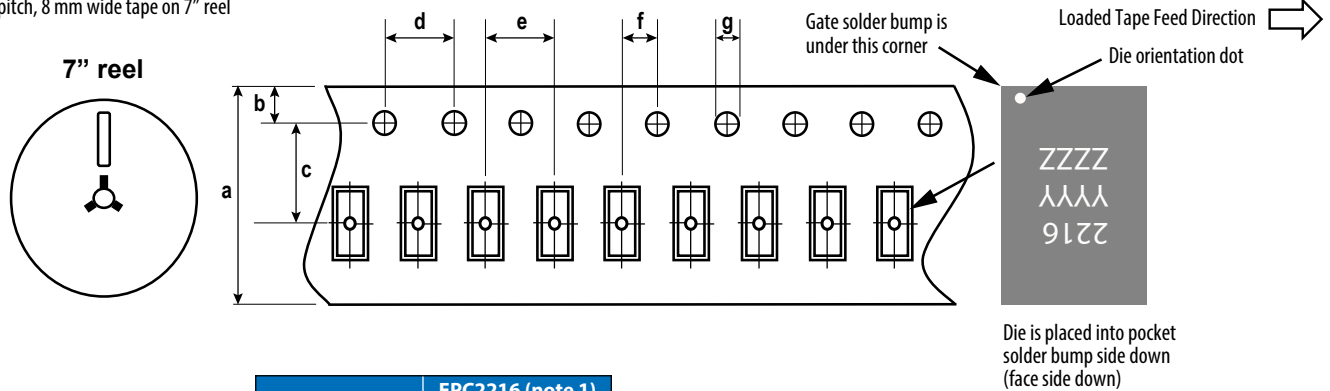


Figure 12: Typical Transient Thermal Response Curves



TAPE AND REEL CONFIGURATION

4 mm pitch, 8 mm wide tape on 7" reel

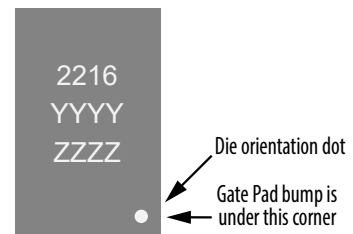


Dimension (mm)	EPC2216 (note 1)		
	target	min	max
a	8.00	7.90	8.30
b	1.75	1.65	1.85
c (note 2)	3.50	3.45	3.55
d	4.00	3.90	4.10
e	4.00	3.90	4.10
f (note 2)	2.00	1.95	2.05
g	1.5	1.5	1.6

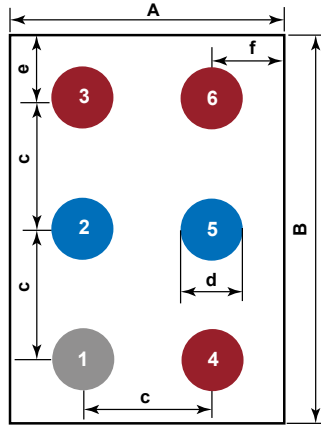
Note 1: MSL 1 (moisture sensitivity level 1) classified according to IPC/JEDEC industry standard.
 Note 2: Pocket position is relative to the sprocket hole measured as true position of the pocket, not the pocket hole.

DIE MARKINGS

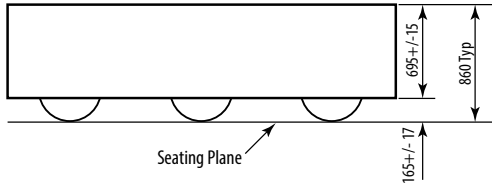
Part Number	Laser Markings		
	Part # Marking Line 1	Lot_Date Code Marking line 2	Lot_Date Code Marking line 3
EPC2216	2216	YYYY	ZZZZ



DIE OUTLINE
Solder Bump View



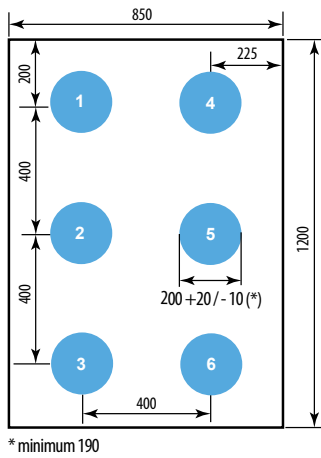
Side View



DIM	Micrometers		
	MIN	Nominal	MAX
A	820	850	880
B	1170	1200	1230
c		400	
d	187	208	229
e	185	200	215
f	210	225	240

Pad 1 is Gate;
Pads 2 and 5 are Drain;
Pads 3, 4, 6 are Source

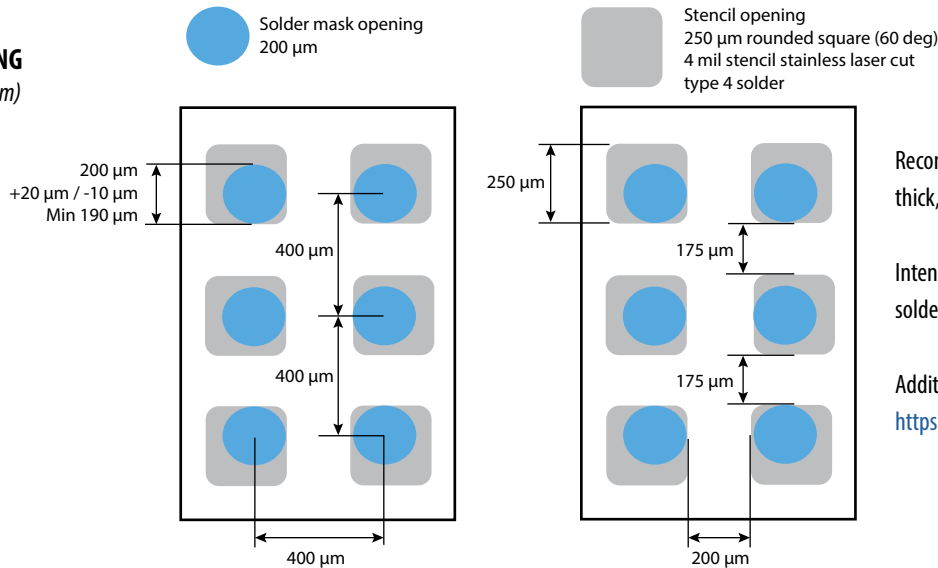
RECOMMENDED LAND PATTERN
(measurements in μm)



The land pattern is solder mask defined.

Pad 1 is Gate;
Pads 2 and 5 are Drain;
Pads 3, 4, 6 are Source

RECOMMENDED STENCIL DRAWING
(measurements in μm)



Recommended stencil should be 4 mil (100 μm) thick, must be laser cut, openings per drawing.

Intended for use with SAC305 Type 4 solder, reference 88.5% metals content.

Additional assembly resources available at <https://epc-co.com/epc/design-support>

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