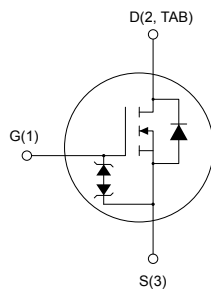
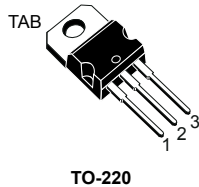


## N-channel 800 V, 230 mΩ typ., 16 A MDmesh K5 Power MOSFET in a TO-220 package



AM01476v1\_tab



### Product status link

[STP23N80K5](#)

### Product summary

|            |            |
|------------|------------|
| Order code | STP23N80K5 |
| Marking    | 23N80K5    |
| Package    | TO-220     |
| Packing    | Tube       |

### Features

| Order code | V <sub>DS</sub> | R <sub>DS(on)</sub> max. | I <sub>D</sub> |
|------------|-----------------|--------------------------|----------------|
| STP23N80K5 | 800 V           | 280 mΩ                   | 16 A           |

- Very low FoM (figure of merit)
- Ultra-low gate charge
- 100% avalanche tested
- Zener-protected

### Applications

- Switching applications

### Description

This very high voltage N-channel Power MOSFET is designed using MDmesh K5 technology based on an innovative proprietary vertical structure. The result is a dramatic reduction in on-resistance and ultra-low gate charge for applications requiring superior power density and high efficiency.

# 1 Electrical ratings

**Table 1. Absolute maximum ratings**

| Symbol         | Parameter                                                         | Value      | Unit               |
|----------------|-------------------------------------------------------------------|------------|--------------------|
| $V_{DS}$       | Drain-source voltage                                              | 800        | V                  |
| $V_{GS}$       | Gate-source voltage                                               | $\pm 30$   | V                  |
| $I_D$          | Drain current (continuous) at $T_C = 25\text{ }^{\circ}\text{C}$  | 16         | A                  |
|                | Drain current (continuous) at $T_C = 100\text{ }^{\circ}\text{C}$ | 10         |                    |
| $I_{DM}^{(1)}$ | Drain current (pulsed)                                            | 64         | A                  |
| $P_{TOT}$      | Total power dissipation at $T_C = 25\text{ }^{\circ}\text{C}$     | 190        | W                  |
| $dv/dt^{(2)}$  | Peak diode recovery voltage slope                                 | 4.5        | V/ns               |
| $dv/dt^{(3)}$  | MOSFET $dv/dt$ ruggedness                                         | 50         |                    |
| $T_{stg}$      | Storage temperature range                                         | -55 to 150 | $^{\circ}\text{C}$ |
| $T_J$          | Operating junction temperature range                              |            |                    |

1. Pulse width is limited by safe operating area.
2.  $I_{SD} \leq 16\text{ A}$ ,  $di/dt=100\text{ A}/\mu\text{s}$ ;  $V_{DS(peak)} < V_{(BR)DSS}$ ,  $V_{DD} = 640\text{ V}$ .
3.  $V_{DD} \leq 640\text{ V}$

**Table 2. Thermal data**

| Symbol     | Parameter                               | Value | Unit                        |
|------------|-----------------------------------------|-------|-----------------------------|
| $R_{thJC}$ | Thermal resistance, junction-to-case    | 0.66  | $^{\circ}\text{C}/\text{W}$ |
| $R_{thJA}$ | Thermal resistance, junction-to-ambient | 62.5  |                             |

**Table 3. Avalanche characteristics**

| Symbol         | Parameter                                       | Value | Unit |
|----------------|-------------------------------------------------|-------|------|
| $I_{AR}^{(1)}$ | Avalanche current, repetitive or not repetitive | 5     | A    |
| $E_{AS}^{(2)}$ | Single pulse avalanche energy                   | 400   | mJ   |

1. Pulse width limited by  $T_J$  max.
2. Starting  $T_J = 25\text{ }^{\circ}\text{C}$ ,  $I_D = I_{AR}$ ,  $V_{DD} = 50\text{ V}$ .

## 2 Electrical characteristics

$T_C = 25\text{ °C}$  unless otherwise specified.

**Table 4. On/off states**

| Symbol        | Parameter                         | Test conditions                                                                        | Min. | Typ. | Max.     | Unit          |
|---------------|-----------------------------------|----------------------------------------------------------------------------------------|------|------|----------|---------------|
| $V_{(BR)DSS}$ | Drain-source breakdown voltage    | $V_{GS} = 0\text{ V}$ , $I_D = 1\text{ mA}$                                            | 800  |      |          | V             |
| $I_{DSS}$     | Zero gate voltage drain current   | $V_{GS} = 0\text{ V}$ , $V_{DS} = 800\text{ V}$                                        |      |      | 1        | $\mu\text{A}$ |
|               |                                   | $V_{GS} = 0\text{ V}$ , $V_{DS} = 800\text{ V}$ , $T_C = 125\text{ °C}$ <sup>(1)</sup> |      |      | 50       |               |
| $I_{GSS}$     | Gate-body leakage current         | $V_{DS} = 0\text{ V}$ , $V_{GS} = \pm 20\text{ V}$                                     |      |      | $\pm 10$ | $\mu\text{A}$ |
| $V_{GS(th)}$  | Gate threshold voltage            | $V_{DS} = V_{GS}$ , $I_D = 100\text{ }\mu\text{A}$                                     | 3    | 4    | 5        | V             |
| $R_{DS(on)}$  | Static drain-source on-resistance | $V_{GS} = 10\text{ V}$ , $I_D = 8\text{ A}$                                            |      | 230  | 280      | m $\Omega$    |

1. Specified by design, not tested in production.

**Table 5. Dynamic**

| Symbol            | Parameter                             | Test conditions                                                                                                                              | Min. | Typ. | Max. | Unit     |
|-------------------|---------------------------------------|----------------------------------------------------------------------------------------------------------------------------------------------|------|------|------|----------|
| $C_{iss}$         | Input capacitance                     | $V_{DS} = 100\text{ V}$ , $f = 1\text{ MHz}$ , $V_{GS} = 0\text{ V}$                                                                         | -    | 1000 | -    | pF       |
| $C_{oss}$         | Output capacitance                    |                                                                                                                                              | -    | 65   | -    |          |
| $C_{rss}$         | Reverse transfer capacitance          |                                                                                                                                              | -    | 1.5  | -    |          |
| $C_{o(tr)}^{(1)}$ | Time-related equivalent capacitance   | $V_{DS} = 0\text{ to }640\text{ V}$ , $V_{GS} = 0\text{ V}$                                                                                  | -    | 165  | -    | pF       |
| $C_{o(er)}^{(2)}$ | Energy-related equivalent capacitance |                                                                                                                                              | -    | 59   | -    |          |
| $R_g$             | Intrinsic gate resistance             | $f = 1\text{ MHz}$ , $I_D = 0\text{ A}$                                                                                                      | -    | 4.7  | -    | $\Omega$ |
| $Q_g$             | Total gate charge                     | $V_{DD} = 640\text{ V}$ , $I_D = 16\text{ A}$ , $V_{GS} = 0\text{ to }10\text{ V}$<br>(see Figure 13. Test circuit for gate charge behavior) | -    | 33   | -    | nC       |
| $Q_{gs}$          | Gate-source charge                    |                                                                                                                                              | -    | 6    | -    |          |
| $Q_{gd}$          | Gate-drain charge                     |                                                                                                                                              | -    | 25   | -    |          |

1.  $C_{o(tr)}$  is a constant capacitance value that gives the same charging time as  $C_{oss}$  while  $V_{DS}$  is rising from 0 V to the stated value.

2.  $C_{o(er)}$  is a constant capacitance value that gives the same stored energy as  $C_{oss}$  while  $V_{DS}$  is rising from 0 V to the stated value.

**Table 6. Switching times**

| Symbol       | Parameter           | Test conditions                                                                                                                                                                                              | Min. | Typ. | Max. | Unit |
|--------------|---------------------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|------|------|------|------|
| $t_{d(on)}$  | Turn-on delay time  | $V_{DD} = 400\text{ V}$ , $I_D = 8\text{ A}$ , $R_G = 4.7\text{ }\Omega$ ,<br>$V_{GS} = 10\text{ V}$ (see Figure 12. Test circuit for resistive load switching times and Figure 17. Switching time waveform) | -    | 14   | -    | ns   |
| $t_r$        | Rise time           |                                                                                                                                                                                                              | -    | 9    | -    |      |
| $t_{d(off)}$ | Turn-off delay time |                                                                                                                                                                                                              | -    | 48   | -    |      |
| $t_f$        | Fall time           |                                                                                                                                                                                                              | -    | 9    | -    |      |

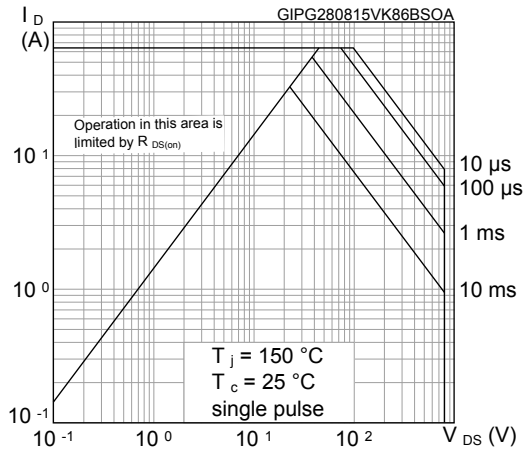
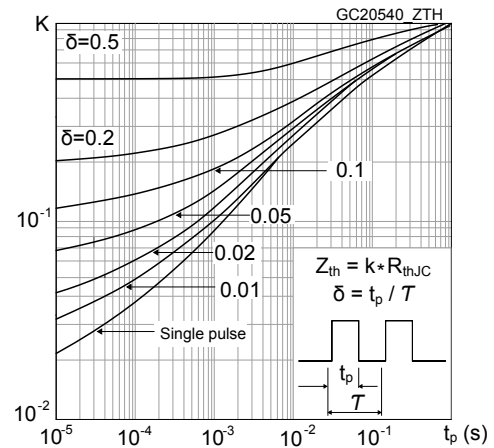
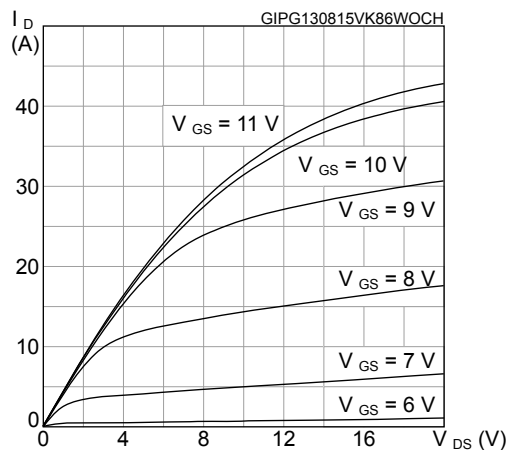
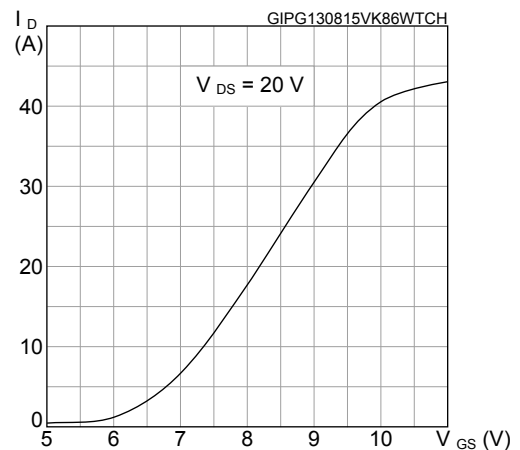
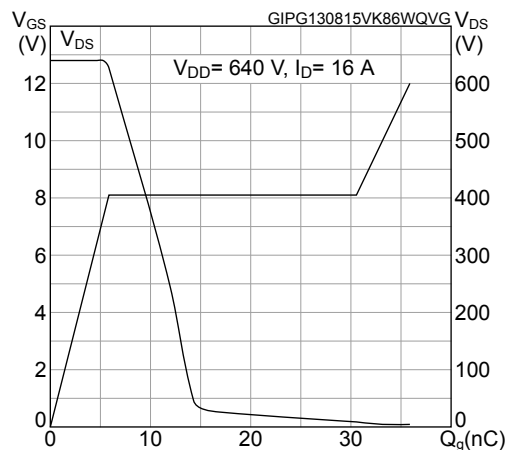
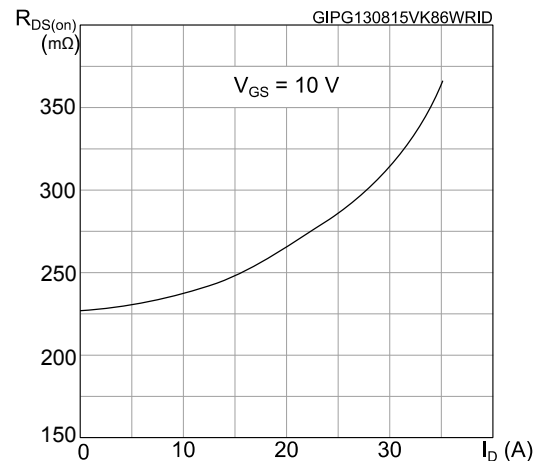
**Table 7. Source-drain diode**

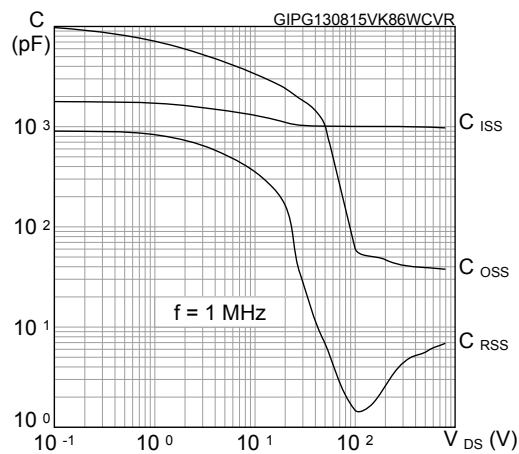
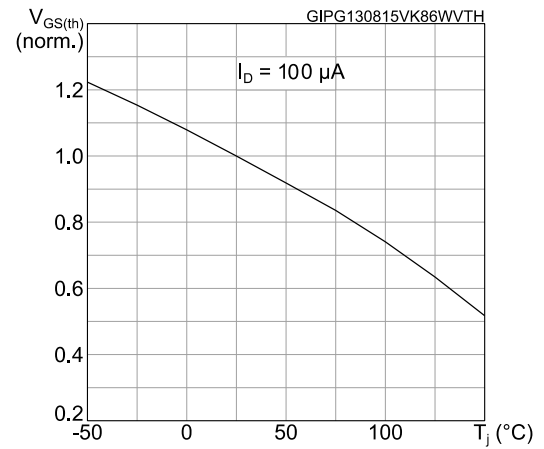
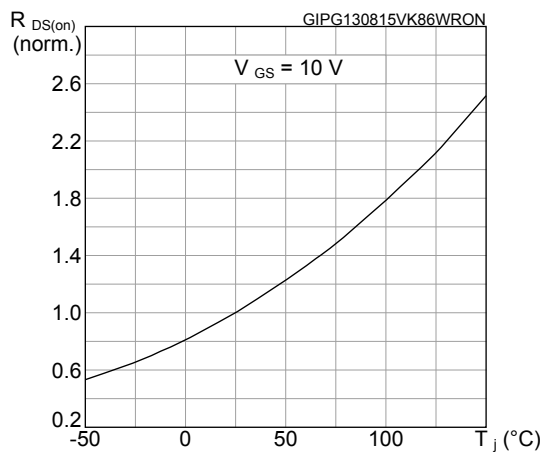
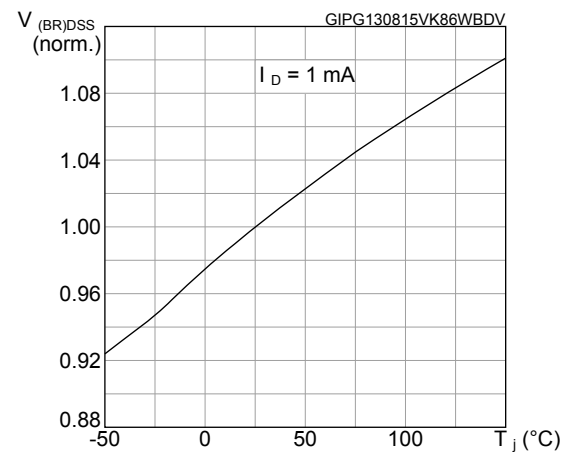
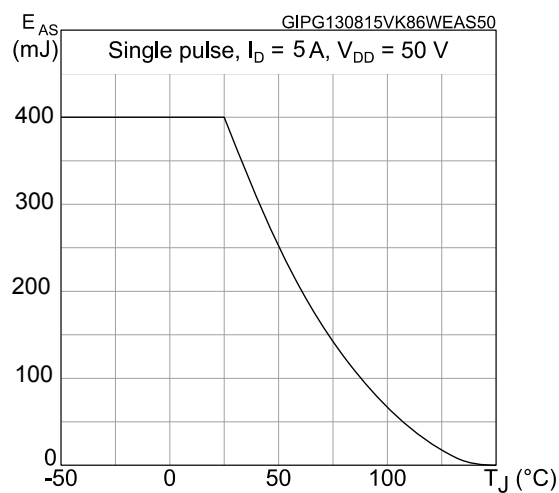
| Symbol          | Parameter                     | Test conditions                                                                                                                                                                                                 | Min. | Typ. | Max. | Unit          |
|-----------------|-------------------------------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|------|------|------|---------------|
| $I_{SD}$        | Source-drain current          |                                                                                                                                                                                                                 | -    |      | 16   | A             |
| $I_{SDM}^{(1)}$ | Source-drain current (pulsed) |                                                                                                                                                                                                                 | -    |      | 64   | A             |
| $V_{SD}^{(2)}$  | Forward on voltage            | $V_{GS} = 0\text{ V}$ , $I_{SD} = 16\text{ A}$                                                                                                                                                                  | -    |      | 1.5  | V             |
| $t_{rr}$        | Reverse recovery time         | $I_{SD} = 16\text{ A}$ , $di/dt = 100\text{ A}/\mu\text{s}$ , $V_{DD} = 60\text{ V}$<br>(see Figure 14. Test circuit for inductive load switching and diode recovery times)                                     | -    | 410  |      | ns            |
| $Q_{rr}$        | Reverse recovery charge       |                                                                                                                                                                                                                 | -    | 7    |      | $\mu\text{C}$ |
| $I_{RRM}$       | Reverse recovery current      |                                                                                                                                                                                                                 | -    | 34   |      | A             |
| $t_{rr}$        | Reverse recovery time         | $I_{SD} = 16\text{ A}$ , $di/dt = 100\text{ A}/\mu\text{s}$ , $V_{DD} = 60\text{ V}$ ,<br>$T_J = 150\text{ }^\circ\text{C}$ (see Figure 14. Test circuit for inductive load switching and diode recovery times) | -    | 650  |      | ns            |
| $Q_{rr}$        | Reverse recovery charge       |                                                                                                                                                                                                                 | -    | 10   |      | $\mu\text{C}$ |
| $I_{RRM}$       | Reverse recovery current      |                                                                                                                                                                                                                 | -    | 32   |      | A             |

1. Pulse width is limited by safe operating area.

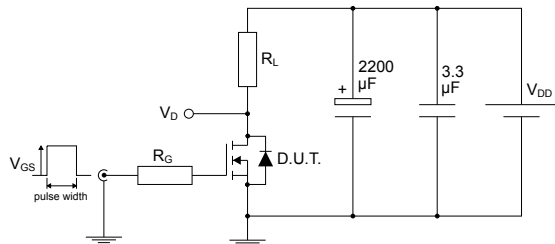
2. Pulse test: pulse duration = 300  $\mu\text{s}$ , duty cycle 1.5%.

## 2.1 Electrical characteristics (curves)

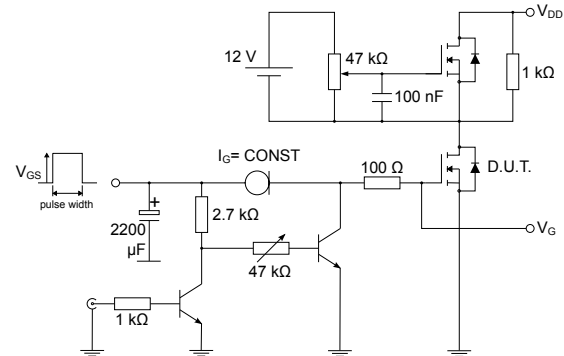
**Figure 1. Safe operating area**

**Figure 2. Normalized transient thermal impedance**

**Figure 3. Typical output characteristics**

**Figure 4. Typical transfer characteristics**

**Figure 5. Typical gate charge characteristics**

**Figure 6. Typical drain-source on-resistance**


**Figure 7. Typical capacitance characteristics**

**Figure 8. Normalized gate threshold vs temperature**

**Figure 9. Normalized on-resistance vs temperature**

**Figure 10. Normalized breakdown voltage vs temperature**

**Figure 11. Maximum avalanche energy vs temperature**


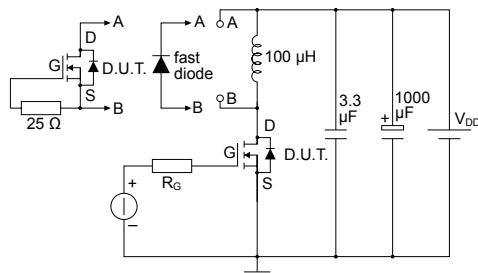
### 3 Test circuits

**Figure 12. Test circuit for resistive load switching times**


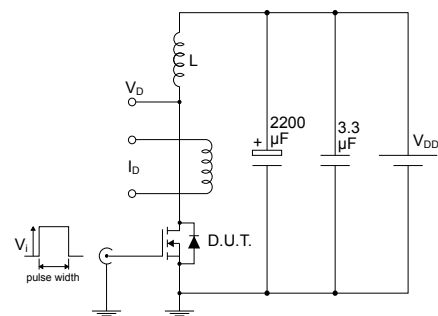
AM01468v1

**Figure 13. Test circuit for gate charge behavior**


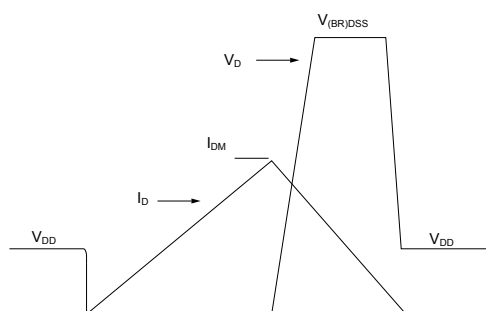
AM01469v1

**Figure 14. Test circuit for inductive load switching and diode recovery times**


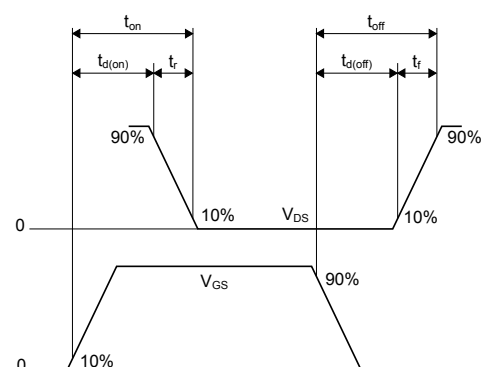
AM01470v1

**Figure 15. Unclamped inductive load test circuit**


AM01471v1

**Figure 16. Unclamped inductive waveform**


AM01472v1

**Figure 17. Switching time waveform**


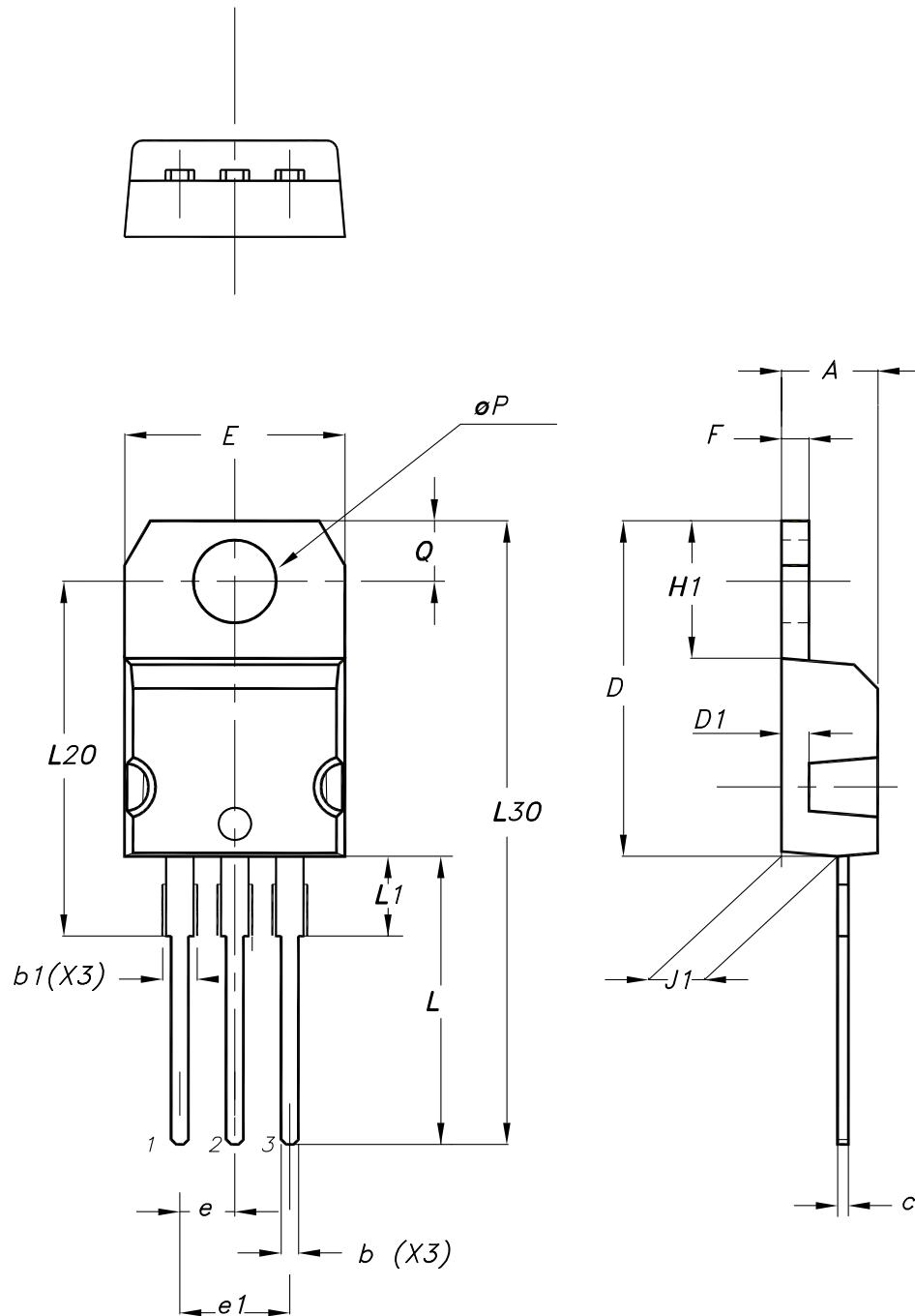
AM01473v1

## 4 Package information

To meet environmental requirements, ST offers these devices in different grades of **ECOPACK** packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions, and product status are available at: [www.st.com](http://www.st.com). ECOPACK is an ST trademark.

### 4.1 TO-220 type A package information

Figure 18. TO-220 type A package outline



0015988\_typeA\_Rev\_24



**Table 8. TO-220 type A package mechanical data**

| Dim.          | mm    |       |       |
|---------------|-------|-------|-------|
|               | Min.  | Typ.  | Max.  |
| A             | 4.40  |       | 4.60  |
| b             | 0.61  |       | 0.88  |
| b1            | 1.14  |       | 1.55  |
| c             | 0.48  |       | 0.70  |
| D             | 15.25 |       | 15.75 |
| D1            |       | 1.27  |       |
| E             | 10.00 |       | 10.40 |
| e             | 2.40  |       | 2.70  |
| e1            | 4.95  |       | 5.15  |
| F             | 1.23  |       | 1.32  |
| H1            | 6.20  |       | 6.60  |
| J1            | 2.40  |       | 2.72  |
| L             | 13.00 |       | 14.00 |
| L1            | 3.50  |       | 3.93  |
| L20           |       | 16.40 |       |
| L30           |       | 28.90 |       |
| øP            | 3.75  |       | 3.85  |
| Q             | 2.65  |       | 2.95  |
| Slug flatness |       | 0.03  | 0.10  |

## Revision history

**Table 9. Document revision history**

| Date        | Version | Changes                                                                                         |
|-------------|---------|-------------------------------------------------------------------------------------------------|
| 06-Oct-2015 | 1       | First release.                                                                                  |
| 16-Mar-2026 | 2       | Updated <a href="#">Section 4.1: TO-220 type A package information</a> .<br>Minor text changes. |

## Contents

|          |                                     |           |
|----------|-------------------------------------|-----------|
| <b>1</b> | <b>Electrical ratings</b>           | <b>2</b>  |
| <b>2</b> | <b>Electrical characteristics</b>   | <b>3</b>  |
| 2.1      | Electrical characteristics (curves) | 5         |
| <b>3</b> | <b>Test circuits</b>                | <b>7</b>  |
| <b>4</b> | <b>Package information</b>          | <b>8</b>  |
| 4.1      | TO-220 type A package information   | 8         |
|          | <b>Revision history</b>             | <b>10</b> |

**IMPORTANT NOTICE – READ CAREFULLY**

STMicroelectronics NV and its subsidiaries ("ST") reserve the right to make changes, corrections, enhancements, modifications, and improvements to ST products and/or to this document at any time without notice.

In the event of any conflict between the provisions of this document and the provisions of any contractual arrangement in force between the purchasers and ST, the provisions of such contractual arrangement shall prevail.

The purchasers should obtain the latest relevant information on ST products before placing orders. ST products are sold pursuant to ST's terms and conditions of sale in place at the time of order acknowledgment.

The purchasers are solely responsible for the choice, selection, and use of ST products and ST assumes no liability for application assistance or the design of the purchasers' products.

No license, express or implied, to any intellectual property right is granted by ST herein.

Resale of ST products with provisions different from the information set forth herein shall void any warranty granted by ST for such product.

If the purchasers identify an ST product that meets their functional and performance requirements but that is not designated for the purchasers' market segment, the purchasers shall contact ST for more information.

ST and the ST logo are trademarks of ST. For additional information about ST trademarks, refer to [www.st.com/trademarks](http://www.st.com/trademarks). All other product or service names are the property of their respective owners.

Information in this document supersedes and replaces information previously supplied in any prior versions of this document.

© 2026 STMicroelectronics – All rights reserved