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FDB088N08

N-Channel PowerTrench® MOSFET

75 V, 85 A, 8.8 mΩ

Features

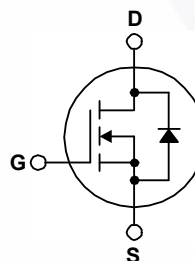
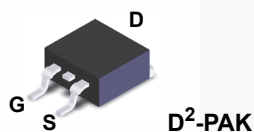
- $R_{DS(on)} = 7.3 \text{ m}\Omega$ (Typ.) @ $V_{GS} = 10 \text{ V}$, $I_D = 75 \text{ A}$
- Fast Switching Speed
- Low Gate Charge
- High Performance Trench Technology for Extremely Low $R_{DS(on)}$
- High Power and Current Handling Capability
- 100% Internal R_G Screening for Easy Paralleling Operation
- RoHS Compliant

Description

This N-Channel MOSFET is produced using Fairchild Semiconductor's advanced PowerTrench® process that has been tailored to minimize the on-state resistance while maintaining superior switching performance.

Applications

- Synchronous Rectification for ATX / Server / Telecom PSU
- Battery Protection Circuit
- Motor Drives and Uninterruptible Power Supplies



Absolute Maximum Ratings $T_C = 25^\circ\text{C}$ unless otherwise noted.

Symbol	Parameter	FDB088N08	Unit
V_{DSS}	Drain to Source Voltage	75	V
V_{GSS}	Gate to Source Voltage	± 20	V
I_D	Drain Current - Continuous ($T_C = 25^\circ\text{C}$, Silicon Limited) - Continuous ($T_C = 100^\circ\text{C}$, Silicon Limited) - Continuous ($T_C = 25^\circ\text{C}$, Package Limited)	85	A
		60	A
		120	A
I_{DM}	Drain Current - Pulsed (Note 1)	340	A
E_{AS}	Single Pulsed Avalanche Energy (Note 2)	309	mJ
dv/dt	Peak Diode Recovery dv/dt (Note 3)	10	V/ns
P_D	Power Dissipation ($T_C = 25^\circ\text{C}$) - Derate above 25°C	160	W
		1.06	W/ $^\circ\text{C}$
T_J, T_{STG}	Operating and Storage Temperature Range	-55 to +175	$^\circ\text{C}$
T_L	Maximum Lead Temperature for Soldering, 1/8" from Case for 5 Seconds	300	$^\circ\text{C}$

Thermal Characteristics

Symbol	Parameter	FDB088N08	Unit
$R_{\theta JC}$	Thermal Resistance, Junction to Case, Max.	0.94	$^\circ\text{C/W}$
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient (Minimum Pad of 2-oz Copper), Max.	62.5	
	Thermal Resistance, Junction to Ambient (1 in ² Pad of 2-oz Copper), Max.	40	

Package Marking and Ordering Information

Part Number	Top Mark	Package	Packing Method	Reel Size	Tape Width	Quantity
FDB088N08	FDB088N08	D ² -PAK	Tape and Reel	330 mm	24 mm	800 units

Electrical Characteristics $T_C = 25^\circ\text{C}$ unless otherwise noted.

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
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Off Characteristics

BV_{DSS}	Drain to Source Breakdown Voltage	$I_D = 250\ \mu\text{A}$, $V_{GS} = 0\ \text{V}$, $T_C = 25^\circ\text{C}$	75	-	-	V
$\Delta BV_{DSS} / \Delta T_J$	Breakdown Voltage Temperature Coefficient	$I_D = 250\ \mu\text{A}$, Referenced to 25°C	-	0.07	-	$V/^\circ\text{C}$
I_{DSS}	Zero Gate Voltage Drain Current	$V_{DS} = 75\ \text{V}$, $V_{GS} = 0\ \text{V}$	-	-	1	μA
		$V_{DS} = 75\ \text{V}$, $T_C = 150^\circ\text{C}$	-	-	500	
I_{GSS}	Gate to Body Leakage Current	$V_{GS} = \pm 20\ \text{V}$, $V_{DS} = 0\ \text{V}$	-	-	± 100	nA

On Characteristics

$V_{GS(th)}$	Gate Threshold Voltage	$V_{GS} = V_{DS}$, $I_D = 250\ \mu\text{A}$	2.0	-	4.0	V
$R_{DS(on)}$	Static Drain to Source On Resistance	$V_{GS} = 10\ \text{V}$, $I_D = 75\ \text{A}$	-	7.3	8.8	m Ω
g_{FS}	Forward Transconductance	$V_{DS} = 10\ \text{V}$, $I_D = 37.5\ \text{A}$	-	300	-	S

Dynamic Characteristics

C_{iss}	Input Capacitance	$V_{DS} = 25\ \text{V}$, $V_{GS} = 0\ \text{V}$, $f = 1\ \text{MHz}$	-	4960	6595	pF
C_{oss}	Output Capacitance		-	355	470	pF
C_{rss}	Reverse Transfer Capacitance		-	200	300	pF
$Q_g(tot)$	Total Gate Charge at 10V	$V_{DS} = 60\ \text{V}$, $I_D = 75\ \text{A}$, $V_{GS} = 10\ \text{V}$ (Note 4)	-	91	118	nC
Q_{gs}	Gate to Source Gate Charge		-	22	-	nC
Q_{gd}	Gate to Drain "Miller" Charge		-	28	-	nC
R_G	Gate Resistance	$f = 1\ \text{MHz}$	-	-	4	Ω

Switching Characteristics

$t_{d(on)}$	Turn-On Delay Time	$V_{DD} = 37.5\ \text{V}$, $I_D = 75\ \text{A}$, $R_G = 25\ \Omega$, $V_{GS} = 10\ \text{V}$ (Note 4)	-	45	100	ns
t_r	Turn-On Rise Time		-	158	326	ns
$t_{d(off)}$	Turn-Off Delay Time		-	244	498	ns
t_f	Turn-Off Fall Time		-	102	214	ns

Drain-Source Diode Characteristics

I _S	Maximum Continuous Drain to Source Diode Forward Current	-	-	85	A	
I _{SM}	Maximum Pulsed Drain to Source Diode Forward Current	-	-	340	A	
V _{SD}	Drain to Source Diode Forward Voltage	V _{GS} = 0 V, I _{SD} = 75 A	-	-	1.25	V
t _{rr}	Reverse Recovery Time	V _{GS} = 0 V, I _{SD} = 75 A, dI _F /dt = 100 A/μs	-	41.1	-	ns
Q _{rr}	Reverse Recovery Charge		-	80.7	-	nC

Notes:

1. Repetitive rating: pulse-width limited by maximum junction temperature.
2. $L = 0.11\ \text{mH}$, $I_{AS} = 75\ \text{A}$, $V_{DD} = 50\ \text{V}$, $R_G = 25\ \Omega$, starting $T_J = 25^\circ\text{C}$.
3. $I_{SD} \leq 75\ \text{A}$, $di/dt \leq 200\ \text{A}/\mu\text{s}$, $V_{DD} \leq BV_{DSS}$, starting $T_J = 25^\circ\text{C}$.
4. Essentially independent of operating temperature typical characteristics.

Typical Performance Characteristics

Figure 1. On-Region Characteristics

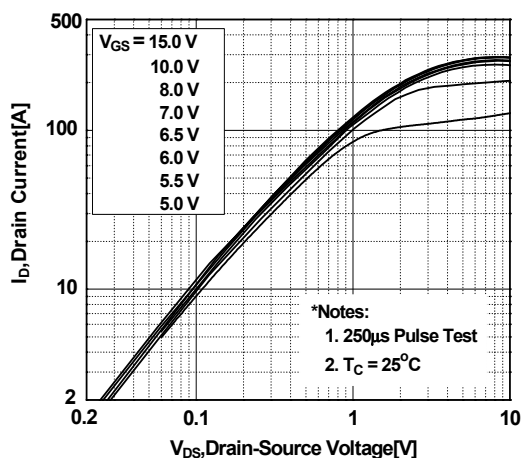


Figure 2. Transfer Characteristics

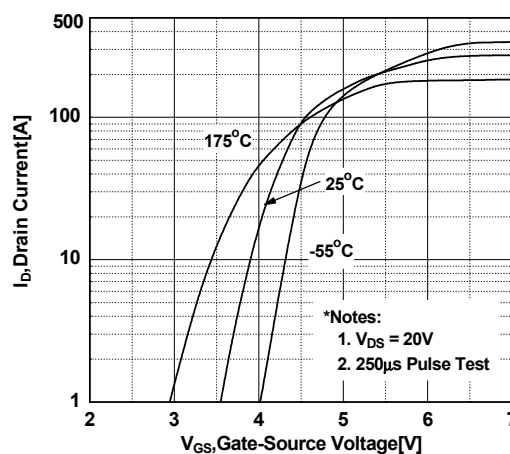


Figure 3. On-Resistance Variation vs. Drain Current and Gate Voltage

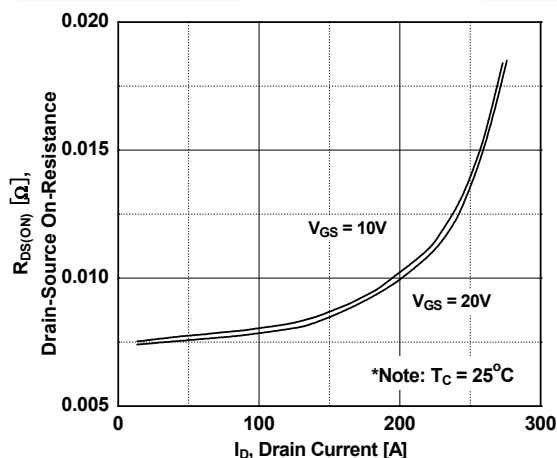


Figure 4. Body Diode Forward Voltage Variation vs. Source Current and Temperature

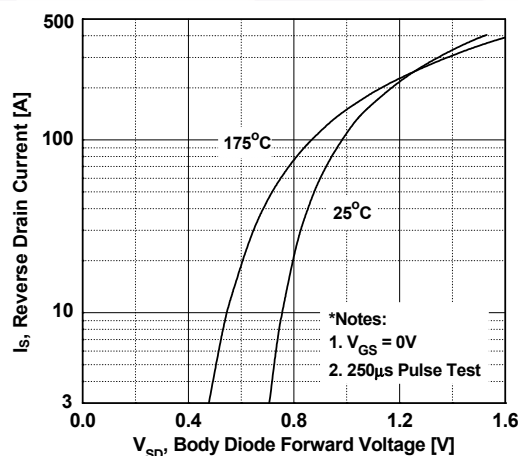


Figure 5. Capacitance Characteristics

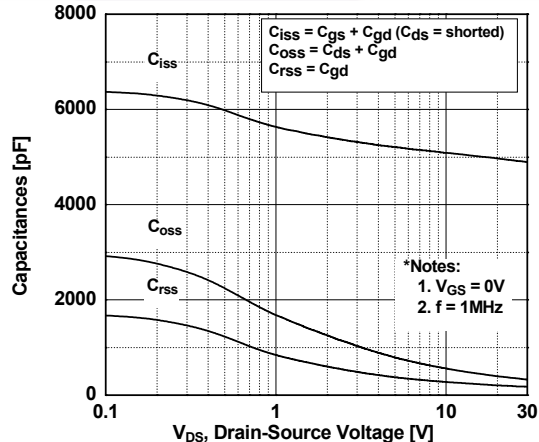
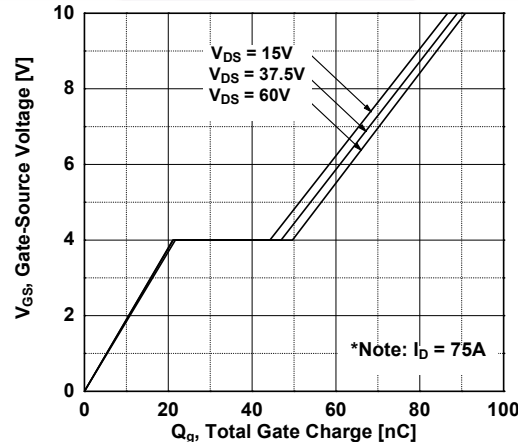


Figure 6. Gate Charge Characteristics



Typical Performance Characteristics (Continued)

Figure 7. Breakdown Voltage Variation vs. Temperature

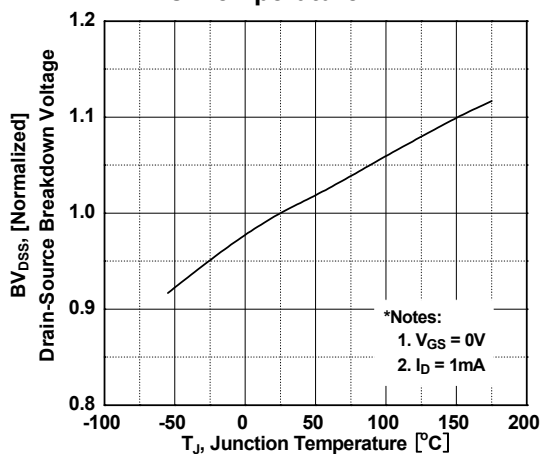


Figure 8. On-Resistance Variation vs. Temperature

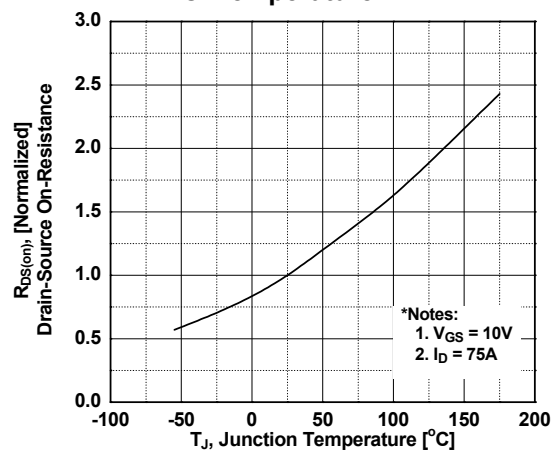


Figure 9. Maximum Safe Operating Area

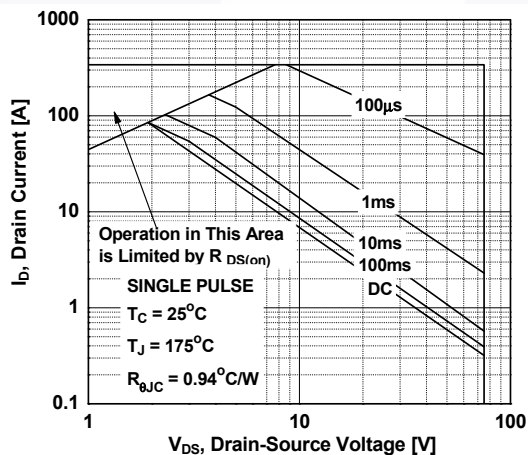


Figure 10. Maximum Drain Current vs. Case Temperature

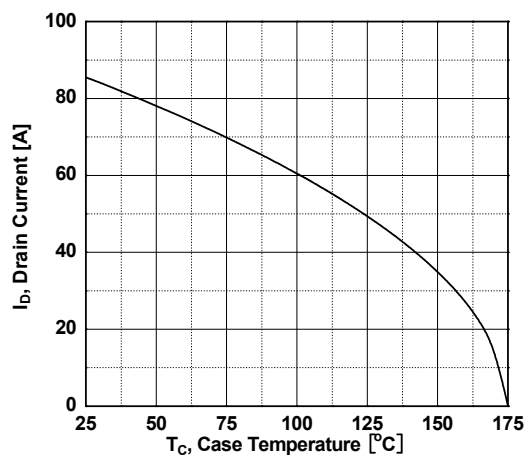
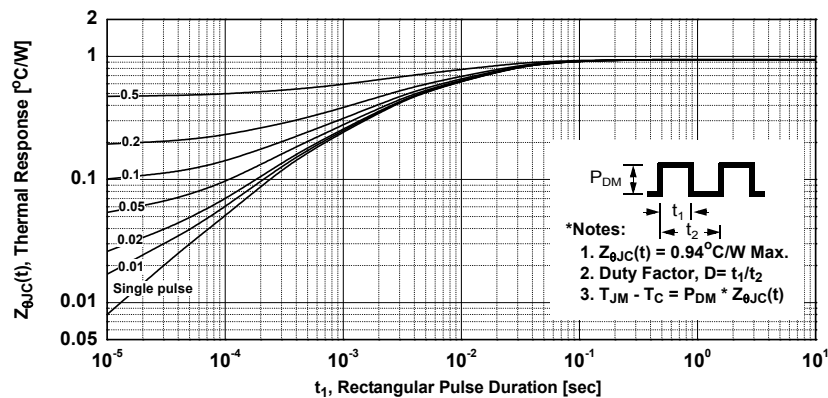


Figure 11. Transient Thermal Response Curve



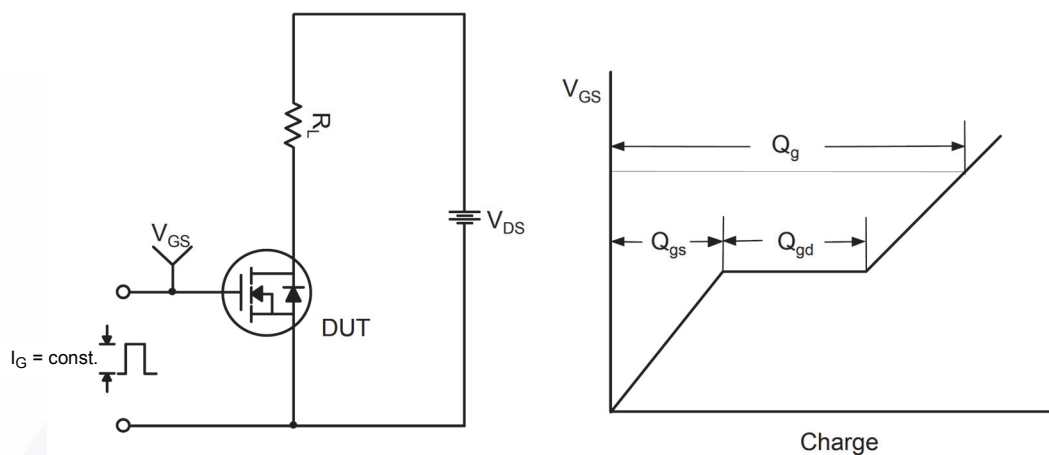


Figure 12. Gate Charge Test Circuit & Waveform

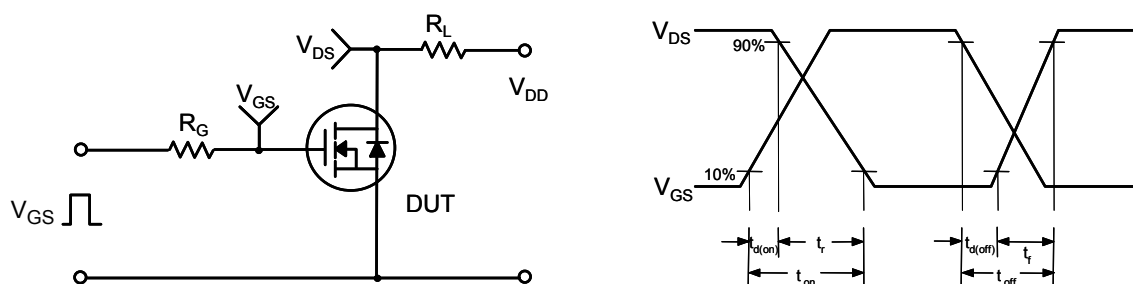


Figure 13. Resistive Switching Test Circuit & Waveforms

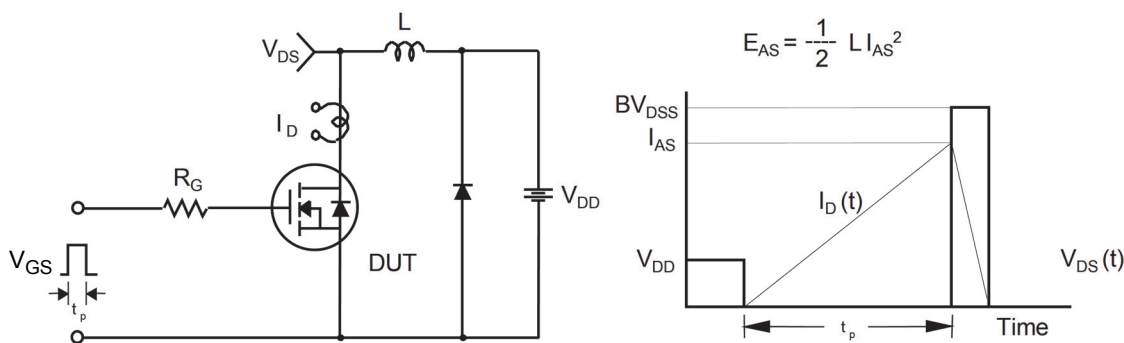


Figure 14. Unclamped Inductive Switching Test Circuit & Waveforms

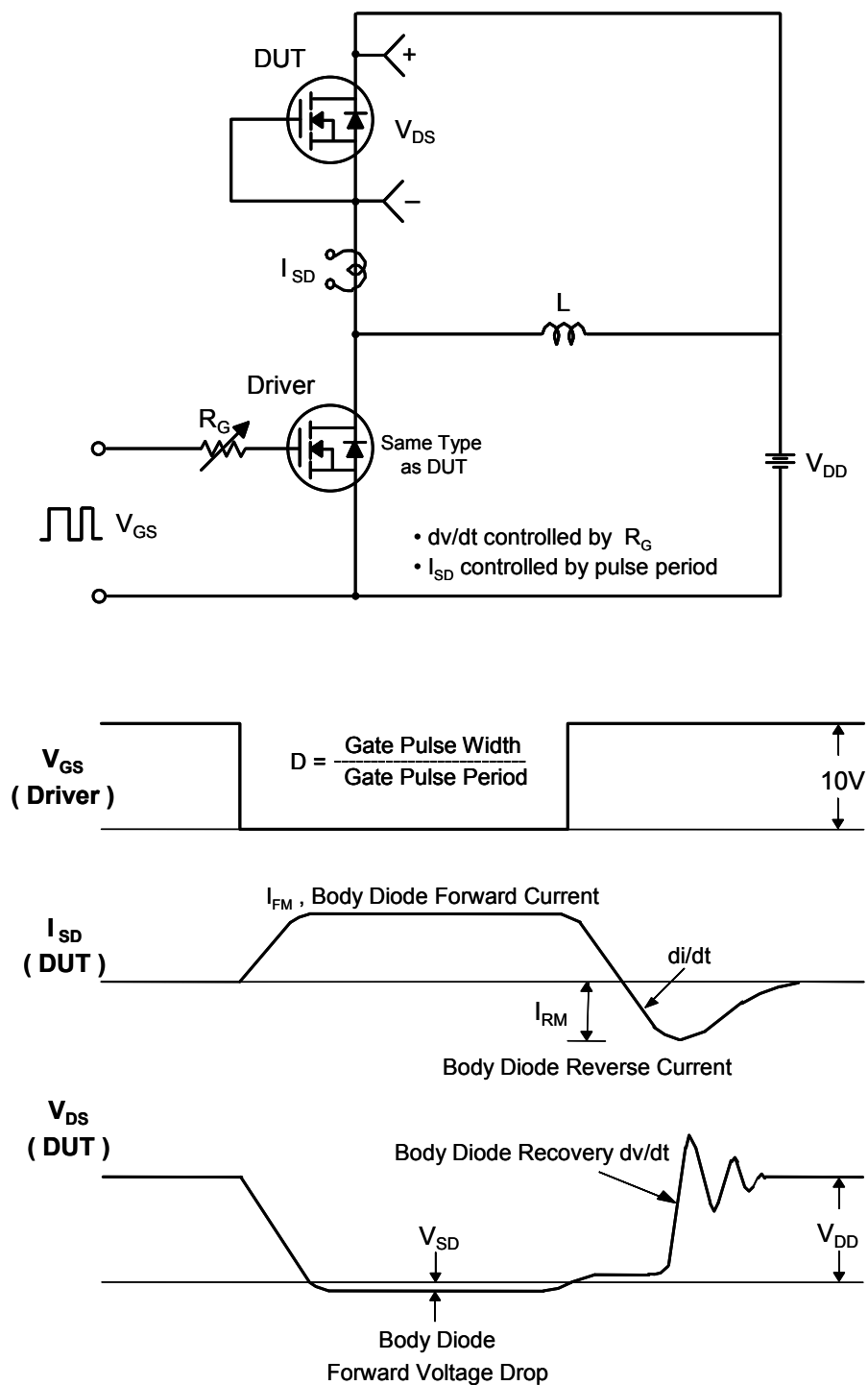


Figure 15. Peak Diode Recovery dv/dt Test Circuit & Waveforms

Mechanical Dimensions

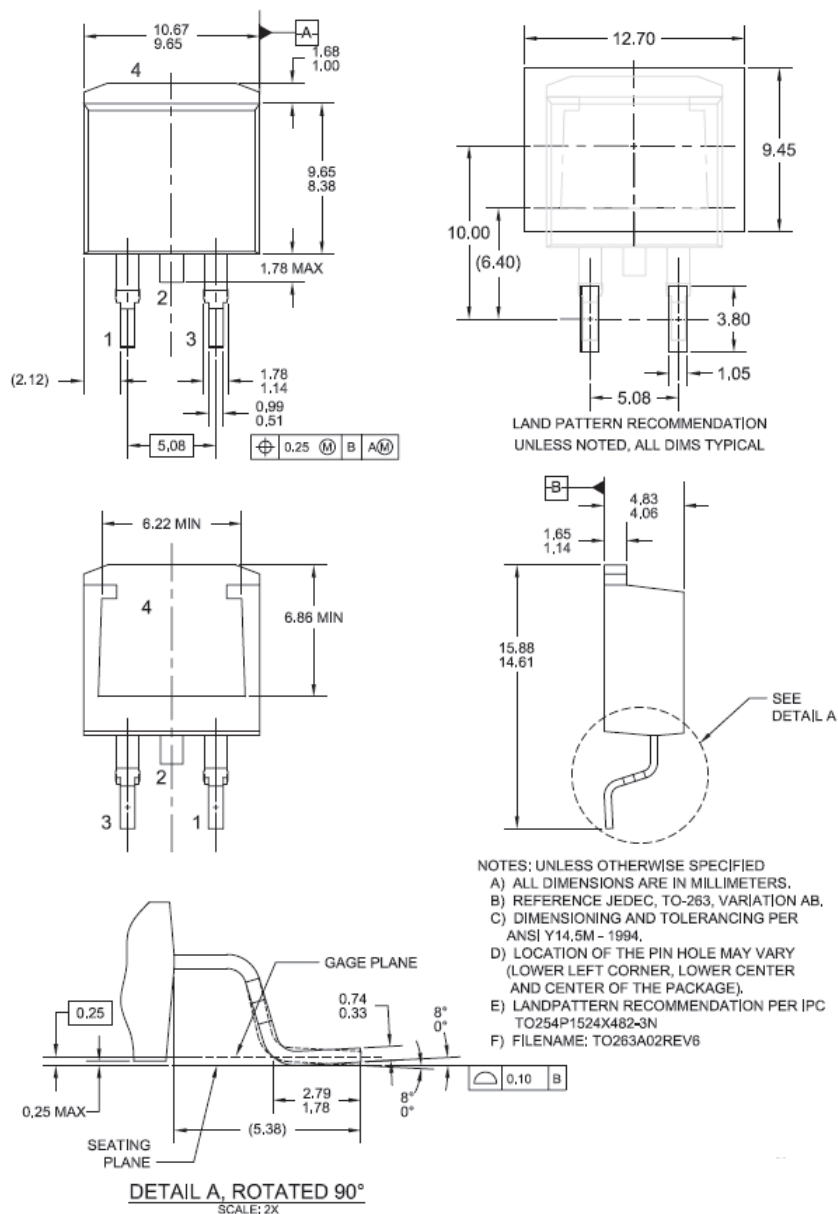


Figure 16. TO263 (D²PAK), Molded, 2-Lead, Surface Mount

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No Identification Needed	Full Production	Datasheet contains final specifications. Fairchild Semiconductor reserves the right to make changes at any time without notice to improve the design.
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