

8-Pin DIP Low Input Current High Gain Split Darlington Optocouplers

Single-Channel: 6N138M, 6N139M Dual-Channel: HCPL2730M, HCPL2731M

Description

The single-channel, 6N138M, 6N139M and dual-channel HCPL2730M, HCPL2731M optocouplers consist of an AlGaAs LED optically coupled to a high gain split darlington photodetector.

The split darlington configuration separating the input photodiode and the first stage gain from the output transistor permits lower output saturation voltage and higher speed operation than possible with conventional darlington phototransistor optocoupler. In the dual channel devices, HCPL2730M and HCPL2731M, an integrated emitter-base resistor provides superior stability over temperature.

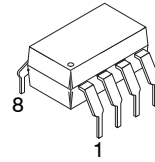
The combination of a very low input current of 0.5 mA and a high current transfer ratio of 2000% makes this family particularly useful for input interface to MOS, CMOS, LSTTL and EIA RS232C, while output compatibility is ensured to CMOS as well as high fan-out TTL requirements. An internal noise shield provides exceptional common mode rejection of 10 kV/ μ s.

Features

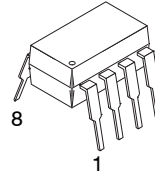
- Low Current – 0.5 mA
- Superior CTR – 2000%
- Superior CMR – 10 kV/ μ s
- CTR Guaranteed 0 to 70°C
- Dual Channel – HCPL2730M, HCPL2731M
- Safety and Regulatory Approvals
- UL1577, 5,000 VAC_{RMS} for 1 Minute
- DIN EN/IEC60747-5-5
- These are Pb-Free Devices

Applications

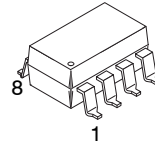
- Digital Logic Ground Isolation
- Telephone Ring Detector
- EIA-RS-232C Line Receiver
- High Common Mode Noise Line Receiver
- μ P Bus Isolation
- Current Loop Receiver



PDIP8 6.6x3.81, 2.54P
CASE 646BW

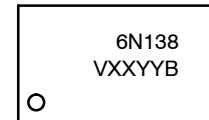


PDIP8 9.655x6.6, 2.54P
CASE 646CQ



PDIP8 GW
CASE 709AC

MARKING DIAGRAM



- | | |
|-------|---|
| 6N138 | = Device Number |
| V | = DIN EN/IEC60747-5-5 Option (only appears on component ordered with this option) |
| XX | = Two-Digit Year Code, e.g., '16' |
| YY | = Two-Digit Work Week, Ranging from '01' to '53' |
| B | = Assembly Package Code |

ORDERING INFORMATION

See detailed ordering and shipping information on page 11 of this data sheet.

Related Resources

- <https://www.onsemi.com/products/interfaces/high-performance-optocouplers/high-performance-transistor-optocouplers>
- <https://www.onsemi.com/products/interfaces/high-performance-optocouplers/high-performance-transistor-optocouplers/hcpl0700>
- <https://www.onsemi.com/products/interfaces/high-performance-optocouplers/high-performance-transistor-optocouplers/hcpl0731>

Single-Channel: 6N138M, 6N139M Dual-Channel: HCPL2730M, HCPL2731M

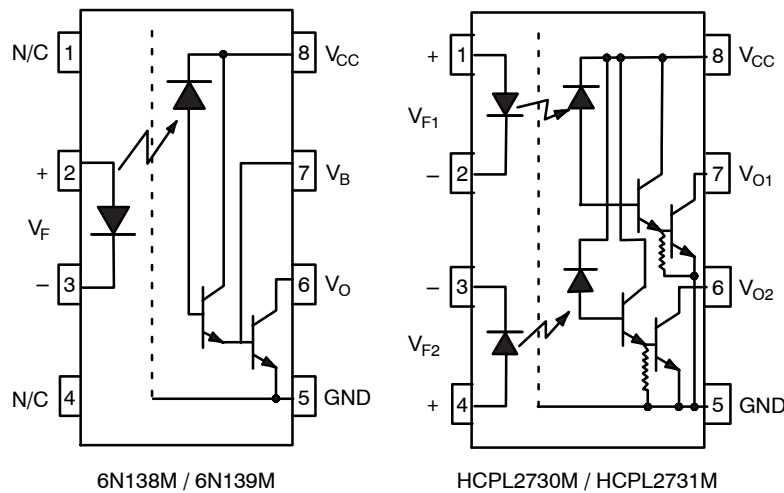


Figure 1. Schematics

SAFETY AND INSULATION RATINGS (As per DIN EN/IEC 60747-5-5, this optocoupler is suitable for “safe electrical insulation” only within the safety limit data. Compliance with the safety ratings shall be ensured by means of protective circuits.)

Parameter		Characteristics
Installation Classifications per DIN VDE 0110/1.89 Table 1, For Rated Mains Voltage	<150 V _{RMS}	I–IV
	<300 V _{RMS}	I–IV
	<450 V _{RMS}	I–III
	<600 V _{RMS}	I–III
	<1,000 V _{RMS} (Option T, TS)	I–III
Climatic Classification		40/100/21
Pollution Degree (DIN VDE 0110/1.89)		2
Comparative Tracking Index		175

Symbol	Parameter	Value	Unit
V _{PR}	Input-to-Output Test Voltage, Method A, V _{IORM} x 1.6 = V _{PR} , Type and Sample Test with t _m = 10 s, Partial Discharge < 5 pC	2,262	V _{peak}
	Input-to-Output Test Voltage, Method B, V _{IORM} x 1.875 = V _{PR} , 100% Production Test with t _m = 1 s, Partial Discharge < 5 pC	2,651	V _{peak}
V _{IORM}	Maximum Working Insulation Voltage	1,414	V _{peak}
V _{IOTM}	Highest Allowable Over-Voltage	6,000	V _{peak}
	External Creepage	≥8.0	mm
	External Clearance	≥7.4	mm
	External Clearance (for Option TV, 0.4" Lead Spacing)	≥10.16	mm
DTI	Distance Through Insulation (Insulation Thickness)	≥0.5	mm
T _S	Case Temperature (Note 1)	150	°C
I _{S,INPUT}	Input Current (Note 1)	200	mA
P _{S,OUTPUT}	Output Power (Duty Factor ≤ 2.7%) (Note 1)	300	mW
R _{IO}	Insulation Resistance at T _S , V _{IO} = 500 V (Note 1)	>10 ⁹	Ω

1. Safety limit value – maximum values allowed in the event of a failure.

Single-Channel: 6N138M, 6N139M Dual-Channel: HCPL2730M, HCPL2731M

ABSOLUTE MAXIMUM RATINGS (T_A = 25°C unless otherwise noted)

Symbol	Parameter	Device	Value	Unit
T _{STG}	Storage Temperature		–40 to +125	°C
T _{OPR}	Operating Temperature		–40 to +100	°C
T _J	Junction Temperature		–40 to +125	°C
T _{SOL}	Lead Solder Temperature		260 for 10 s	°C

EMITTER

I _F (avg)	DC/Average Forward Input Current Per Channel	All	20	mA
I _F (pk)	Peak Forward Input Current Per Channel (50% Duty Cycle, 1 ms P.W.)	All	40	mA
I _F (trans)	Peak Transient Input Current Per Channel (≤1 μs P.W., 300 pps)	All	1	A
V _R	Reverse Input Voltage Per Channel	All	5	V
P _D	Input Power Dissipation Per Channel (Note 2)	All	35	mW

DETECTOR

I _O (avg)	Average Output Current Per Channel	All	60	mA
V _{ER}	Emitter–Base Reverse Voltage	6N138M, 6N139M	0.5	V
V _{CC} , V _O	Supply Voltage, Output Voltage	6N138M, HCPL2730M	–0.5 to 7.0	V
		6N139M, HCPL2731M	–0.5 to 18.0	
P _O	Output Power Dissipation Per Channel	All	100	mW

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

2. No derating required for devices operated within the T_{OPR} specification (6N138M and 6N139M only).



Single-Channel: 6N138M, 6N139M Dual-Channel: HCPL2730M, HCPL2731M

ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Device	Test Conditions	Min	Typ	Max	Unit
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INDIVIDUAL COMPONENT CHARACTERISTICS ($V_{CC} = 5.0\text{ V}$, $T_A = 0^\circ\text{C}$ to 70°C unless otherwise specified. Typical value is measured at $T_A = 25^\circ\text{C}$.)

EMITTER								
V _F	Input Forward Voltage	All	I _F = 1.6 mA, T _A = 25°C		–	1.30	1.70	V
			I _F = 1.6 mA		–	–	1.75	
BV _R	Input Reverse Breakdown Voltage	All	I _R = 10 μA, T _A = 25°C		5.0	19.0	–	V
ΔV _F / ΔT _A	Temperature Coefficient of Forward Voltage	All	I _F = 1.6 mA		–	–1.94	–	mV/°C
DETECTOR								
I _{CCL}	Logic Low Supply Current	6N138M, 6N139M	I _F = 1.6 mA, V _O = Open, V _{CC} = 18 V		–	0.4	1.5	mA
		HCPL2730M	V _{CC} = 7 V	I _{F1} = I _{F2} = 1.6 mA, V _{O1} = V _{O2} = Open	–	1.25	3	
		HCPL2731M	V _{CC} = 18 V					
I _{CCH}	Logic High Supply Current	6N138M, 6N139M	I _F = 0 mA, V _O = Open, V _{CC} = 18 V		–	0.0003	10	μA
		HCPL2730M	V _{CC} = 7 V	I _{F1} = I _{F2} = 0 mA, V _{O1} = V _{O2} = Open	–	0.0003	20	
		HCPL2731M	V _{CC} = 18 V					

TRANSFER CHARACTERISTICS

COUPLED							
CTR	Current Transfer Ratio (Note 3) (Note 4)	6N138M	$I_F = 1.6\text{ mA}$, $V_O = 0.4\text{ V}$, $V_{CC} = 4.5\text{ V}$	300	1600	–	%
		HCPL2730M			2400		
		6N139M	$I_F = 0.5\text{ mA}$, $V_O = 0.4\text{ V}$, $V_{CC} = 4.5\text{ V}$	400	2000	–	
		HCPL2731M			3500		
		6N139M	$I_F = 1.6\text{ mA}$, $V_O = 0.4\text{ V}$, $V_{CC} = 4.5\text{ V}$	500	1600	–	
		HCPL2731M			2400		
I_{OH}	Logic High Output Current	6N138M	$I_F = 0\text{ mA}$, $V_O = V_{CC} = 7\text{ V}$	–	0.001	250	μA
		HCPL2730M					
		6N139M	$I_F = 0\text{ mA}$, $V_O = V_{CC} = 18\text{ V}$	–	0.0036	100	
		HCPL2731M					
V_{OL}	Logic Low Output Voltage (Note 4)	6N138M	$I_F = 1.6\text{ mA}$, $I_O = 4.8\text{ mA}$, $V_{CC} = 4.5\text{ V}$	–	0.06	0.4	V
		HCPL2730M			0.05		
		6N139M	$I_F = 0.5\text{ mA}$, $I_O = 2\text{ mA}$, $V_{CC} = 4.5\text{ V}$	–	0.05	0.4	
		6N139M	$I_F = 1.6\text{ mA}$, $I_O = 8\text{ mA}$, $V_{CC} = 4.5\text{ V}$	–	0.093	0.4	
		HCPL2731M			0.08		
		6N139M	$I_F = 5\text{ mA}$, $I_O = 15\text{ mA}$, $V_{CC} = 4.5\text{ V}$	–	0.13	0.4	
		HCPL2731M			0.12		
		6N139M	$I_F = 12\text{ mA}$, $I_O = 24\text{ mA}$, $V_{CC} = 4.5\text{ V}$	–	0.18	0.4	
		HCPL2731M			0.17		

Single-Channel: 6N138M, 6N139M Dual-Channel: HCPL2730M, HCPL2731M

ELECTRICAL CHARACTERISTICS (continued)

Symbol	Parameter	Device	Test Conditions	Min	Typ	Max	Unit
SWITCHING CHARACTERISTICS ($V_{CC} = 5.0\text{ V}$, $T_A = 0^\circ\text{C}$ to 70°C unless otherwise specified. Typical value is measured at $T_A = 25^\circ\text{C}$.)							
t_{PHL}	Propagation Delay Time to Logic LOW (Note 4) (Figure 14)	6N139M	$R_L = 270\ \Omega$, $I_F = 12\text{ mA}$	–	0.2	2	μs
		HCPL2730M, HCPL2731M	$R_L = 270\ \Omega$, $I_F = 12\text{ mA}$	–	0.5	3	
		6N138M	$R_L = 2.2\text{ k}\Omega$, $I_F = 1.6\text{ mA}$	–	1.0	15	
		HCPL2730M, HCPL2731M	$R_L = 2.2\text{ k}\Omega$, $I_F = 1.6\text{ mA}$	–	2.5	25	
		6N139M	$R_L = 4.7\text{ k}\Omega$, $I_F = 0.5\text{ mA}$	–	2.5	30	
		HCPL2731M	$R_L = 4.7\text{ k}\Omega$, $I_F = 0.5\text{ mA}$	–	8.4	120	
t_{PLH}	Propagation Delay Time to Logic HIGH (Note 4) (Figure 14)	6N139M	$R_L = 270\ \Omega$, $I_F = 12\text{ mA}$	–	1.3	10	μs
		HCPL2730M, HCPL2731M	$R_L = 270\ \Omega$, $I_F = 12\text{ mA}$	–	1.0	15	
		6N138M, HCPL2730M, HCPL2731M	$R_L = 2.2\text{ k}\Omega$, $I_F = 1.6\text{ mA}$	–	7.3	50	
		6N139M, HCPL2731M	$R_L = 4.7\text{ k}\Omega$, $I_F = 0.5\text{ mA}$	–	13.6	90	
$ CM_H $	Common Mode Transient Immunity at Logic High (Note 5) (Figure 15)	All	$I_F = 0\text{ mA}$, $ V_{CM} = 10\text{ V}_{P-P}$, $R_L = 2.2\text{ k}\Omega$, $T_A = 25^\circ\text{C}$	1,000	10,000	–	$\text{V}/\mu\text{s}$
$ CM_L $	Common Mode Transient Immunity at Logic Low (Note 5) (Figure 15)	All	$I_F = 1.6\text{ mA}$, $ V_{CM} = 10\text{ V}_{P-P}$, $R_L = 2.2\text{ k}\Omega$, $T_A = 25^\circ\text{C}$	1,000	10,000	–	$\text{V}/\mu\text{s}$

ISOLATION CHARACTERISTICS ($T_A = 25^\circ\text{C}$ unless otherwise specified.)

V_{ISO}	Withstand Insulation Test Voltage (Note 6) (Note 7)	All	$RH \leq 50\%$, $T_A = 25^\circ\text{C}$, $I_{I-O} \leq 10\ \mu\text{A}$, $t = 1\text{ min}$, $f = 50\text{ Hz}$	5,000	–	–	VAC_{RMS}
R_{I-O}	Resistance (Input to Output) (Note 6)	All	$V_{I-O} = 500\text{ V}_{DC}$	–	10^{11}	–	Ω
C_{I-O}	Capacitance (Input to Output) (Note 6) (Note 8)	All	$f = 1\text{ MHz}$, $V_{I-O} = 0\text{ V}$	–	1	–	pF
I_{I-I}	Input–Input Insulation Leakage Current (Note 9)	HCPL2730M, HCPL2731M	$RH \leq 45\%$, $V_{I-I} = 500\text{ V}_{DC}$, $t = 5\text{ s}$	–	0.005	–	μA
R_{I-I}	Input–Input Resistance (Note 9)	HCPL2730M, HCPL2731M	$V_{I-I} = 500\text{ V}_{DC}$	–	10^{11}	–	Ω
C_{I-I}	Input–Input Capacitance (Note 9)	HCPL2730M, HCPL2731M	$f = 1\text{ MHz}$	–	0.03	–	pF

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

- Current Transfer Ratio is defined as a ratio of output collector current, I_O , to the forward LED input current, I_F , times 100%.
- Pin 7 open. (6N138M and 6N139M only)
- Common mode transient immunity in logic HIGH level is the maximum tolerable (positive) dV_{CM}/dt on the leading edge of the common mode pulse signal V_{CM} , to assure that the output will remain in a logic HIGH state (i.e., $V_O > 2.0\text{ V}$). Common mode transient immunity in logic LOW level is the maximum tolerable (negative) dV_{CM}/dt on the trailing edge of the common mode pulse signal, V_{CM} , to assure that the output will remain in a logic LOW state (i.e., $V_O < 0.8\text{ V}$).
- Device is considered a two terminal device: Pins 1, 2, 3 and 4 are shorted together and Pins 5, 6, 7 and 8 are shorted together.
- 5000 VAC_{RMS} for 1 minute duration is equivalent to 6000 VAC_{RMS} for 1 second duration.
- For dual channel devices, C_{I-O} is measured by shorting pins 1 and 2 or pins 3 and 4 together and pins 5 through 8 shorted together.
- Measured between pins 1 and 2 shorted together, and pins 3 and 4 shorted together.

Single-Channel: 6N138M, 6N139M Dual-Channel: HCPL2730M, HCPL2731M

ELECTRICAL CHARACTERISTICS (continued)

(T_A = 25°C unless otherwise specified.)

Current Limiting Resistor Calculations:

$$R_1 \text{ (Non-Invert)} = \frac{V_{CC1} - V_{DF} - V_{OL1}}{I_F} \quad (\text{eq. 1})$$

$$R_1 \text{ (Invert)} = \frac{V_{CC1} - V_{OH1} - V_{DF}}{I_F} \quad (\text{eq. 2})$$

$$R_2 = \frac{V_{CC2} - V_{OLX} (@ I_L - I_2)}{I_L} \quad (\text{eq. 3})$$

Where:

V_{CC1} = Input Supply Voltage

V_{CC2} = Output Supply Voltage

V_{DF} = Diode Forward Voltage

V_{OL1} = Logic "0" Voltage of Driver

V_{OH1} = Logic "1" Voltage of Driver

I_F = Diode Forward Current

V_{OLX} = Saturation Voltage of Output Transistor

I_L = Load Current Through Resistor R₂

I₂ = Input Current of Output Gate

INPUT CONFIGURATION		R ₁ (Ω)	R ₂ (Ω) @ OUTPUT CONFIGURATION						
			CMOS @ 5 V	CMOS @ 10 V	74XX	74LXX	74SXX	74LSXX	74HXX
CMOS @ 5 V	NON-INV.	2000	1000	2200	750	1000	1000	1000	560
	INV.	510							
CMOS @ 10 V	NON-INV.	5100							
	INV.	4700							
74XX	NON-INV.	2200							
	INV.	180							
74LXX	NON-INV.	1800							
	INV.	100							
74SXX	NON-INV.	2000							
	INV.	360							
74LSXX	NON-INV.	2000							
	INV.	180							
74HXX	NON-INV.	2000							
	INV.	180							

Figure 2. Resistor Values for Logic Interface

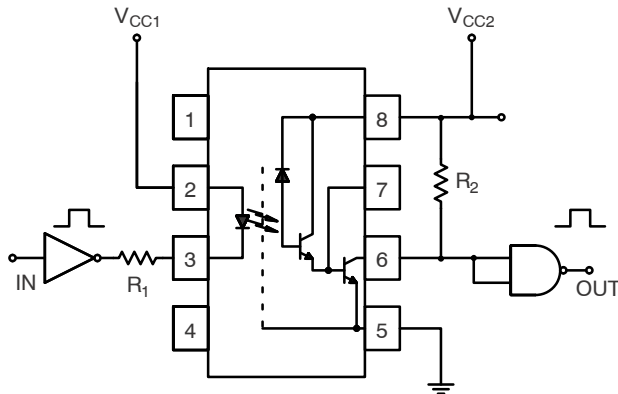


Figure 3. Non-Inverting Logic Interface

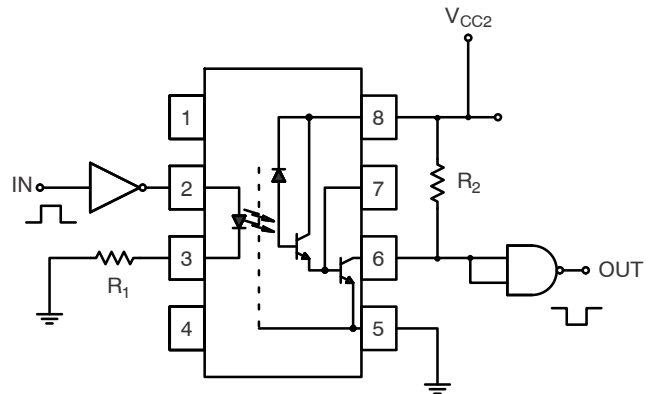


Figure 4. Inverting Logic Interface

Typical Performance Curves

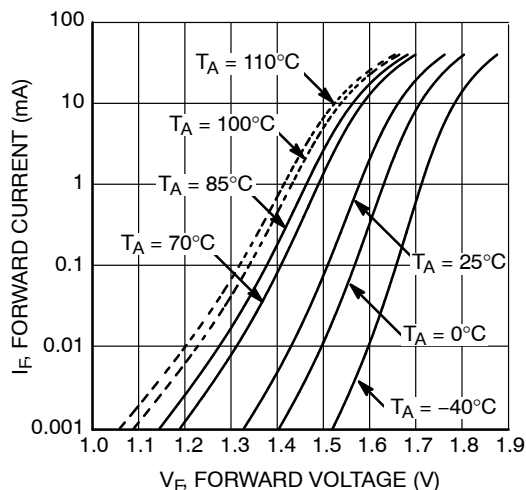


Figure 5. LED Forward Current vs. Forward Voltage

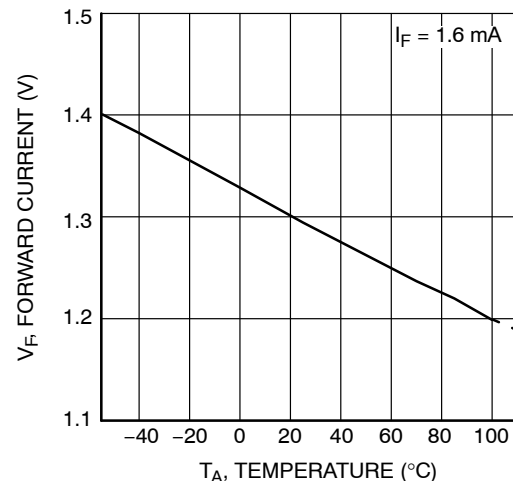


Figure 6. LED Forward Current vs. Temperature

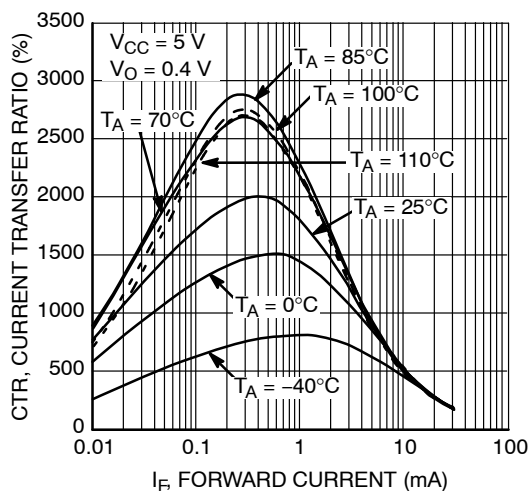


Figure 7. Current Transfer Ratio vs. Forward Current (6N138M / 6N139M Only)

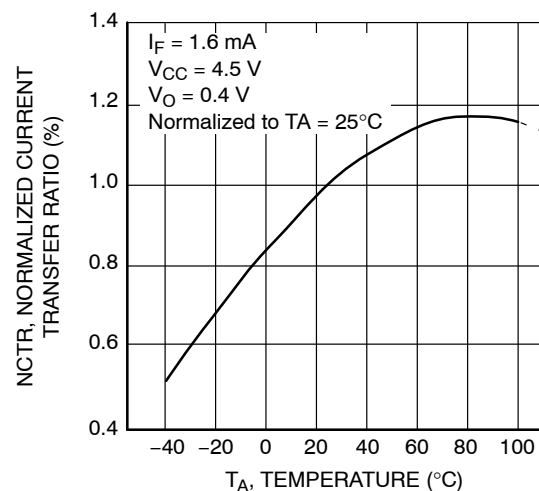


Figure 8. Normalized Current Transfer Ratio vs. Ambient Temperature (6N138M / 6N139M Only)

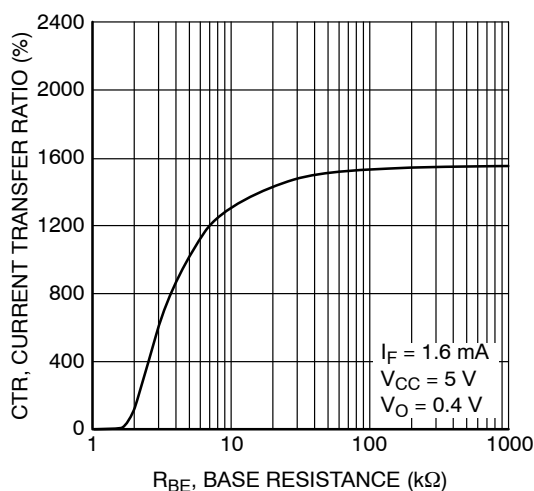


Figure 9. Current Transfer Ratio vs. Base-Emitter Resistance (6N138M / 6N139M Only)

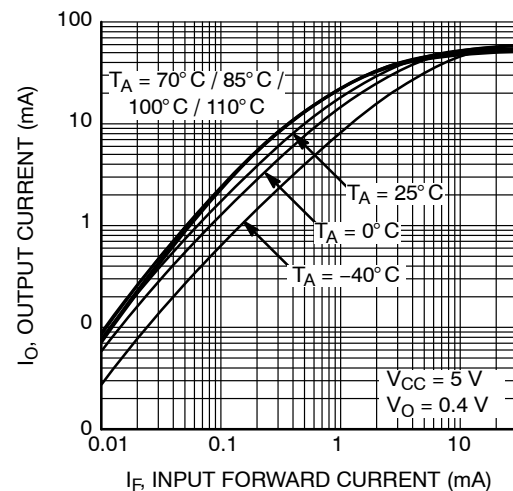


Figure 10. Output Current vs. Input Diode Forward Current (6N138M / 6N139M Only)

Typical Performance Curves (continued)

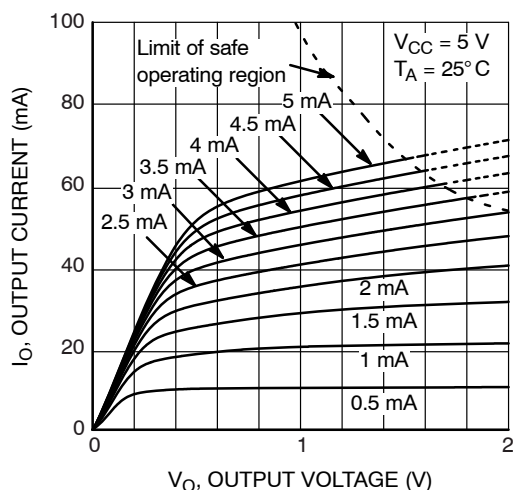


Figure 11. Output Current vs Output Voltage (6N138M / 6N139M Only)

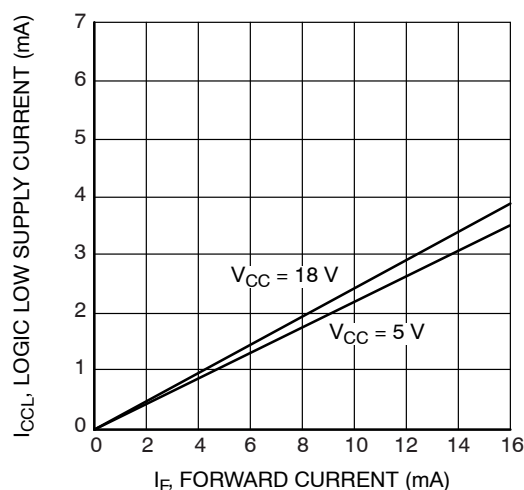


Figure 12. Logic Low Supply Current vs. Input Diode Forward Current (6N138M / 6N139M Only)

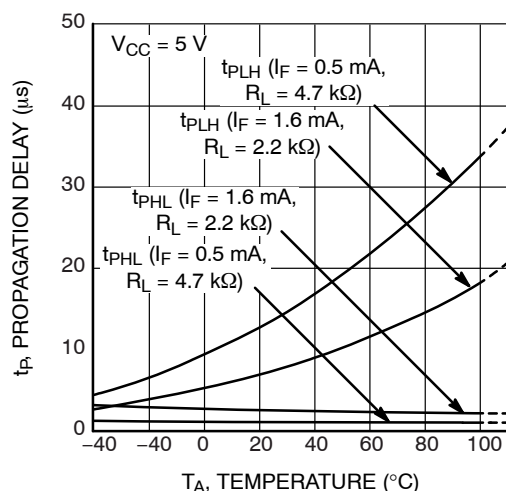
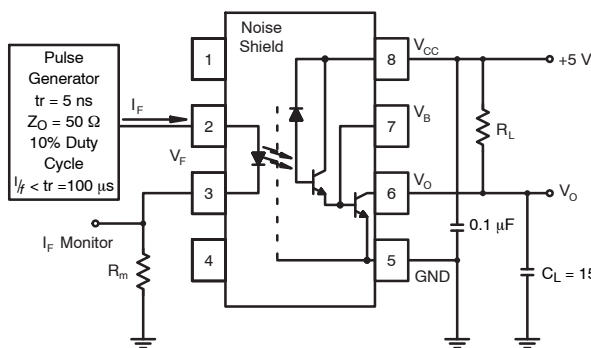


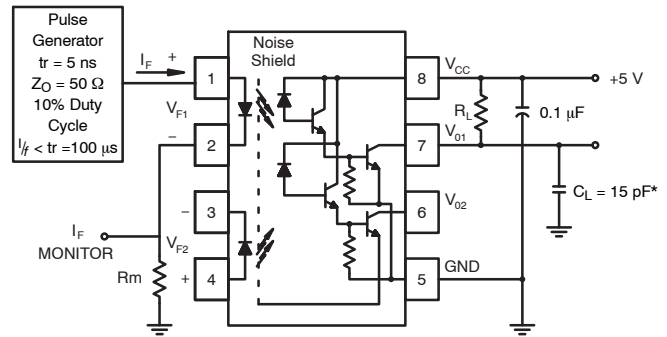
Figure 13. Propagation Delay vs. Temperature (6N138M / 6N139M Only)

Single-Channel: 6N138M, 6N139M Dual-Channel: HCPL2730M, HCPL2731M

Test Circuits



Test Circuit for 6N138M, 6N139M



Test Circuit for HCPL2730M and HCPL2731M

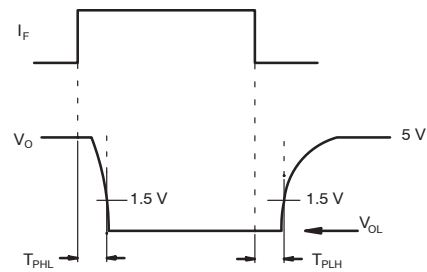
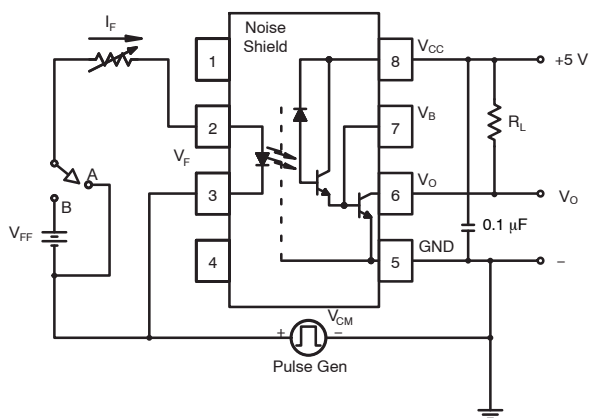
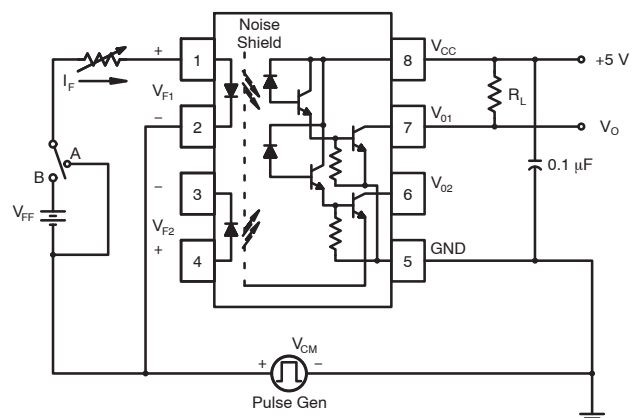


Figure 14. Switching Time Test Circuit



Test Circuit for 6N138M and 6N139M



Test Circuit for HCPL2730M and HCPL2731M

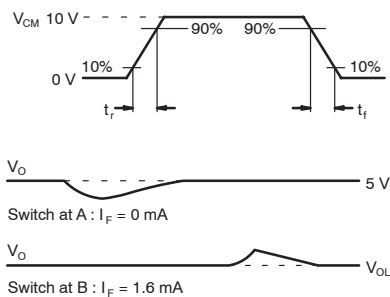
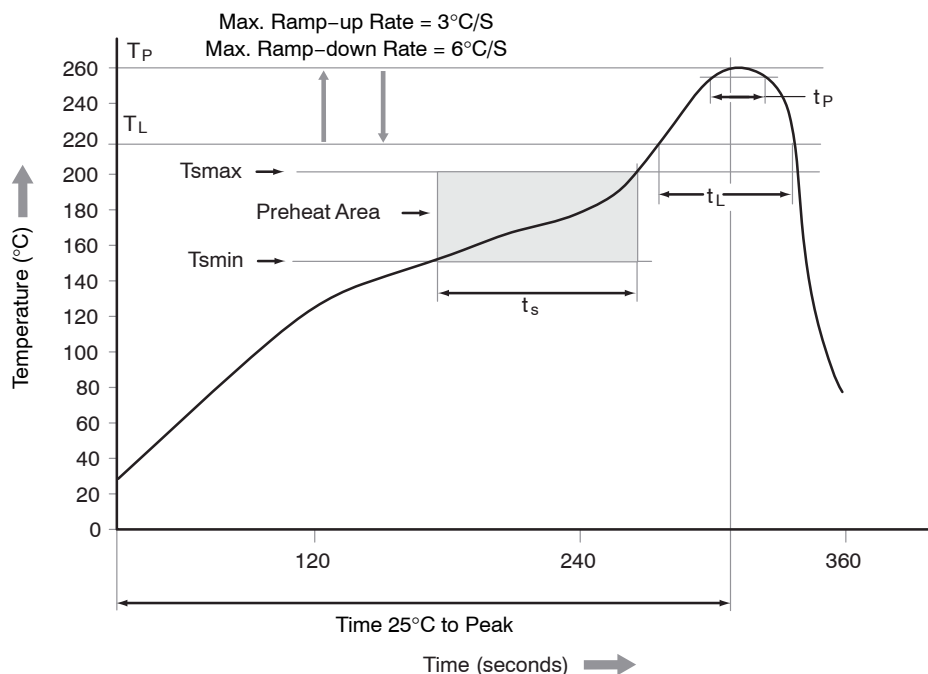


Figure 15. Common Mode Immunity Test Circuit

Reflow Profile



Profile Feature	Pb-Free Assembly Profile
Temperature Min. (Tsmmin)	150°C
Temperature Max. (Tsmmax)	200°C
Time (t _s) from (Tsmmin to Tsmmax)	60 – 120 seconds
Ramp-up Rate (t _L to t _P)	3°C/second max.
Liquidous Temperature (T _L)	217°C
Time (t _L) Maintained Above (T _L)	60 – 150 seconds
Peak Body Package Temperature	260°C +0°C / -5°C
Time (t _P) within 5°C of 260°C	30 seconds
Ramp-down Rate (T _P to T _L)	6°C/second max.
Time 25°C to Peak Temperature	8 minutes max.

Figure 16. Reflow Profile

Single-Channel: 6N138M, 6N139M Dual-Channel: HCPL2730M, HCPL2731M

ORDERING INFORMATION

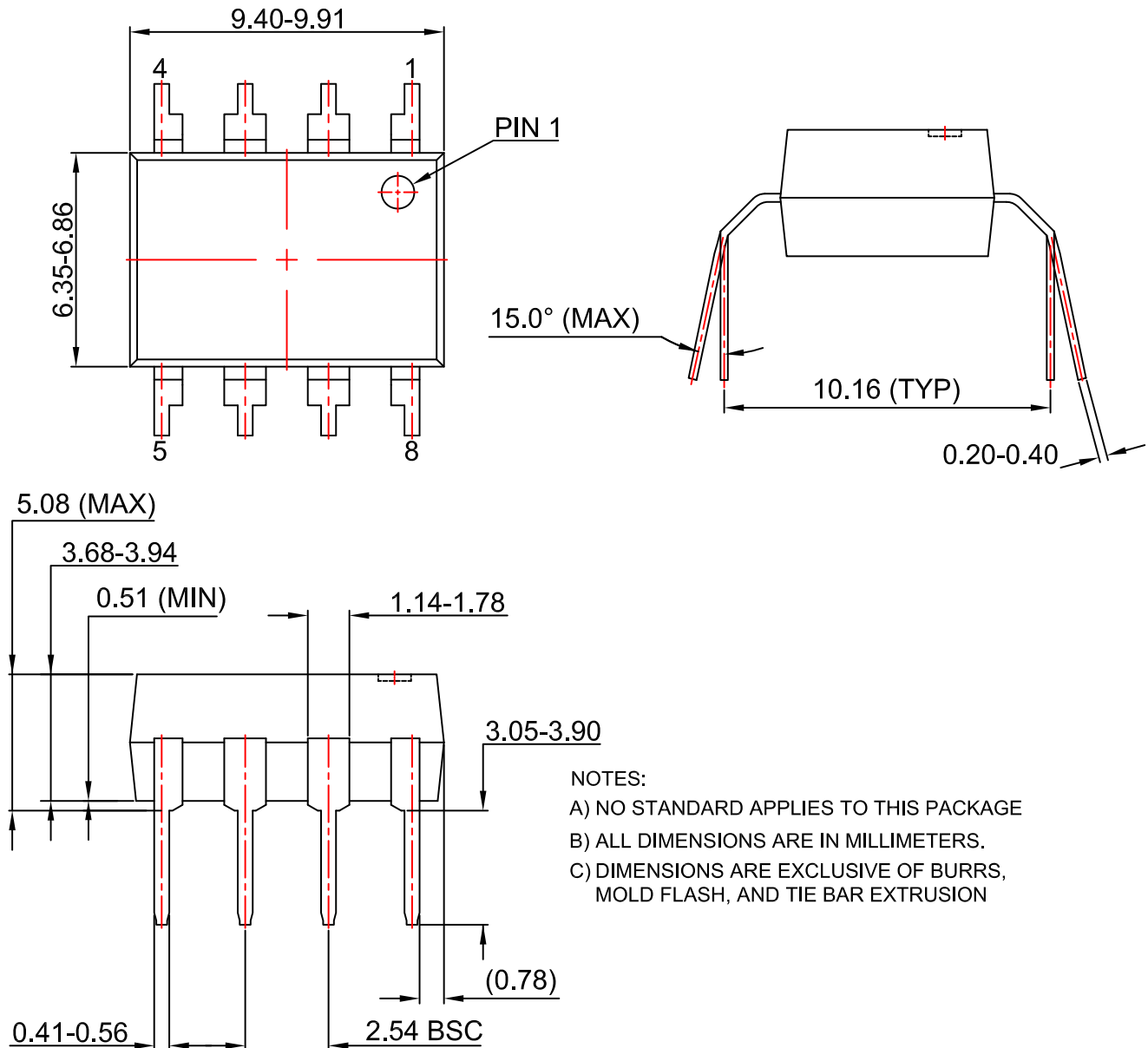
Part Number	Package	Shipping [†]
6N138M	DIP 8-Pin (Pb-Free)	50 Units / Tube
6N138SM	SMT 8-Pin (Lead Bend) (Pb-Free)	50 Units / Tube
6N138SDM	SMT 8-Pin (Lead Bend) (Pb-Free)	1,000 Units / Tape & Reel
6N139M	DIP 8-Pin (Pb-Free)	50 Units / Tube
6N139SM	SMT 8-Pin (Lead Bend) (Pb-Free)	50 Units / Tube
6N139SDM	SMT 8-Pin (Lead Bend) (Pb-Free)	1,000 Units / Tape & Reel
6N139VM	DIP 8-Pin, DIN EN/IEC 60747-5-5 Option (Pb-Free)	50 Units / Tube
6N139SVM	SMT 8-Pin (Lead Bend), DIN EN/IEC 60747-5-5 Option (Pb-Free)	50 Units / Tube
6N139SDVM	SMT 8-Pin (Lead Bend), DIN EN/IEC 60747-5-5 Option (Pb-Free)	1,000 Units / Tape & Reel
6N139TVM	DIP 8-Pin, 0.4" Lead Spacing, DIN EN/IEC 60747-5-5 Option (Pb-Free)	50 Units / Tube
HCPL2730M	DIP 8-Pin (Pb-Free)	50 Units / Tube
HCPL2730SM	SMT 8-Pin (Lead Bend) (Pb-Free)	50 Units / Tube
HCPL2730SDM	SMT 8-Pin (Lead Bend) (Pb-Free)	1,000 Units / Tape & Reel
HCPL2731M	DIP 8-Pin (Pb-Free)	50 Units / Tube
HCPL2731SM	SMT 8-Pin (Lead Bend) (Pb-Free)	50 Units / Tube
HCPL2731SDM	SMT 8-Pin (Lead Bend) (Pb-Free)	1,000 Units / Tape & Reel
HCPL2731VM	DIP 8-Pin, DIN EN/IEC 60747-5-5 Option (Pb-Free)	50 Units / Tube

[†]For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.



PDIP8 6.6x3.81, 2.54P
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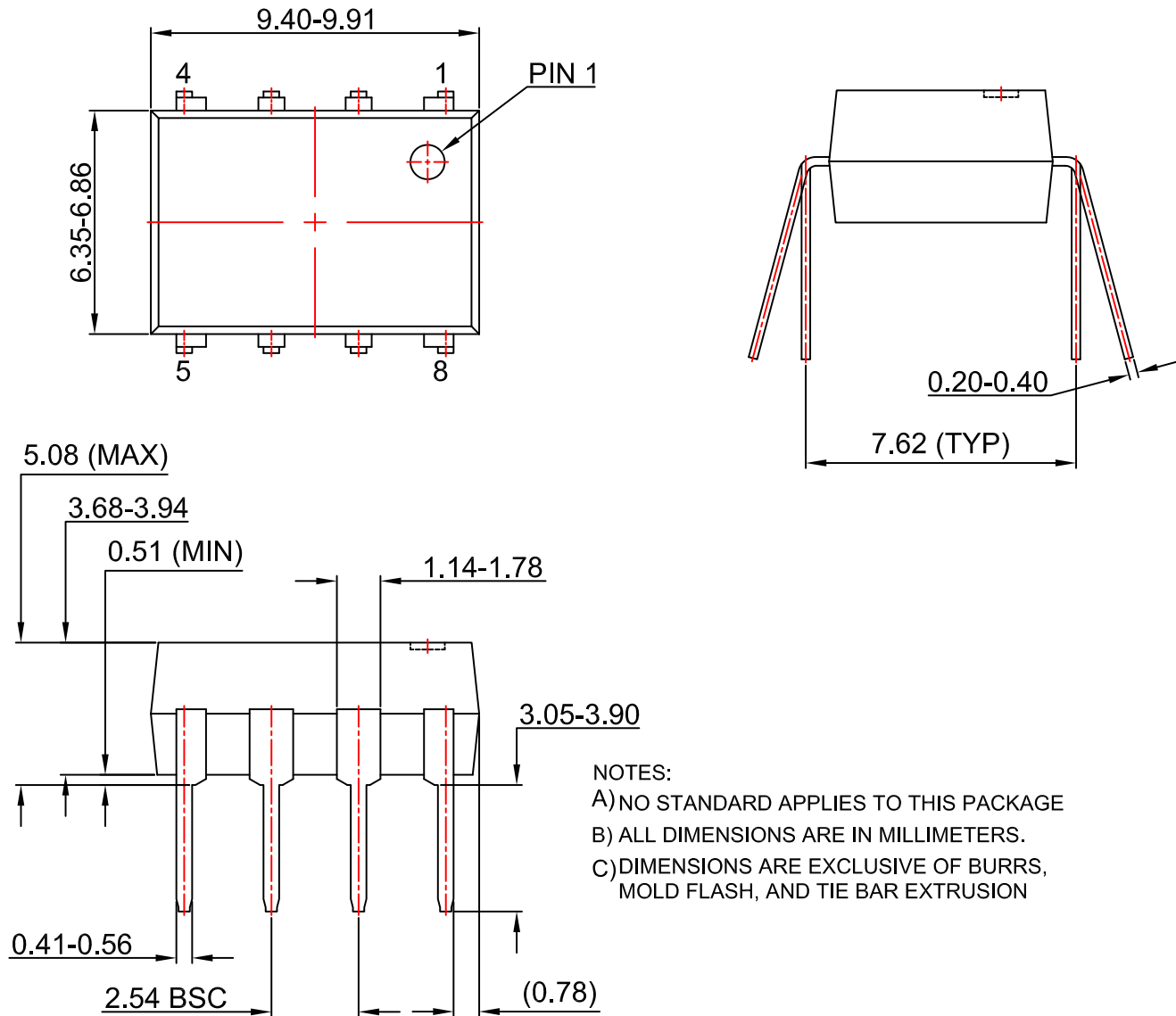


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CASE 646CQ
ISSUE O

DATE 18 SEP 2017

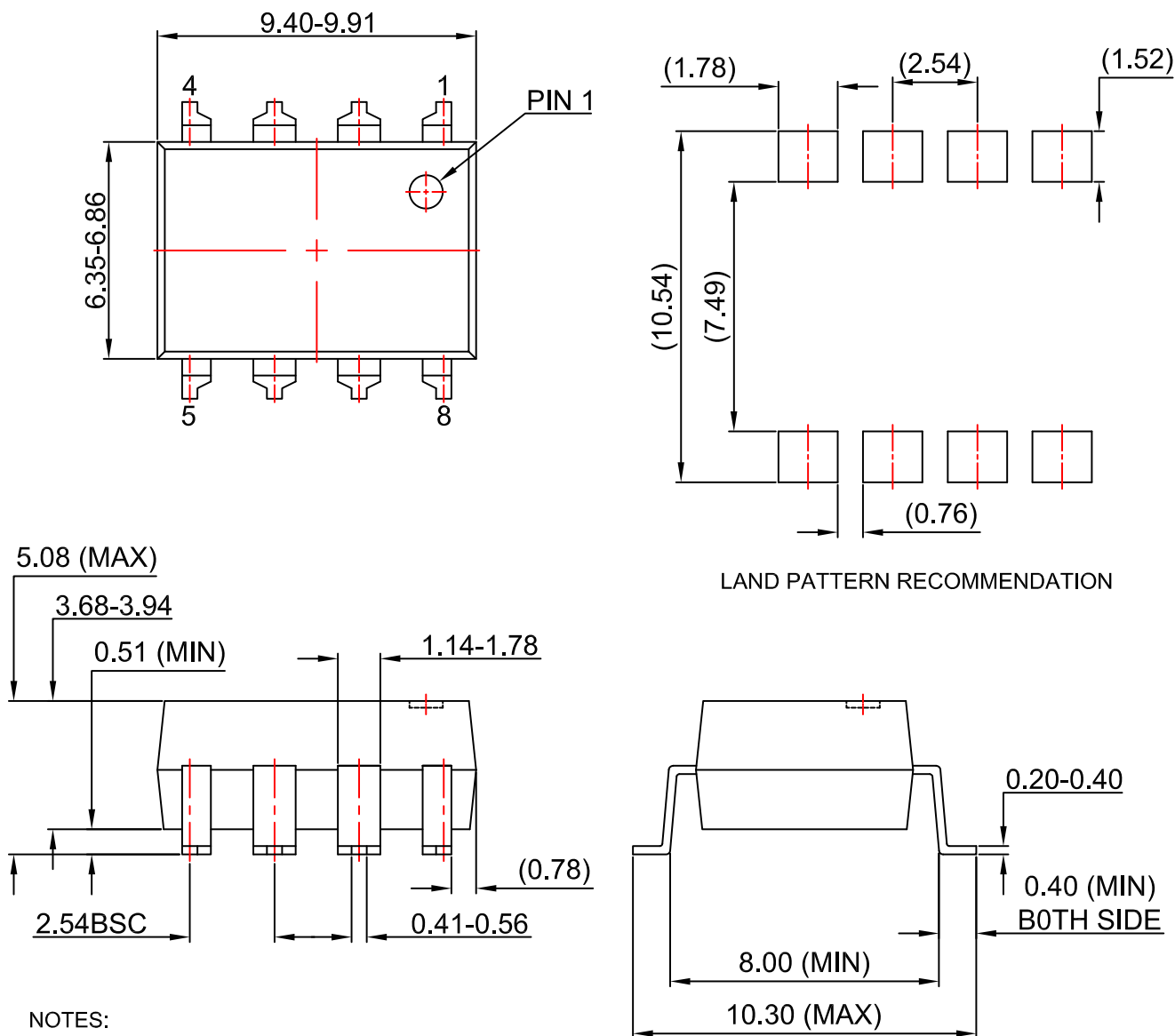


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