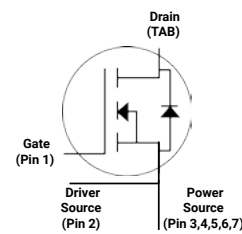


C3M0065100J

Silicon Carbide Power MOSFET C3M™ MOSFET Technology N-Channel Enhancement Mode

Features

- C3M™ SiC MOSFET technology
- Low parasitic inductance with separate driver source pin
- 7mm of creepage distance between drain and source
- High blocking voltage with low On-resistance
- Fast intrinsic diode with low reverse recovery (Q_{rr})
- Low output capacitance (60pF)
- Halogen free, RoHS compliant



Part Number	Package	Marking
C3M0065100J	TO 263-7	C3M0065100J

Wolfspeed, Inc. is in the process of rebranding its products and related materials pursuant to the entity name change from Cree, Inc. to Wolfspeed, Inc. During this transition period, products received may be marked with either the Cree name and/or logo or the Wolfspeed name and/or logo.

Typical Applications

- Renewable energy
- EV battery chargers
- High voltage DC/DC converters
- Switch Mode Power Supplies

Benefits

- Reduce switching losses and minimize gate ringing
- Higher system efficiency
- Increase power density
- Increase system switching frequency

Key Parameters

Parameter	Symbol	Min.	Typ.	Max	Unit	Conditions	Note
Drain - Source Voltage	V_{DS}			1000	V	$T_c = 25^\circ\text{C}$	
Maximum Gate - Source Voltage	$V_{GS(max)}$	-8		+19		Transient	
Operational Gate-Source Voltage	$V_{GS op}$		-4/15			Static	Note 1
DC Continuous Drain Current	I_D			32	A	$V_{GS} = 15\text{ V}, T_c = 25^\circ\text{C}, T_J \leq 150^\circ\text{C}$	Fig. 19
				21		$V_{GS} = 15\text{ V}, T_c = 100^\circ\text{C}, T_J \leq 150^\circ\text{C}$	Note 2
Pulsed Drain Current	I_{DM}			90		t_{Pmax} limited by T_{Jmax} $V_{GS} = 15\text{ V}, T_c = 25^\circ\text{C}$	Fig. 22
Avalanche energy, Single pulse	E_{AS}			110	mJ	$I_D = 22\text{ A}, V_{DD} = 50\text{ V}$	
Power Dissipation	P_D			113.5	W	$T_c = 25^\circ\text{C}, T_J = 150^\circ\text{C}$	Fig. 20
Operating Junction and Storage Temperature	T_J, T_{stg}			-55 to +150	$^\circ\text{C}$		
Solder Temperature	T_L			260		According to JEDEC J-STD-020	

Note (1): Recommended turn-on gate voltage is 15V with $\pm 5\%$ regulation tolerance, see Application Note PRD-04814 for additional details

Note (2): Verified by design



Electrical Characteristics ($T_C = 25^\circ\text{C}$ unless otherwise specified)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Test Conditions	Note
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	1000	—	—	V	$V_{GS} = 0\text{ V}, I_D = 100\text{ }\mu\text{A}$	Fig. 11
Gate Threshold Voltage	$V_{GS(th)}$	1.8	2.1	3.5		$V_{DS} = V_{GS}, I_D = 5\text{ mA}$	
		—	1.6	—		$V_{DS} = V_{GS}, I_D = 5\text{ mA}, T_J = 150^\circ\text{C}$	
Zero Gate Voltage Drain Current	I_{DSS}	—	1	100	μA	$V_{DS} = 1000\text{ V}, V_{GS} = 0\text{ V}$	
Gate-Source Leakage Current	I_{GSS}	—	10	250	nA	$V_{GS} = 15\text{ V}, V_{DS} = 0\text{ V}$	
Drain-Source On-State Resistance	$R_{DS(on)}$	—	65	78	m Ω	$V_{GS} = 15\text{ V}, I_D = 20\text{ A}$	Fig. 4, 5, 6
		—	95	—		$V_{GS} = 15\text{ V}, I_D = 20\text{ A}, T_J = 150^\circ\text{C}$	
Transconductance	g_{fs}	—	14.3	—	S	$V_{DS} = 20\text{ V}, I_{DS} = 20\text{ A}$	Fig. 7
			11.9			$V_{DS} = 20\text{ V}, I_{DS} = 20\text{ A}, T_J = 150^\circ\text{C}$	
Input Capacitance	C_{iss}	—	760	—	pF	$V_{GS} = 0\text{ V}, V_{DS} = 600\text{ V}$ $f = 1\text{ MHz}$ $V_{AC} = 25\text{ mV}$	Fig. 17, 18
Output Capacitance	C_{oss}	—	70	—			
Reverse Transfer Capacitance	C_{rss}	—	5	—			
C_{oss} Stored Energy	E_{oss}	—	15	—	μJ	$V_{DS} = 700\text{ V}, V_{GS} = -4\text{ V}/15\text{ V}, I_D = 20\text{ A},$ $R_{G(ext)} = 2.5\text{ }\Omega, L = 130\text{ }\mu\text{H}, T_J = 150^\circ\text{C}$	Fig. 26, 30 Note 3
Turn-On Switching Energy (Body Diode FWD) ³	E_{on}	—	103	—			
Turn Off Switching Energy (Body Diode FWD) ³	E_{off}	—	30	—			
Turn-On Delay Time	$t_{d(on)}$	—	7	—	ns	$V_{DD} = 700\text{ V}, V_{GS} = -4\text{ V}/15\text{ V}$ $I_D = 20\text{ A}, R_{G(ext)} = 2.5\text{ }\Omega,$ Timing relative to V_{DS} Inductive load	Fig. 27
Rise Time	t_r	—	8	—			
Turn-Off Delay Time	$t_{d(off)}$	—	13	—			
Fall Time	t_f	—	6	—			
Internal Gate Resistance	$R_{G(int)}$	—	3.5	—	Ω	$f = 1\text{ MHz}, V_{AC} = 25\text{ mV}$	
Gate to Source Charge	Q_{gs}	—	9	—	nC	$V_{DS} = 700\text{ V}, V_{GS} = -4\text{ V}/15\text{ V}$ $I_D = 20\text{ A}$ Per IEC60747-8-4 pg 21	Fig. 12
Gate to Drain Charge	Q_{gd}	—		—			
Total Gate Charge	Q_g	—	32	—			

Reverse Diode Characteristics ($T_C = 25^\circ\text{C}$ unless otherwise specified)

Parameter	Symbol	Typ.	Max.	Unit	Test Conditions	Note
Diode Forward Voltage	V_{SD}	4.5	—	V	$V_{GS} = -4\text{ V}, I_{SD} = 10\text{ A}$	Fig. 8, 9, 10
		4.2	—		$V_{GS} = -4\text{ V}, I_{SD} = 10\text{ A}, T_J = 150^\circ\text{C}$	
Continuous Diode Forward Current	I_S	—	22	A	$V_{GS} = -4\text{ V}$	
Diode Pulse Current	$I_{S, pulsed}$	—	90		$V_{GS} = -4\text{ V}, \text{pulse width limited by } T_{JMAX}$	
Reverse Recover Time	t_{rr}	15	—	nS	$V_{GS} = -4\text{ V}, I_{SD} = 20\text{ A}, V_R = 700\text{ V}$ $di_F/dt = 4500\text{ A}/\mu\text{s}, T_J = 150^\circ\text{C}$	
Reverse Recovery Charge	Q_{rr}	159	—	nC		
Peak Reverse Recovery Current	I_{rrm}	19	—	A		

Thermal Characteristics

Parameter	Symbol	Max	Unit	Note
Thermal Resistance from Junction to Case	$R_{\theta JC}$	1.1	$^\circ\text{C}/\text{W}$	Fig. 21
Thermal Resistance From Junction to Ambient	$R_{\theta JA}$	40		

Note (3): Turn-off and Turn-on switching energy and timing values measured using SiC MOSFET Body Diode

Typical Performance

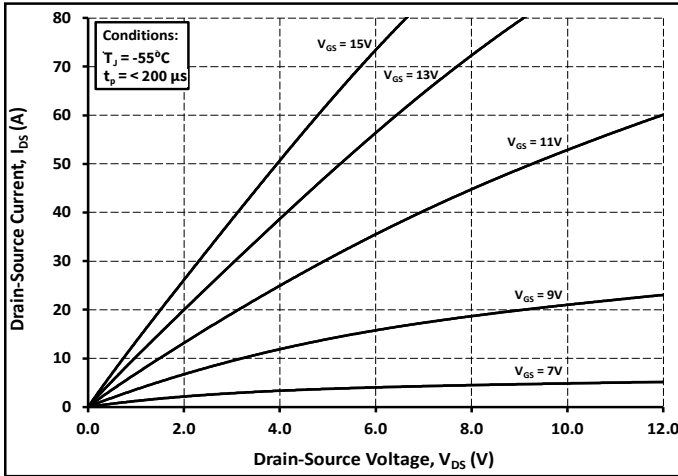


Figure 1. Output Characteristics $T_j = -55^\circ\text{C}$

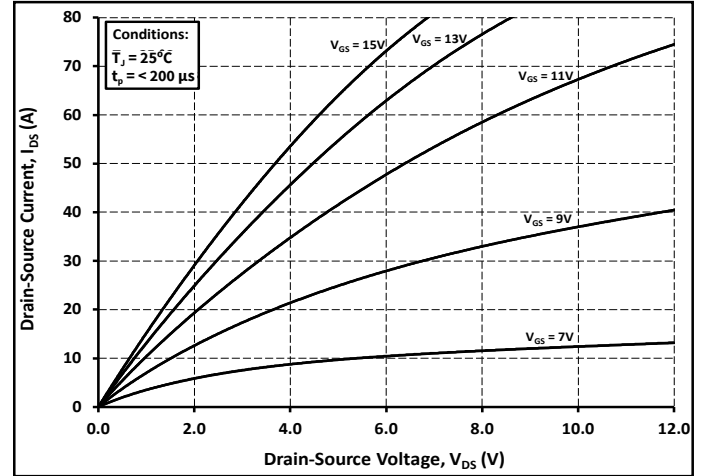


Figure 2. Output Characteristics $T_j = 25^\circ\text{C}$

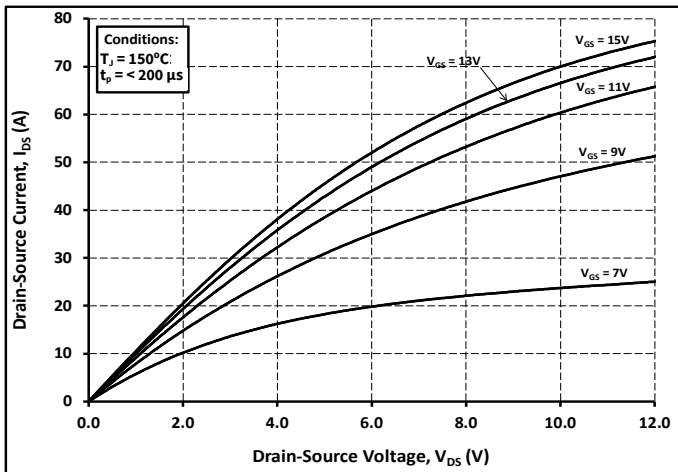


Figure 3. Output Characteristics $T_j = 150^\circ\text{C}$

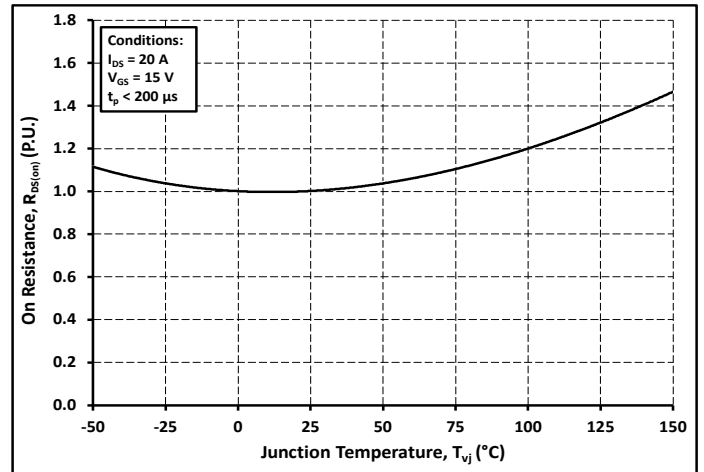


Figure 4. Normalized On-Resistance vs. Temperature

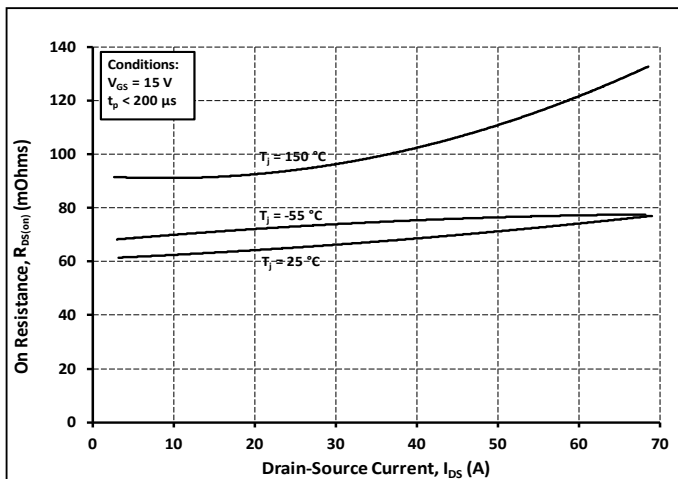


Figure 5. On-Resistance vs. Drain Current For Various Temperatures

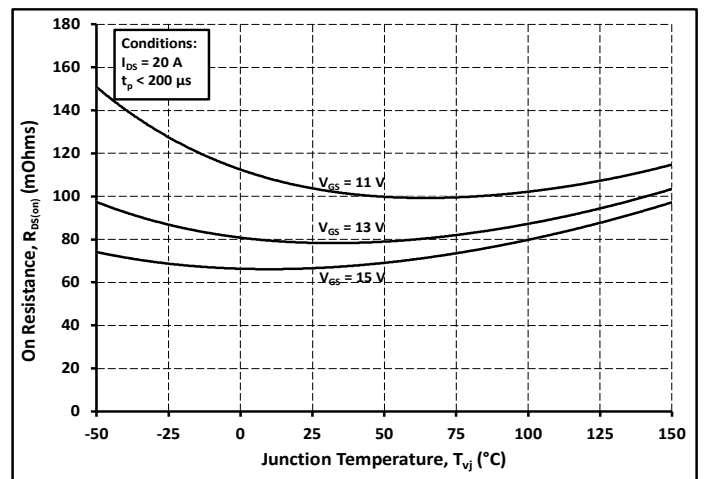


Figure 6. On-Resistance vs. Temperature For Various Gate Voltage

Typical Performance

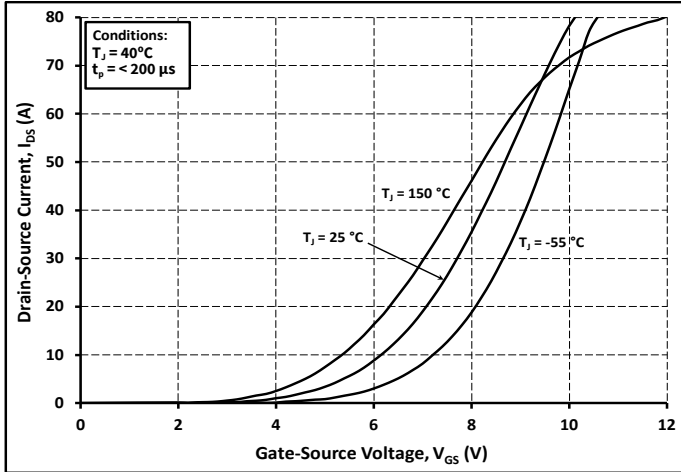


Figure 7. Transfer Characteristic for Various Junction Temperatures

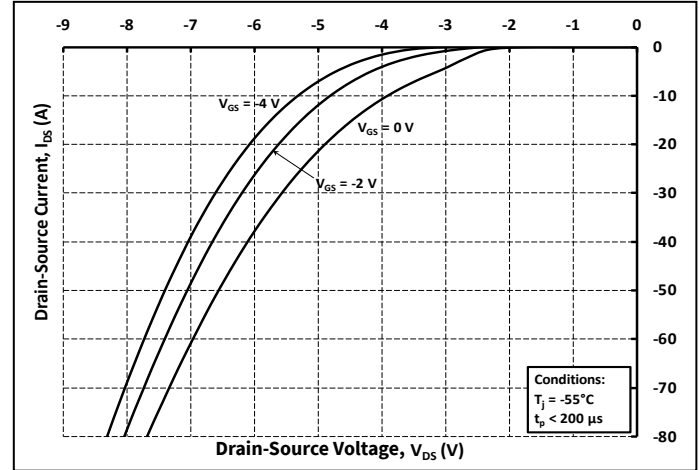


Figure 8. Body Diode Characteristic at -55°C

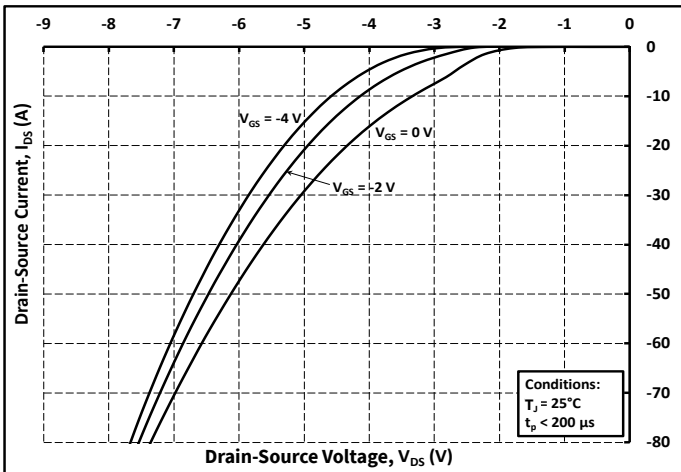


Figure 9. Body Diode Characteristic at 25°C

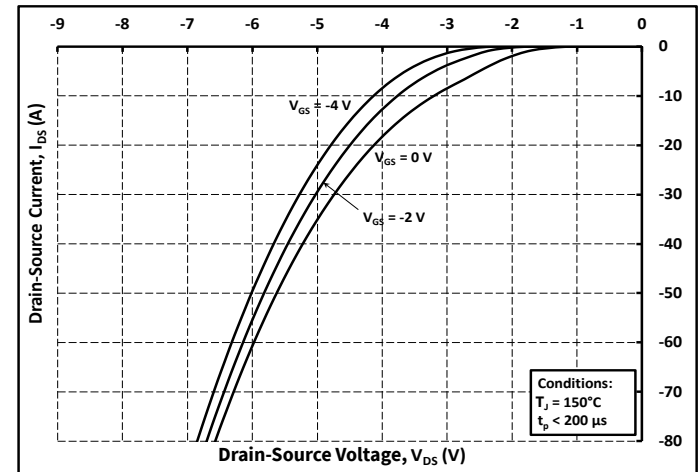


Figure 10. Body Diode Characteristic at 150°C

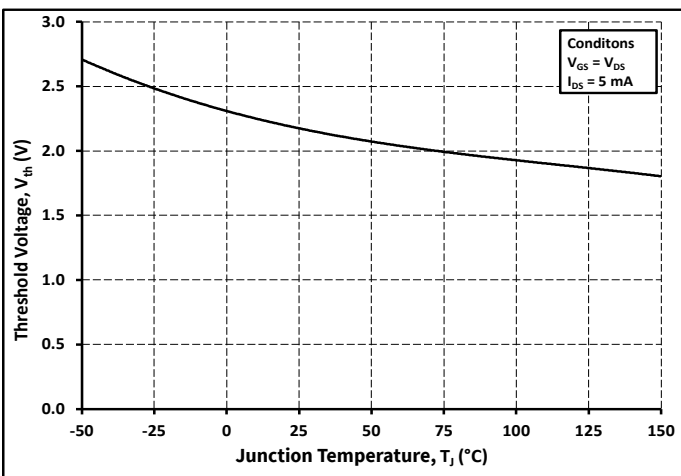


Figure 11. Threshold Voltage vs. Temperature

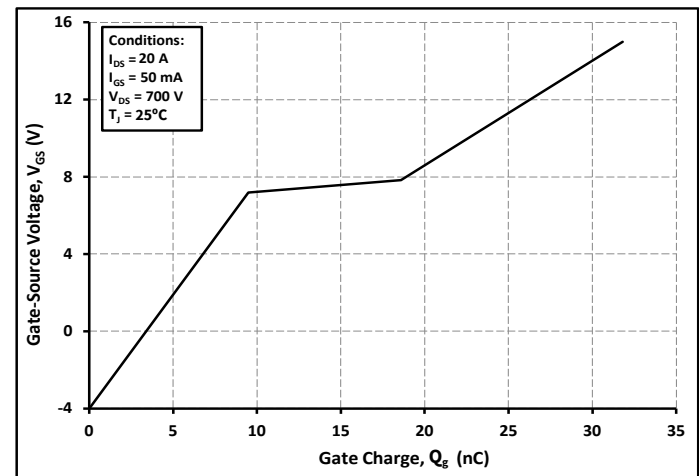


Figure 12. Gate Charge Characteristics

Typical Performance

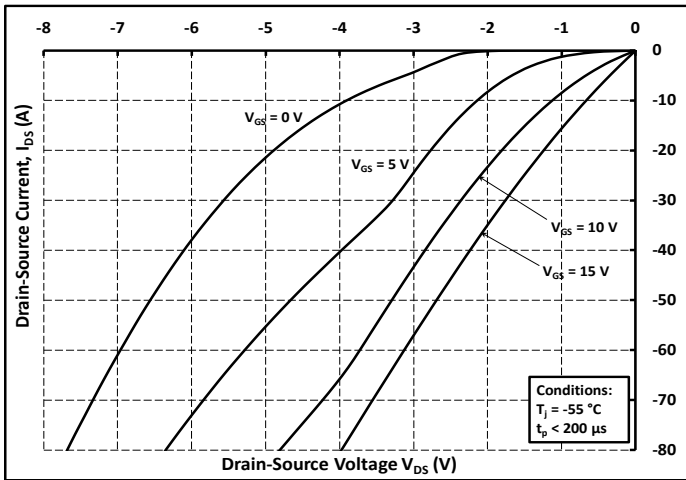


Figure 13. 3rd Quadrant Characteristic at -55°C

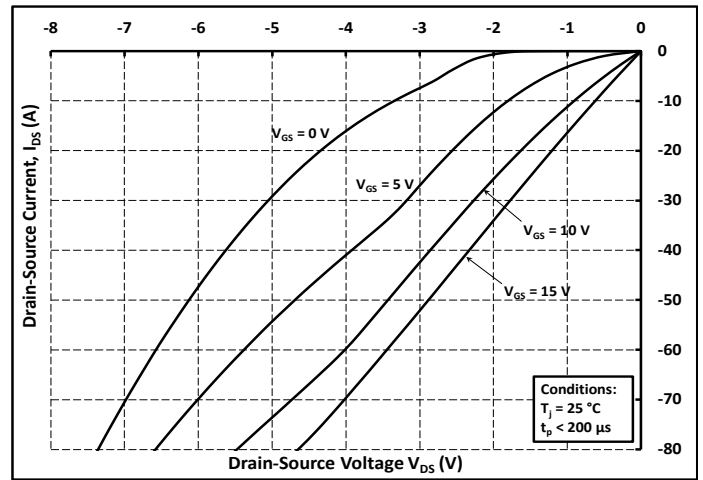


Figure 14. 3rd Quadrant Characteristic at 25°C

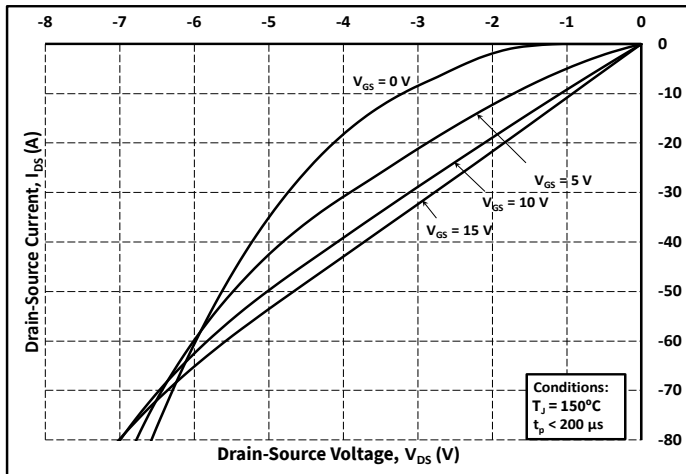


Figure 15. 3rd Quadrant Characteristic at 150°C

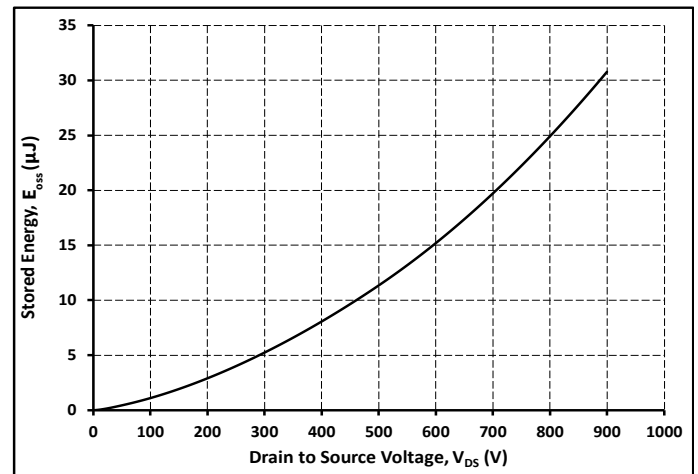


Figure 16. Output Capacitor Stored Energy

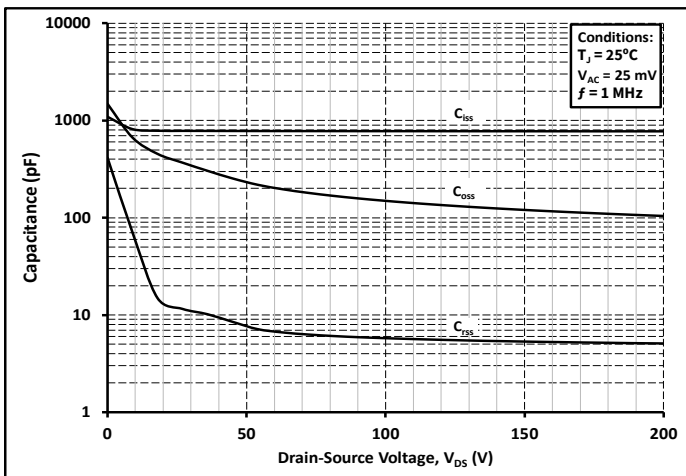


Figure 17. Capacitances vs. Drain-Source Voltage (0 - 200 V)

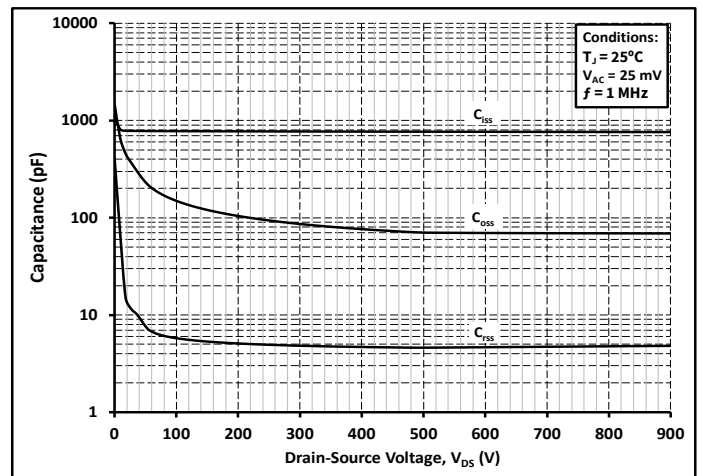


Figure 18. Capacitances vs. Drain-Source Voltage (0 - 1000 V)

Typical Performance

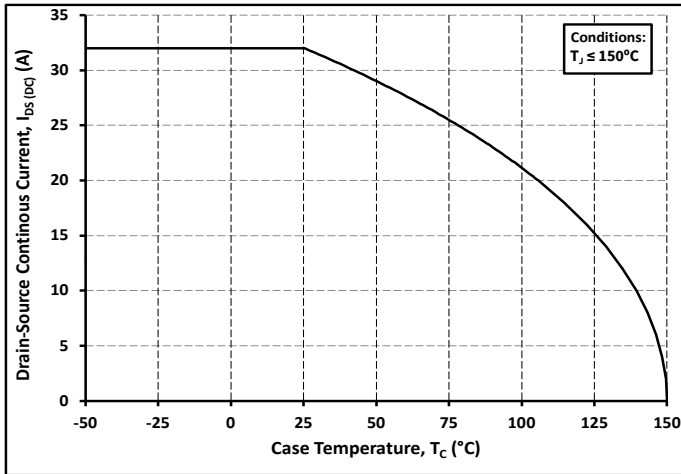


Figure 19. Continuous Drain Current Derating vs. Case Temperature

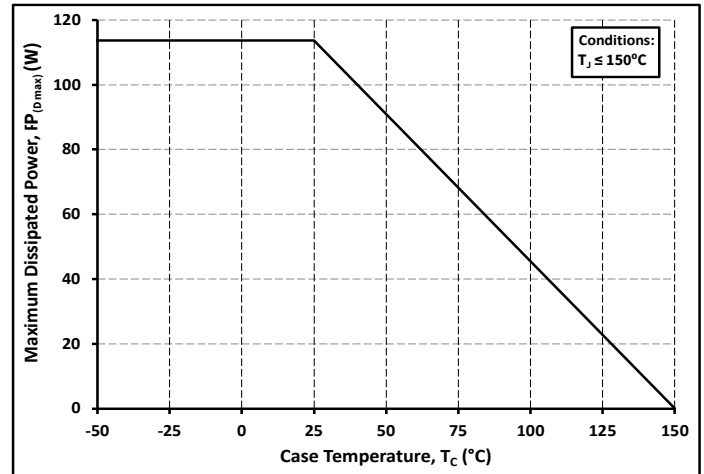


Figure 20. Maximum Power Dissipation Derating vs. Case Temperature

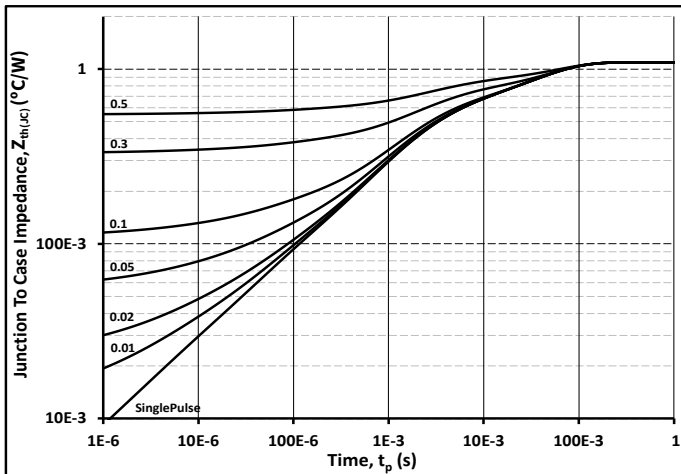


Figure 21. Transient Thermal Impedance (Junction - Case)

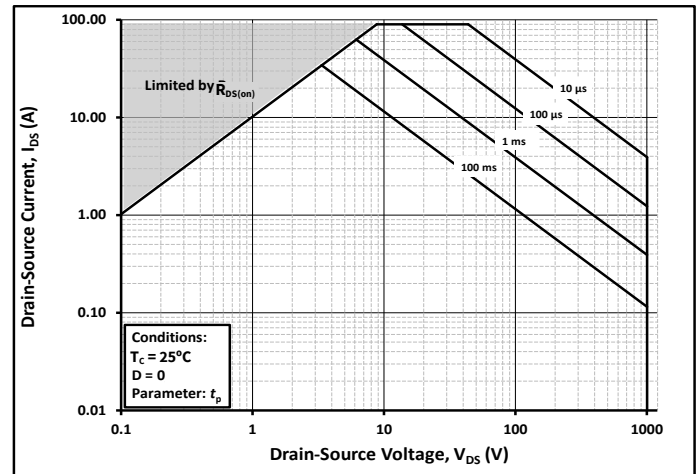


Figure 22. Safe Operating Area

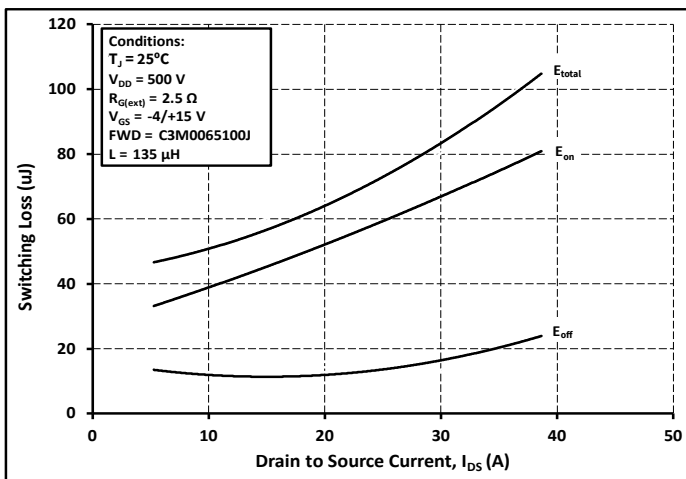


Figure 23. Clamped Inductive Switching Energy vs. Drain Current ($V_{DD} = 500\text{ V}$)

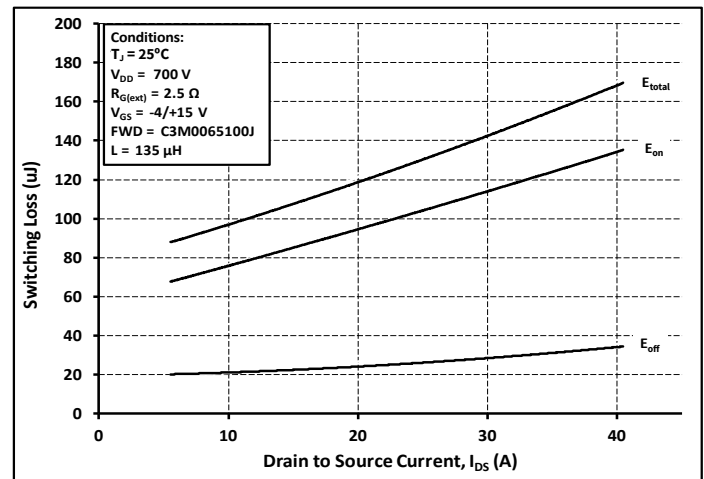


Figure 24. Clamped Inductive Switching Energy vs. Drain Current ($V_{DD} = 700\text{ V}$)

Typical Performance

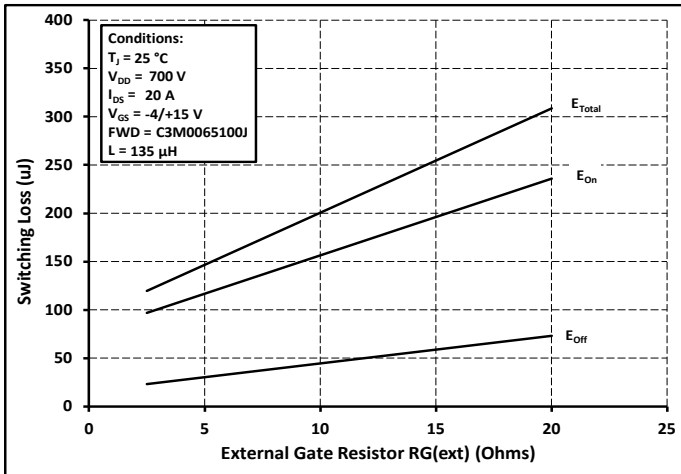


Figure 25. Clamped Inductive Switching Energy vs. $R_{G(\text{ext})}$

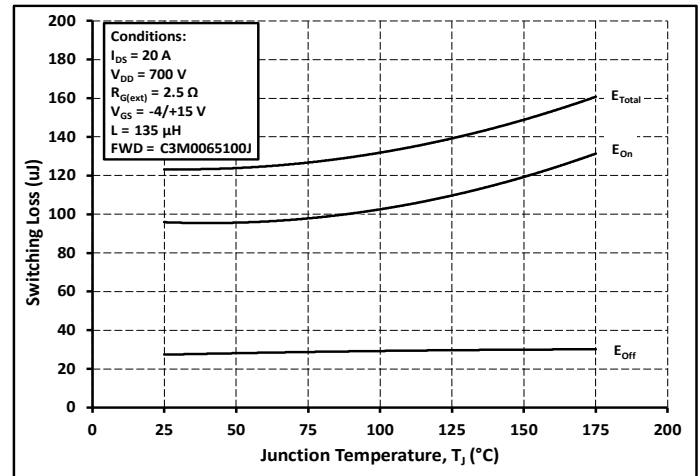


Figure 26. Clamped Inductive Switching Energy vs. Temperature

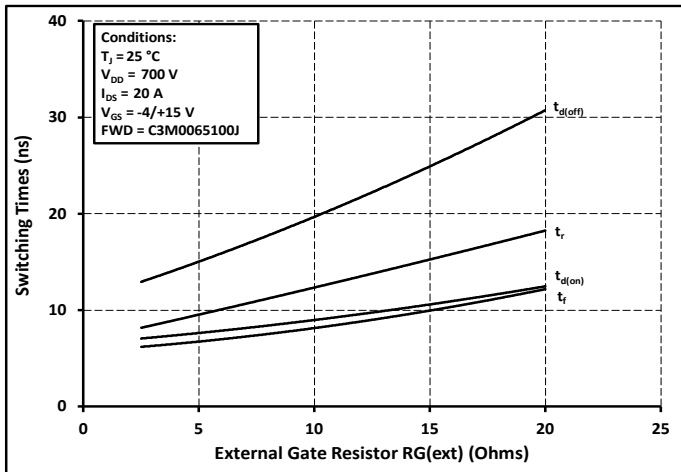


Figure 27. Switching Times vs. $R_{G(\text{ext})}$

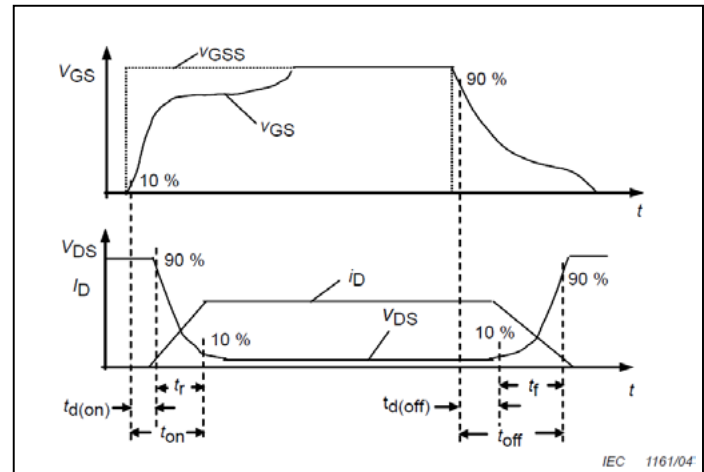


Figure 28. Switching Times Definition

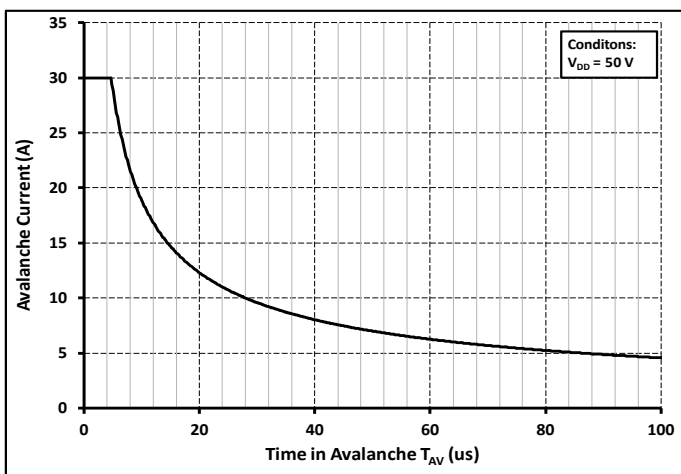


Figure 29. Single Avalanche SOA curve

Test Circuit Schematic

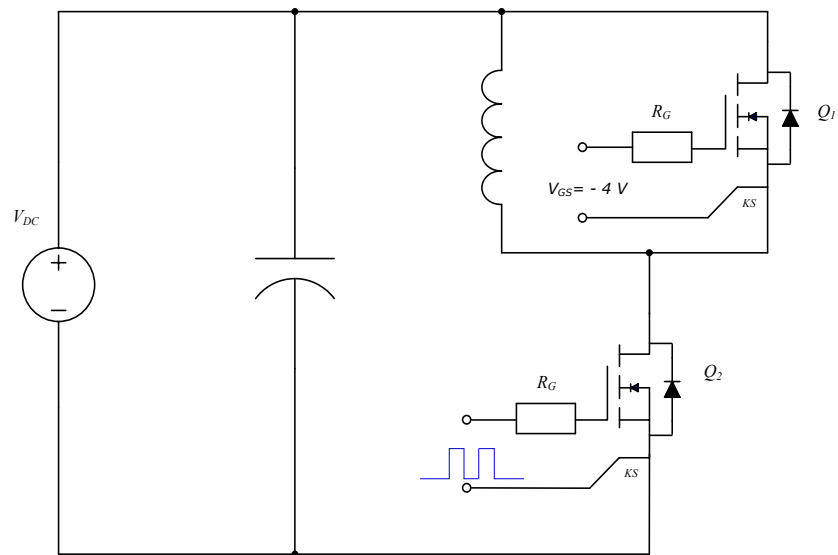
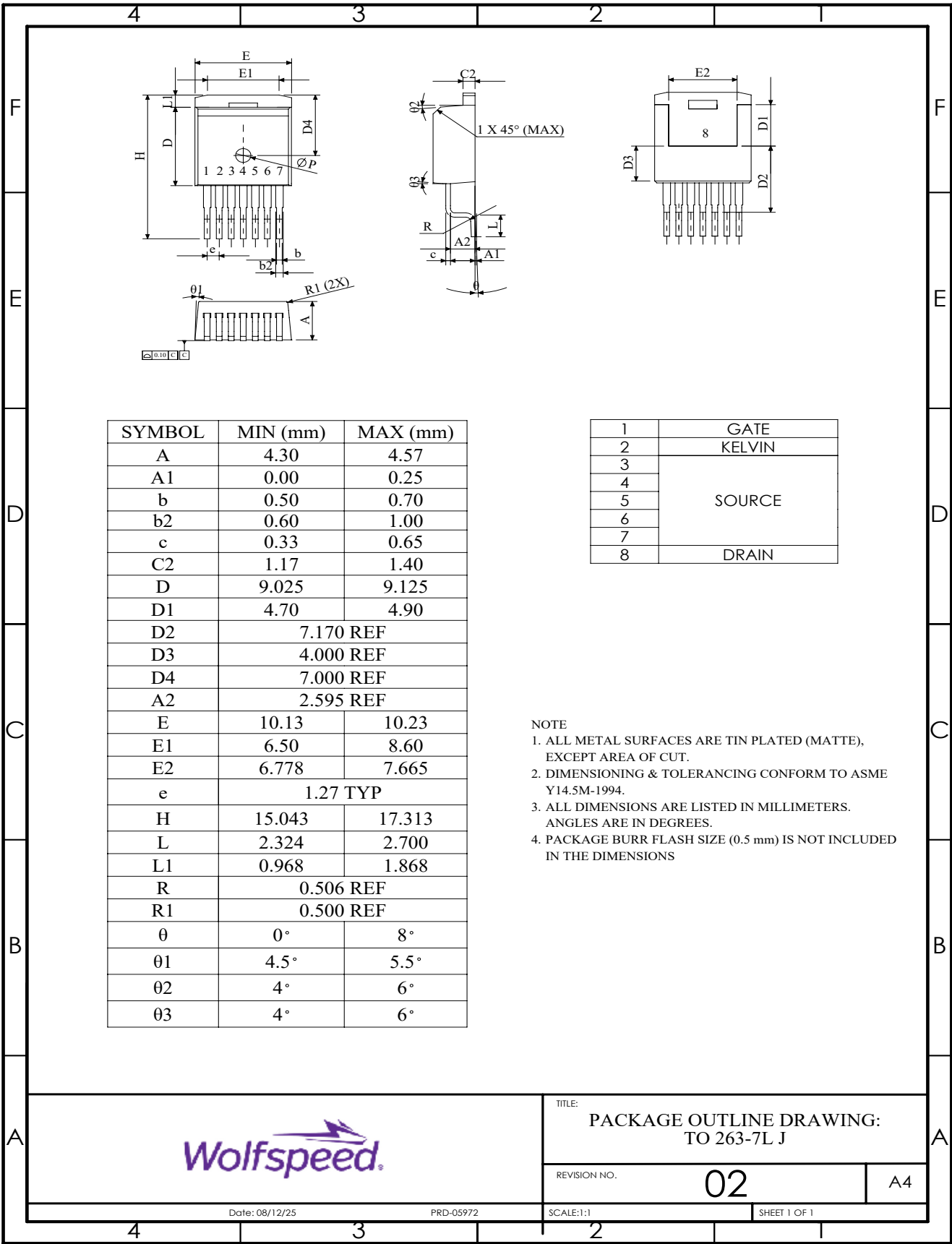


Figure 30. Clamped Inductive Switching
Waveform Test Circuit

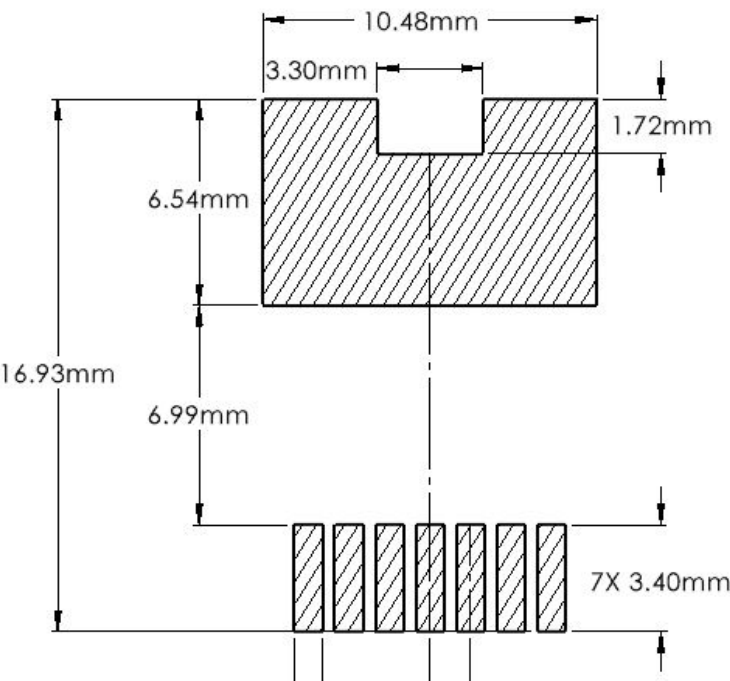
Note:

Turn-off and Turn-on switching energy and timing values measured using SiC MOSFET Body Diode as shown above.

Package Dimensions – Package 7L D2PAK



Recommended Solder Pad Layout



Revision History

Current Revision	Date of Release	Description of Changes
1	September-2020	N/A
2	January-2024	Updated Wolfspeed branding, package drawing, package image, solder pad layout, added Rev history, Table 1 layout revised
3	December - 2024	Legal Disclaimer Updated
4	September - 2025	Package drawing updated to correct dimension D1

Related Links

- [SiC MOSFET Isolated Gate Driver reference design](#)
- [SiC MOSFET Evaluation Board](#)



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