40V 175°C P-CHANNEL ENHANCEMENT MODE MOSFET
PowerDI3333-8

Product Summary

BV_{DSS}	$R_{DS(ON)}$ Max	I_D Max T_A = +25°C
-40V	29mΩ @ V_{GS} = -10V	-8.0A
	45mΩ @ V_{GS} = -4.5V	-6.0A

Features and Benefits

- Rated to +175°C — Ideal for High Ambient Temperature Environments
- 100% Unclamped Inductive Switching Test in Production — Ensures More Reliable and Robust End Application
- Low $R_{DS(ON)}$ — Ensures On State Losses Are Minimized
- Small Form Factor Thermally Efficient Package Enables Higher Density End Products
- Occupies Just 33% of the Board Area Occupied by SO-8 Enabling Smaller End Product
- **Lead-Free Finish; RoHS Compliant (Notes 1 & 2)**
- **Halogen and Antimony Free. "Green" Device (Note 3)**
- **The DMPH4029LFGQ is suitable for automotive applications requiring specific change control; this part is AEC-Q101 qualified, PPAP capable, and manufactured in IATF 16949 certified facilities.**
  https://www.diodes.com/quality/product-definitions/

Description and Applications

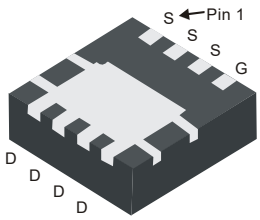
This MOSFET is designed to meet the stringent requirements of automotive applications. It is qualified to AEC-Q101, supported by a PPAP and is ideal for use in:

- Backlighting
- Power-management functions
- DC-DC converters

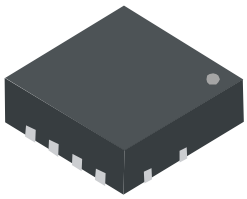
Mechanical Data

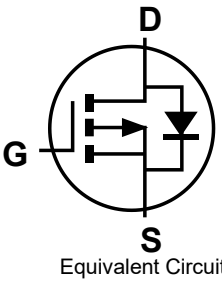
- Package: PowerDI®3333-8
- Surface-Mount Package
- Package Material: Molded Plastic, UL Flammability Rating 94V-0
- Moisture Sensitivity: Level 1 per J-STD-020
- Terminals: Finish - Matte Tin Plated Leads. Solderable per MIL-STD-202, Method 208 e3
- Weight: 0.034 grams (Approximate)

PowerDI3333-8



Bottom View


Top View



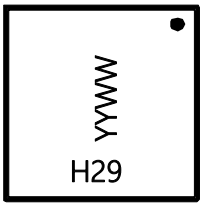
Equivalent Circuit

Ordering Information (Note 4)

Orderable Part Number	Package	Packing	
		Qty.	Carrier
DMPH4029LFGQ-7	PowerDI3333-8	2000	Tape & Reel
DMPH4029LFGQ-13	PowerDI3333-8	3000	Tape & Reel

Notes:
1. EU Directive 2002/95/EC (RoHS), 2011/65/EU (RoHS 2) & 2015/863/EU (RoHS 3) compliant. All applicable RoHS exemptions applied.
2. See https://www.diodes.com/quality/lead-free/ for more information about Diodes Incorporated's definitions of Halogen- and Antimony-free, "Green" and Lead-free.
3. Halogen- and Antimony-free "Green" products are defined as those which contain <900ppm bromine, <900ppm chlorine (<1500ppm total Br + Cl) and <1000ppm antimony compounds.
4. For packaging details, go to our website at https://www.diodes.com/design/support/packaging/diodes-packaging/.

Marking Information



H29 = Product Type Marking Code
YYWW = Date Code Marking
YY = Last Two Digits of Year (ex: 25 = 2025)
WW = Week Code (01 to 53)

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Maximum Ratings (@T_A = +25°C, unless otherwise specified.)

Characteristic			Symbol	Value	Unit
Drain-Source Voltage			V_{DSS}	-40	V
Gate-Source Voltage			V_{GSS}	±20	V
Continuous Drain Current (Note 6) V_{GS} = -10V	Steady State	T_A = +25°C T_A = +70°C	I_D	-8.0 -6.7	A
	Steady State	T_C = +25°C T_C = +70°C	I_D	-22 -18	A
Pulsed Drain Current (380µs Pulse, Duty Cycle = 1%)			I_{DM}	-88	A
Maximum Continuous Body Diode Forward Current (Note 6)			I_S	-8	A
Pulsed Source Current (380µs Pulse, Duty Cycle = 1%)			I_{SM}	-88	A
Avalanche Current (Note 7) L = 0.1mH			I_{AS}	-25	A
Avalanche Energy (Note 7) L = 0.1mH			E_{AS}	32	mJ

Thermal Characteristics (@T_A = +25°C, unless otherwise specified.)

Characteristic		Symbol	Value	Unit
Total Power Dissipation (Note 5)		P_D	1.2	W
Thermal Resistance, Junction to Ambient (Note 5)	Steady State	$R_{\theta JA}$	125	°C/W
	t < 10s		85	
Total Power Dissipation (Note 6)		P_D	2.8	W
Thermal Resistance, Junction to Ambient (Note 6)	Steady State	$R_{\theta JA}$	54	°C/W
	t < 10s		36	
Thermal Resistance, Junction to Case (Note 6)		$R_{\theta JAC}$	6	
Operating and Storage Temperature Range		T_J, T_{STG}	-55 to +175	°C

Electrical Characteristics (@T_A = +25°C, unless otherwise specified.)

Characteristic	Symbol	Min	Typ	Max	Unit	Test Condition
OFF CHARACTERISTICS (Note 8)						
Drain-Source Breakdown Voltage	BV_{DSS}	-40	—	—	V	V_{GS} = 0, I_D = -250µA
Zero Gate Voltage Drain Current, T_J = +25°C	I_{DSS}	—	—	-1	µA	V_{DS} = -40V, V_{GS} = 0
Gate-Source Leakage	I_{GSS}	—	—	±100	nA	V_{GS} = ±20V, V_{DS} = 0
ON CHARACTERISTICS (Note 8)						
Gate Threshold Voltage	$V_{GS(TH)}$	-1.0	—	-3.0	V	V_{DS} = V_{GS}, I_D = -250µA
Static Drain-Source On-Resistance	$R_{DS(ON)}$	—	18	29	mΩ	V_{GS} = -10V, I_D = -3A
		—	23	45		V_{GS} = -4.5V, I_D = -3A
Diode Forward Voltage	V_{SD}	—	-0.7	-1.2	V	V_{GS} = 0, I_S = -1A
DYNAMIC CHARACTERISTICS (Note 9)						
Input Capacitance	C_{iss}	—	1626	—	pF	V_{DS} = -20V, V_{GS} = 0, f = 1.0MHz
Output Capacitance	C_{oss}	—	135	—	pF	
Reverse Transfer Capacitance	C_{rss}	—	107	—	pF	
Gate Resistance	R_g	—	11	—	Ω	V_{DS} = 0, V_{GS} = 0, f = 1MHz
Total Gate Charge (V_{GS} = -4.5V)	Q_g	—	17	—	nC	V_{DS} = -20V, I_D = -3A
Total Gate Charge (V_{GS} = -10V)	Q_g	—	34	—	nC	
Gate-Source Charge	Q_{gs}	—	3.7	—	nC	
Gate-Drain Charge	Q_{gd}	—	6.0	—	nC	
Turn-On Delay Time	$t_{D(ON)}$	—	3.9	—	ns	V_{GS} = -10V, V_{DS} = -20V, R_G = 3Ω, I_D = -3A
Turn-On Rise Time	t_R	—	2.8	—	ns	
Turn-Off Delay Time	$t_{D(OFF)}$	—	83	—	ns	
Turn-Off Fall Time	t_F	—	30	—	ns	
Body Diode Reverse-Recovery Time	t_{RR}	—	17.3	—	ns	I_F = -3A, di/dt = 100A/µs
Body Diode Reverse-Recovery Charge	Q_{RR}	—	7.2	—	nC	I_F = -3A, di/dt = 100A/µs

Notes:
5. Device mounted on FR-4 PC board, with minimum recommended pad layout, single sided.
6. Device mounted on FR-4 substrate PC board, 2oz copper, with thermal bias to bottom layer 1inch square copper plate.
7. I_{AS} and E_{AS} ratings are based on low frequency and duty cycles to keep T_J = +25°C.
8. Short duration pulse test used to minimize self-heating effect.
9. Guaranteed by design. Not subject to product testing.

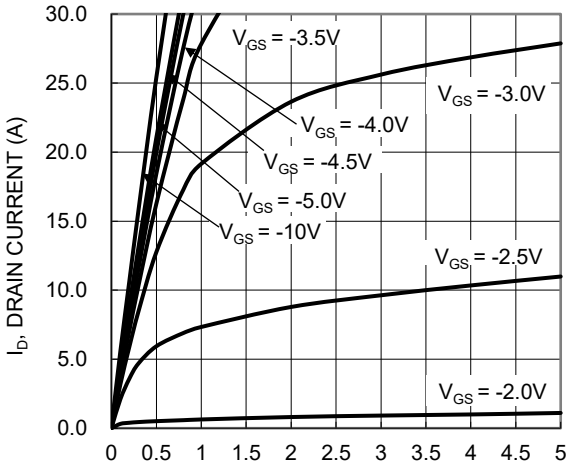


Figure 1. Typical Output Characteristic

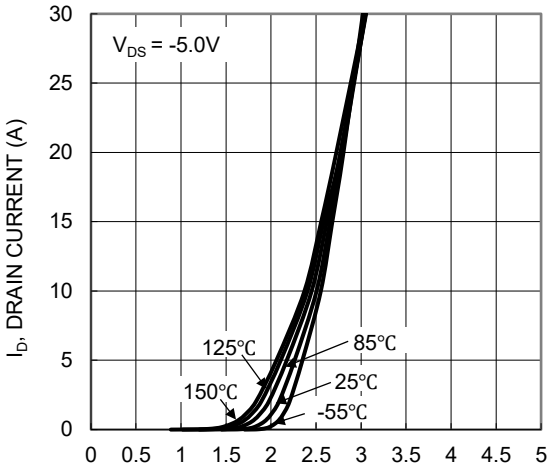


Figure 2. Typical Transfer Characteristic

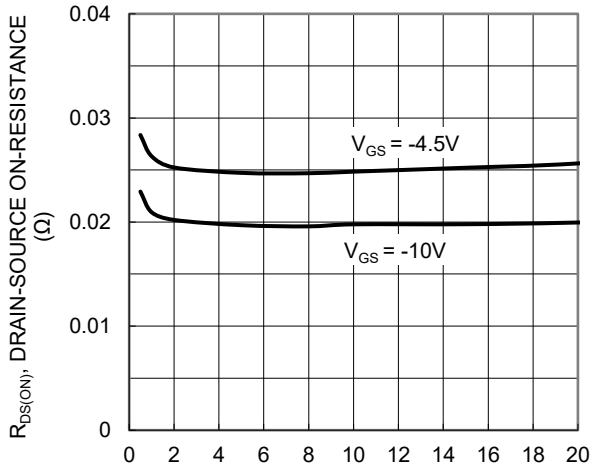


Figure 3. Typical On-Resistance vs. Drain Current and Gate Voltage

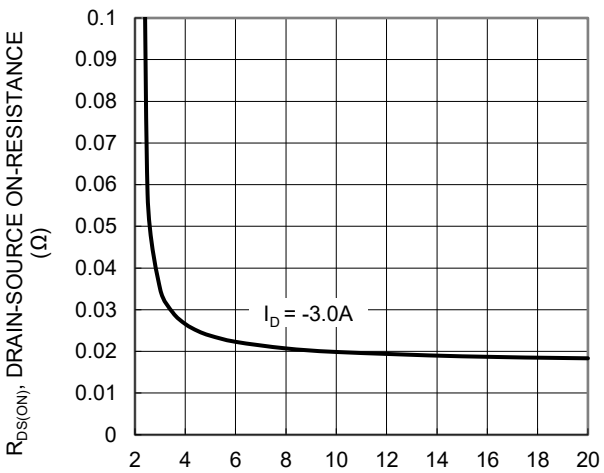


Figure 4. Typical Transfer Characteristic

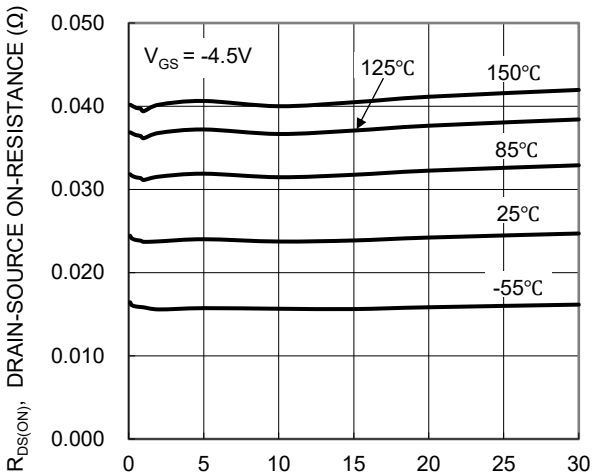


Figure 5. Typical On-Resistance vs. Drain Current and Temperature

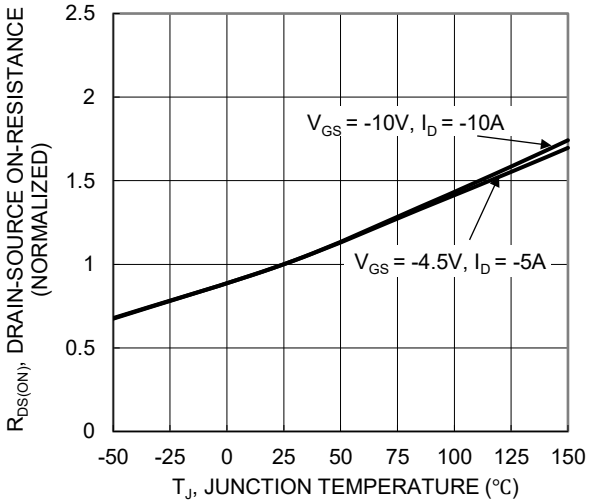


Figure 6. On-Resistance Variation with Temperature

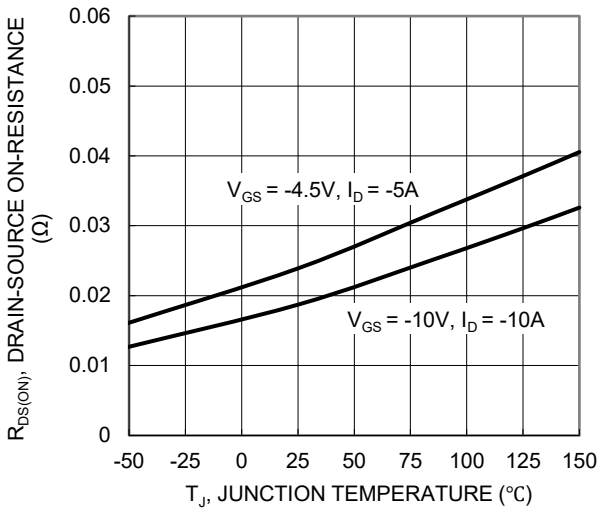


Figure 7. On-Resistance Variation with Temperature

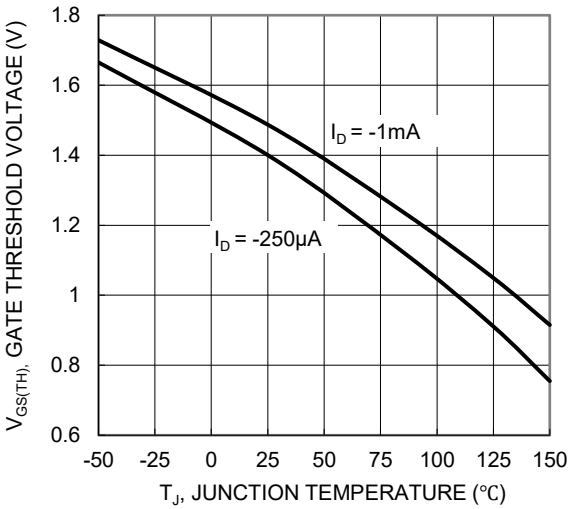


Figure 8. Gate Threshold Variation vs. Junction Temperature

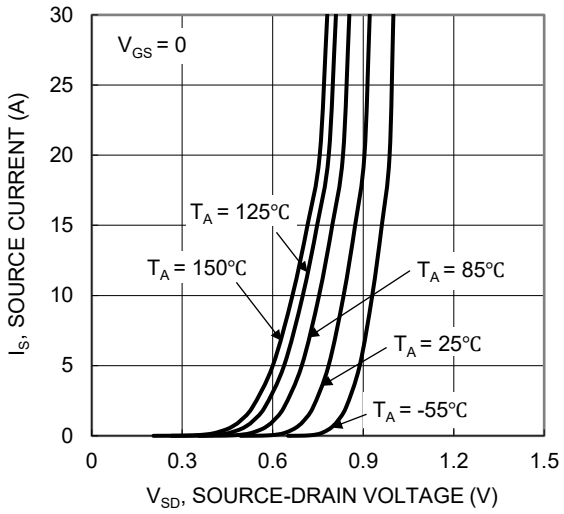


Figure 9. Diode Forward Voltage vs. Current

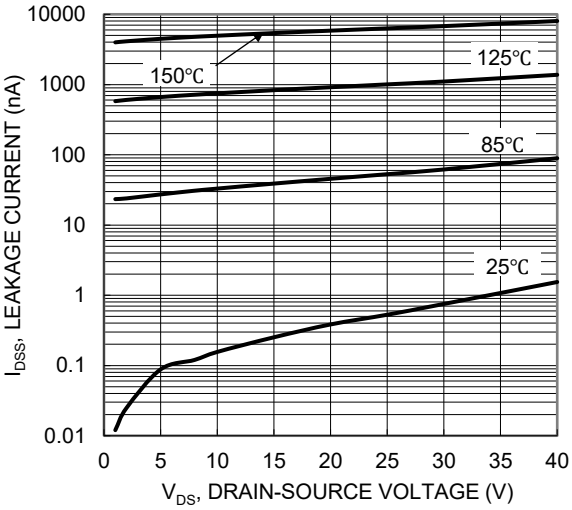


Figure 10. Typical Drain-Source Leakage Current vs. Voltage

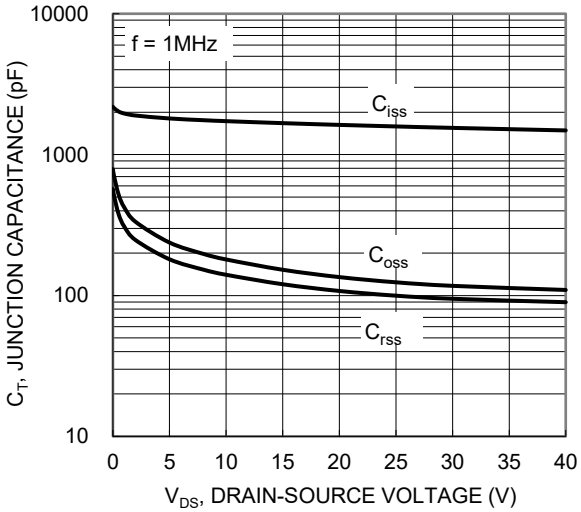


Figure 11. Typical Junction Capacitance

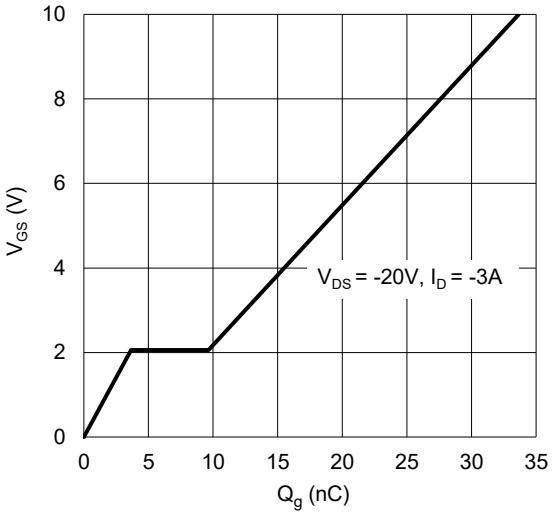


Figure 12. Gate Charge

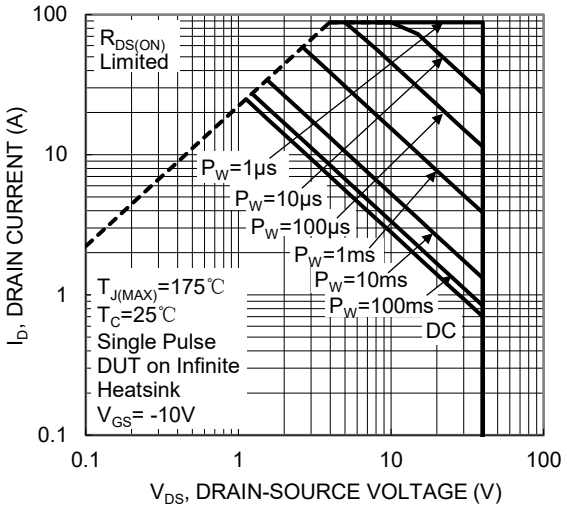


Figure 13. SOA, Safe Operation Area

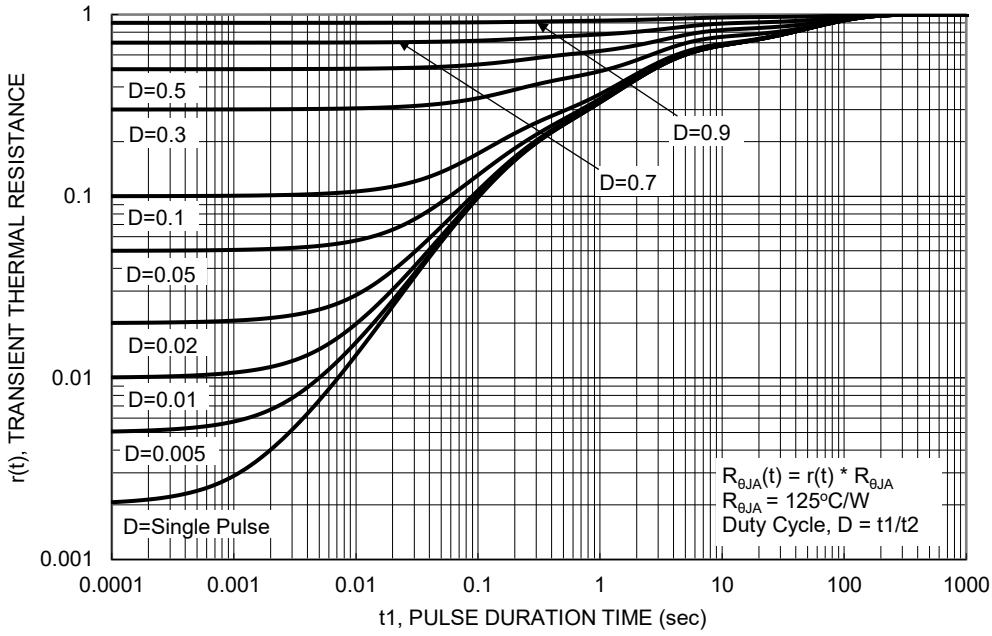
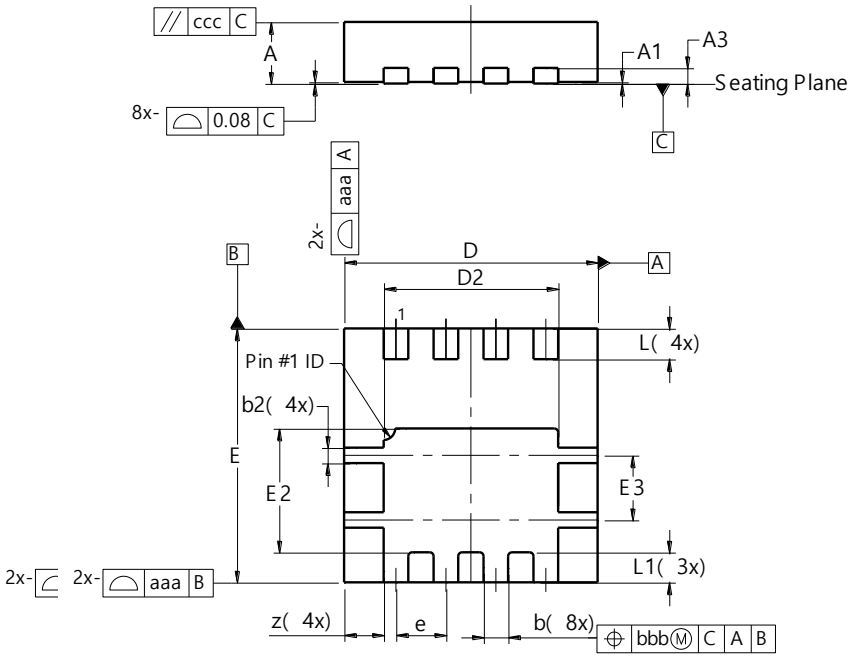


Figure 14. Transient Thermal Resistance

Package Outline Dimensions

Please see http://www.diodes.com/package-outlines.html for the latest version.

PowerDI3333-8

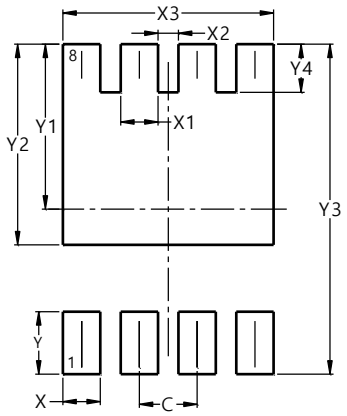


PowerDI3333-8			
Dim	**Min**	**Max**	**Typ**
A	0.75	0.85	0.80
A1	0.00	0.05	0.02
A3	–	–	0.203
b	0.27	0.37	0.32
b2	–	–	0.20
D	3.25	3.35	3.30
D2	2.22	2.32	2.27
E	3.25	3.35	3.30
E2	1.56	1.66	1.61
E3	0.79	0.89	0.84
e	–	–	0.65
L	0.35	0.45	0.40
L1	–	–	0.39
z	–	–	0.515
aaa	0.25		
bbb	0.10		
ccc	0.10		
All Dimensions in mm			

Suggested Pad Layout

Please see http://www.diodes.com/package-outlines.html for the latest version.

PowerDI3333-8



Dimensions	Value (in mm)
C	0.650
X	0.420
X1	0.420
X2	0.230
X3	2.370
Y	0.700
Y1	1.850
Y2	2.250
Y3	3.700
Y4	0.540

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