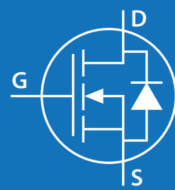
EPC2065 – Enhancement Mode Power Transistor

V_{DS} , 80 V
$R_{DS(on)}$, 3.6 mΩ
I_D , 60 A



EFFICIENT POWER CONVERSION

RoHS Halogen-Free

Revised June 11, 2021

Gallium Nitride's exceptionally high electron mobility and low temperature coefficient allows very low $R_{DS(on)}$, while its lateral device structure and majority carrier diode provide exceptionally low Q_G and zero Q_{RR}. The end result is a device that can handle tasks where very high switching frequency, and low on-time are beneficial as well as those where on-state losses dominate.

Questions: Ask a GaN Expert

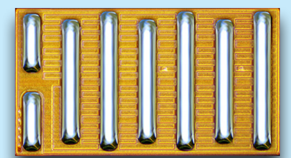
Maximum Ratings			
PARAMETER		VALUE	UNIT
V_{DS}	Drain-to-Source Voltage (Continuous)	80	V
	Drain-to-Source Voltage (up to 10,000 5 ms pulses at 150°C)	96	
I_D	Continuous (T_A = 25°C)	60	A
	Pulsed (25°C, T_{PULSE} = 300 µs)	215	
V_{GS}	Gate-to-Source Voltage	6	V
	Gate-to-Source Voltage	-4	
T_J	Operating Temperature	–40 to 150	°C
T_{STG}	Storage Temperature	–40 to 150	

Thermal Characteristics			
PARAMETER		TYP	UNIT
$R_{θJC}$	Thermal Resistance, Junction-to-Case	0.5	°C/W
$R_{θJB}$	Thermal Resistance, Junction-to-Board	1.4	
$R_{θJA}$	Thermal Resistance, Junction-to-Ambient (Note 1)	53	

Note 1: $R_{θJA}$ is determined with the device mounted on one square inch of copper pad, single layer 2 oz copper on FR4 board. See https://epc-co.com/epc/documents/product-training/Appnote_Thermal_Performance_of_eGaN_FETs.pdf for details.

Static Characteristics (T_J = 25°C unless otherwise stated)						
PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
BV_{DSS}	Drain-to-Source Voltage	V_{GS} = 0 V, I_D = 0.4 mA	80			V
I_{DSS}	Drain-Source Leakage	V_{GS} = 0 V, V_{DS} = 64 V		0.001	0.35	mA
I_{GSS}	Gate-to-Source Forward Leakage	V_{GS} = 5 V		0.002	4	
	Gate-to-Source Reverse Leakage#	V_{GS} = 5 V, T_J = 125°C		0.03	9	
	Gate-to-Source Reverse Leakage	V_{GS} = -4 V		0.004	0.4	
$V_{GS(TH)}$	Gate Threshold Voltage	V_{DS} = V_{GS}, I_D = 7 mA	0.7	1.2	2.5	V
$R_{DS(on)}$	Drain-Source On Resistance	V_{GS} = 5 V, I_D = 25 A		2.7	3.6	mΩ
V_{SD}	Source-Drain Forward Voltage#	I_S = 0.5 A, V_{GS} = 0 V		1.4		V

Defined by design. Not subject to production test.



Die size: 3.5 x 1.95 mm

EPC2065 eGaN® FETs are supplied only in passivated die form with solder bars.

Applications

- DC-DC converters
- BLDC motor drives
- Sync rectification for AC/DC and DC-DC
- Point of load converters

Benefits

- Ultra high efficiency
- No reverse recovery
- Ultra low Q_G
- Small footprint
- High power density
- High frequency capability
- Cost effective

Scan QR code or click link below for more information including reliability reports, device models, demo boards!

https://l.ead.me/EPC2065

Dynamic Characteristics# (T_J = 25°C unless otherwise stated)						
PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
C_{ISS}	Input Capacitance	V_{DS} = 40 V, V_{GS} = 0 V		1097	1449	pF
C_{RSS}	Reverse Transfer Capacitance			8.9		
C_{OSS}	Output Capacitance			534	801	
$C_{OSS(ER)}$	Effective Output Capacitance, Energy Related (Note 2)	V_{DS} = 0 to 40 V, V_{GS} = 0 V		678		
$C_{OSS(TR)}$	Effective Output Capacitance, Time Related (Note 3)			842		
R_G	Gate Resistance			0.5		Ω
Q_G	Total Gate Charge	V_{DS} = 40 V, V_{GS} = 5 V, I_D = 25 A		9.4	12.2	nC
Q_{GS}	Gate-to-Source Charge	V_{DS} = 40 V, I_D = 25 A		2.6		
Q_{GD}	Gate-to-Drain Charge			1.7		
$Q_{G(TH)}$	Gate Charge at Threshold			2.0		
Q_{OSS}	Output Charge	V_{DS} = 40 V, V_{GS} = 0 V		33	50	
Q_{RR}	Source-Drain Recovery Charge			0		

Defined by design. Not subject to production test.
All measurements were done with substrate connected to source.
Note 2: $C_{OSS(ER)}$ is a fixed capacitance that gives the same stored energy as C_{OSS} while V_{DS} is rising from 0 to 50% BV_{DSS}.
Note 3: $C_{OSS(TR)}$ is a fixed capacitance that gives the same charging time as C_{OSS} while V_{DS} is rising from 0 to 50% BV_{DSS}.

Figure 1: Typical Output Characteristics at 25°C

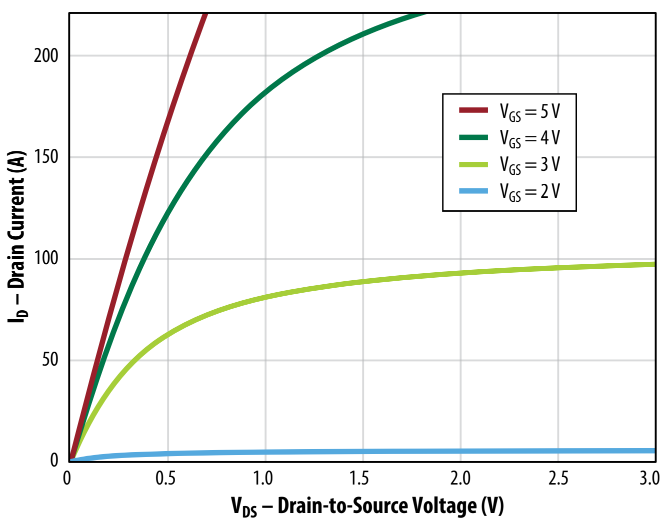


Figure 2: Typical Transfer Characteristics

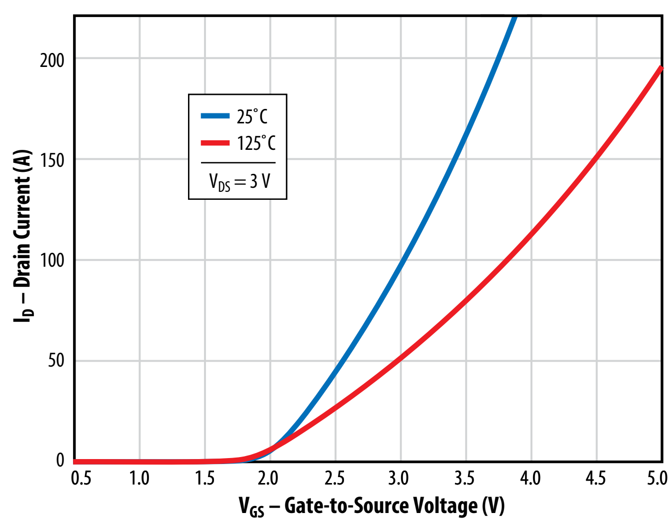


Figure 3: Typical $R_{DS(on)}$ vs. V_{GS} for Various Drain Currents

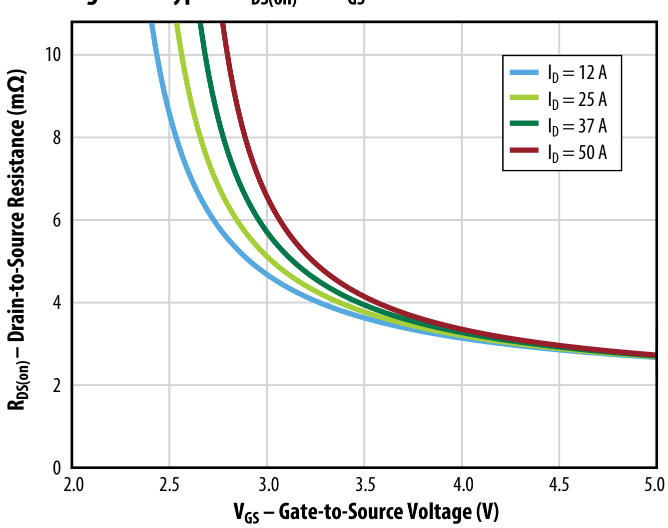


Figure 4: Typical $R_{DS(on)}$ vs. V_{GS} for Various Temperatures

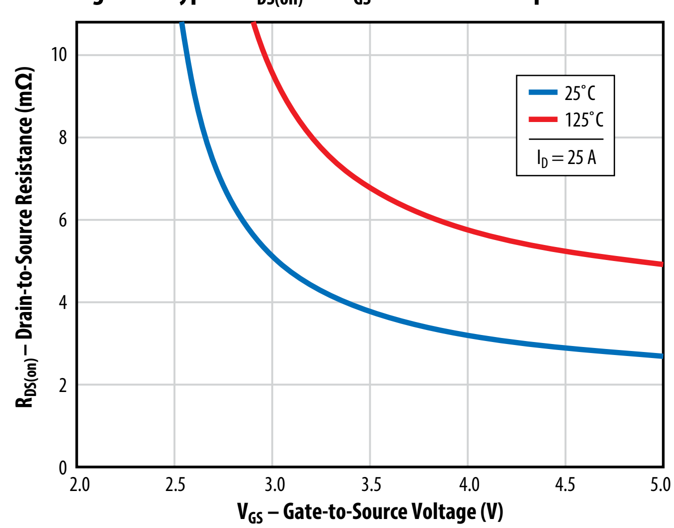


Figure 5a: Typical Capacitance (Linear Scale)

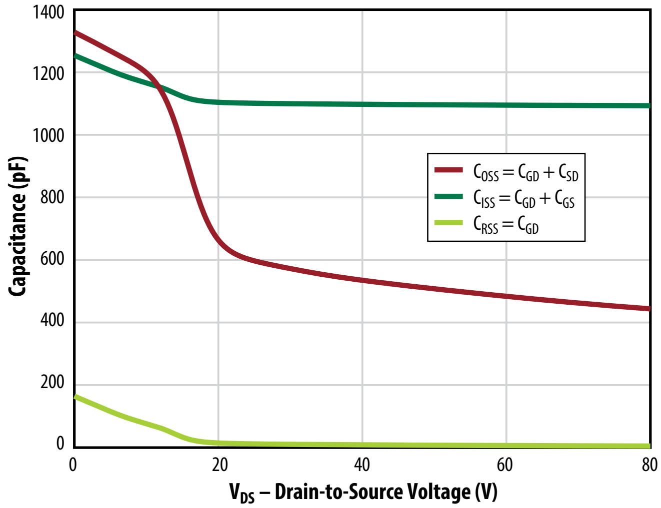


Figure 5b: Typical Capacitance (Log Scale)

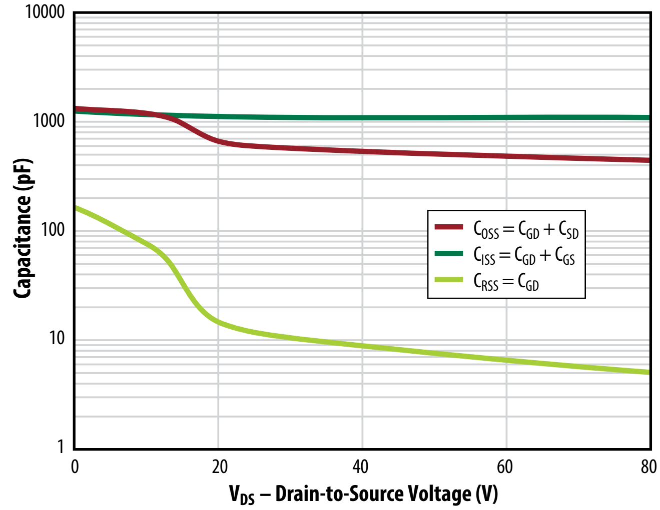


Figure 5c: Typical Output Charge and C_{OSS} Stored Energy

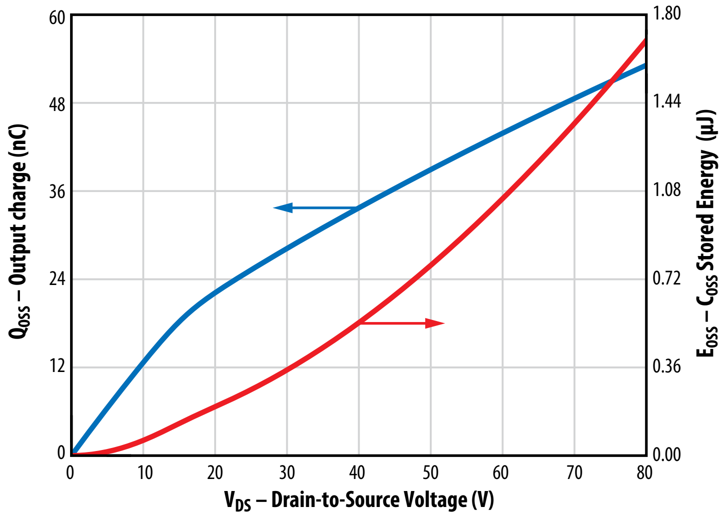


Figure 6: Typical Gate Charge

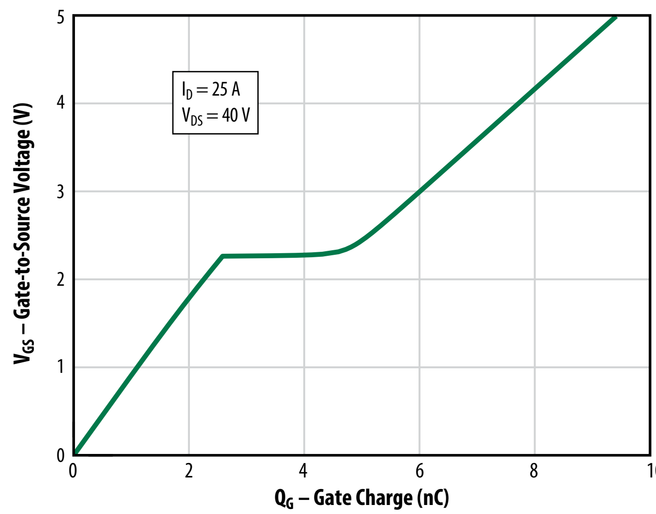
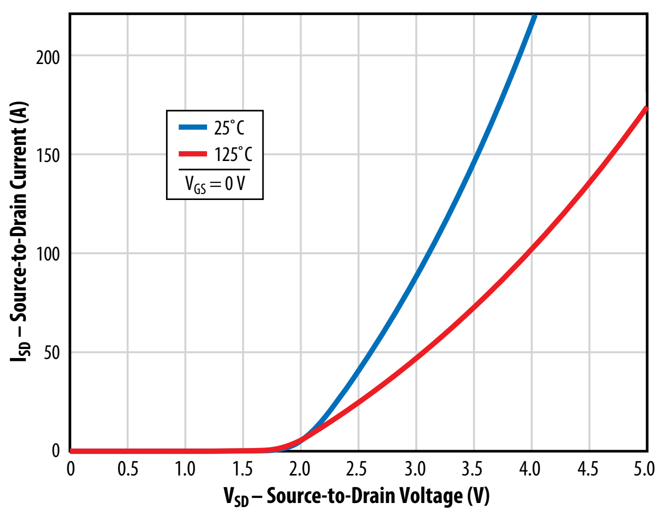


Figure 7: Typical Reverse Drain-Source Characteristics



Note: Negative gate drive voltage increases the reverse drain-source voltage. EPC recommends 0 V for OFF.

Figure 8: Typical Normalized On-State Resistance vs. Temp.

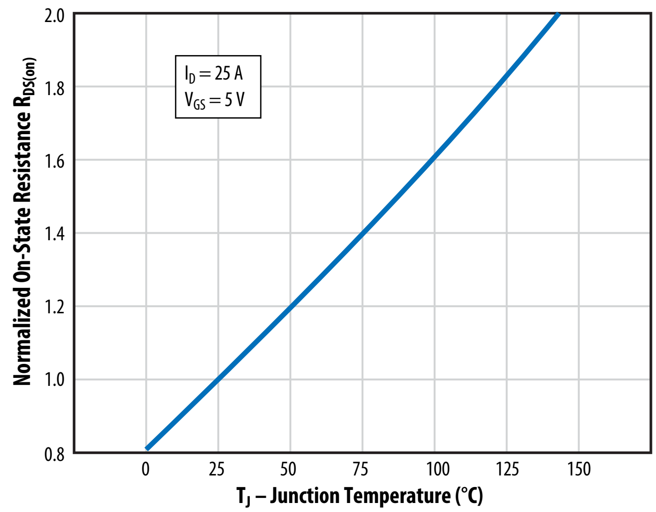


Figure 9: Typical Normalized Threshold Voltage vs. Temperature

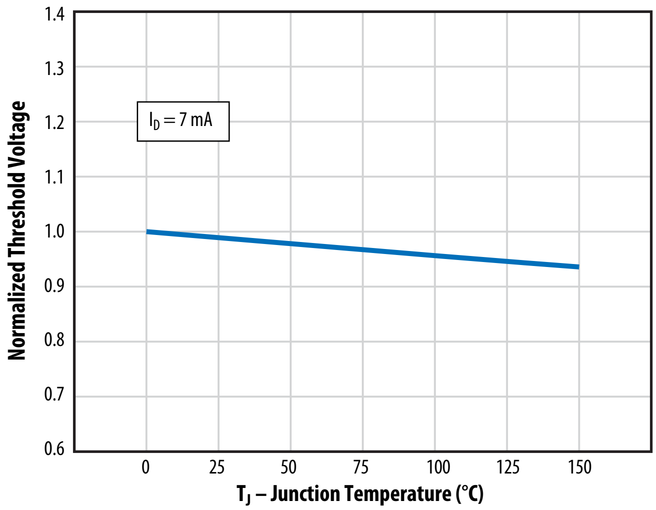


Figure 10: Typical Transient Thermal Response Curves

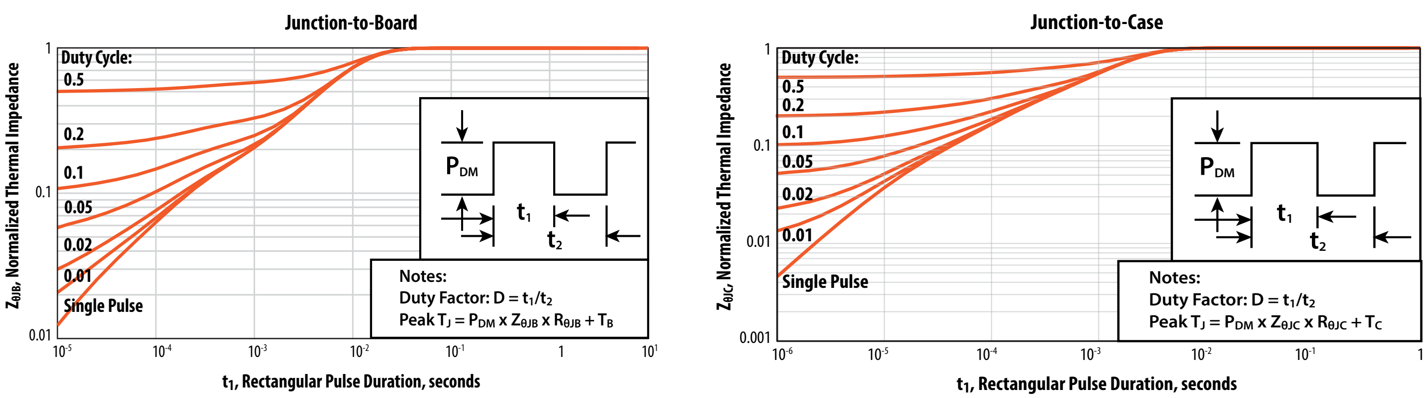
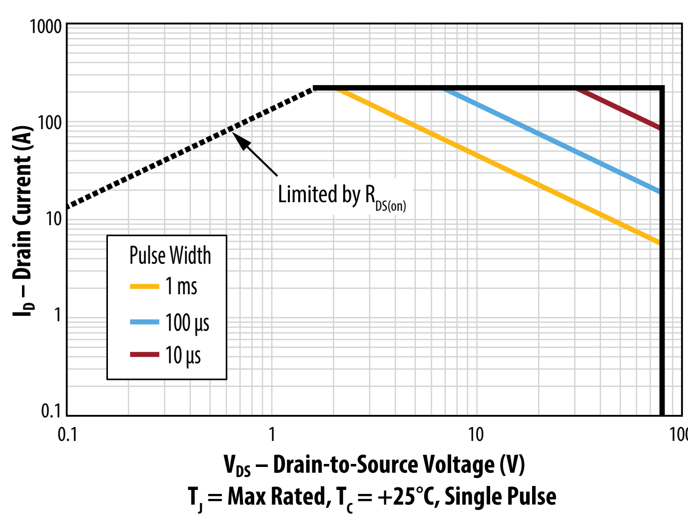
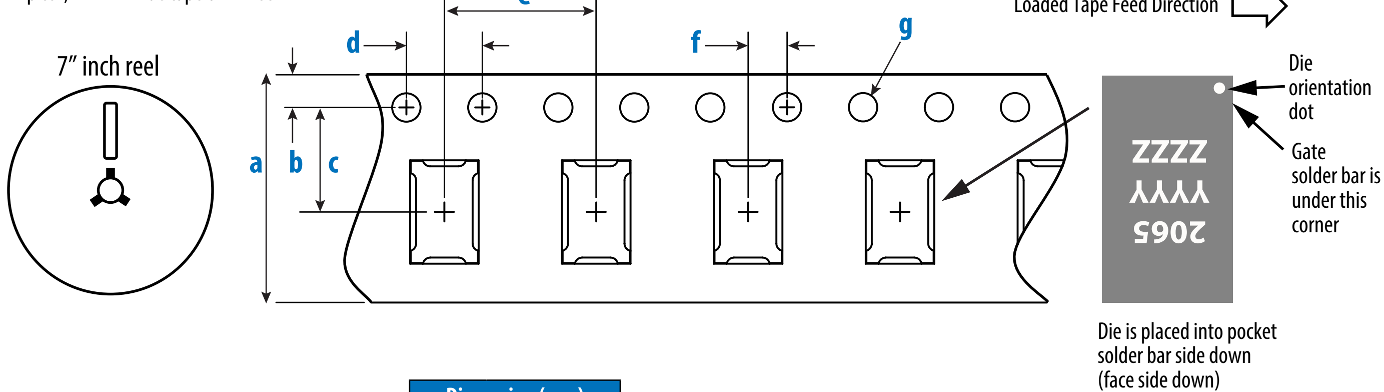


Figure 11: Safe Operating Area



TAPE AND REEL CONFIGURATION

8 mm pitch, 12 mm wide tape on 7" reel

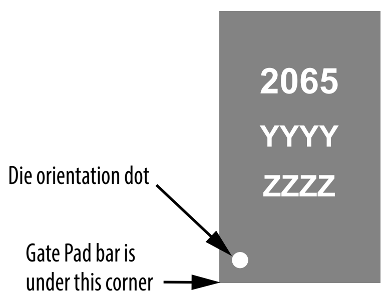


EPC2065 (Note 1)	Dimension (mm) Target	MIN	MAX
a	12.00	11.90	12.30
b	1.75	1.65	1.85
c (Note 2)	5.50	5.45	5.55
d	4.00	3.90	4.10
e	8.00	7.90	8.10
f (Note 2)	2.00	1.95	2.05
g	1.50	1.50	1.60

Note 1: MSL 1 (moisture sensitivity level 1) classified according to IPC/JEDEC industry standard.

Note 2: Pocket position is relative to the sprocket hole measured as true position of the pocket, not the pocket hole.

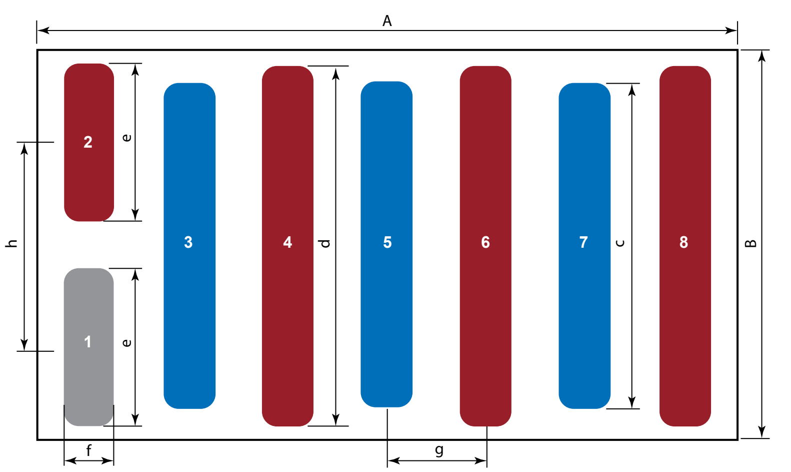
DIE MARKINGS



Part Number	Laser Markings: Part # Marking Line 1	Lot_Date Code Marking Line 2	Lot_Date Code Marking Line 3
EPC2065	2065	YYYY	ZZZZ

DIE OUTLINE

Solder Bump View



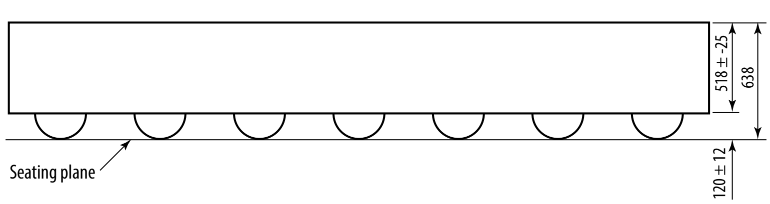
DIM	Micrometers MIN	Nominal	MAX
A	3470	3500	3530
B	1920	1950	1980
c		1625	
d		1800	
e		775	
f		250	
g		500	
h		1025	

Pad 1 is Gate;

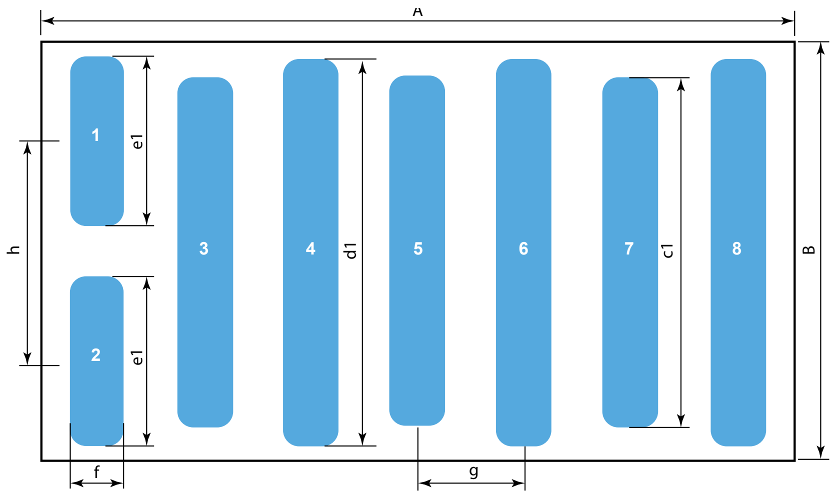
Pads 2 ,4, 6, 8 are Source;

Pads 3, 5, 7 are Drain;

Side View



RECOMMENDED LAND PATTERN
(units in µm)



Land pattern is solder mask defined.

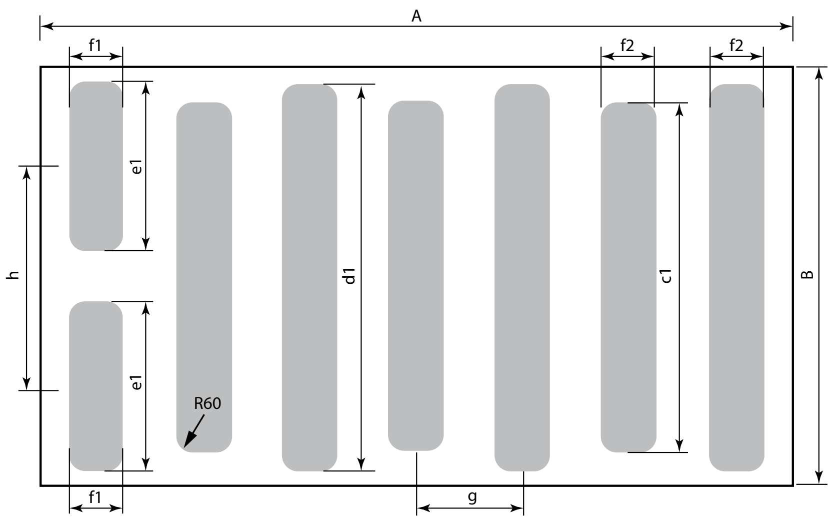
Pad 1 is Gate;

Pads 2 ,4, 6, 8 are Source;

Pads 3, 5, 7 are Drain;

DIM	Nominal
A	3500
B	1950
c1	1605
d1	1780
e1	755
f	230
g	500
h	1025

RECOMMENDED STENCIL DRAWING
(units in µm)



DIM	Nominal
A	3500
B	1950
c1	1605
d1	1780
e1	755
f1	230
f2	210
g	500
h	1025

Recommended stencil should be 4 mil (100 µm) thick, must be laser cut, openings per drawing.

Intended for use with SAC305 Type 4 solder, reference 88.5% metals content.

The corner has a radius of R60.

Split stencil design can be provided upon request, but EPC has tested this stencil design and not found any scooping issues.

Additional assembly resources available at https://epc-co.com/epc/design-support