Data Sheet

ACPL-K71T, ACPL-K72T, ACPL-K74T, ACPL-K75T

Automotive High-Speed Low-Power Digital Optocouplers with R^2Coupler™ Isolation and AEC-Q100 Grade 1 Qualification

Description

The Broadcom® ACPL-K71T and ACPL-K72T are a high-speed digital CMOS optocoupler package suitable for emerging electric vehicle applications. The ACPL-K74T and ACPL-K75T are dual-channel equivalents of the ACPL-K71T and ACPL-K72T, respectively. All products are available in a stretched SO-8 package outline, which is designed to be compatible with standard surface-mount processes.

The ACPL-K71T and ACPL-K74T have a high-speed mode with the fastest propagation delay (maximum 35 ns at I_F = 10 mA), whereas the ACPL-K72T and ACPL-K75T have a low-power mode with the lowest LED drive current of 4 mA for standard digital isolation switching.

Each channel of the digital optocoupler has a CMOS detector IC with an integrated photodiode, a high-speed transimpedance amplifier, and a voltage comparator with an output driver.

The Broadcom R^2Coupler™ provides reinforced insulation and reliability that deliver safe signal isolation critical in automotive and high-temperature industrial applications.

Features

- Qualified to AEC-Q100 Grade 1 test guidelines
- Automotive wide temperature range: –40°C to 125°C
- High temperature and reliability; high-speed digital interface for automotive applications
- 5V CMOS compatibility
- 40-kV/µs common-mode rejection at V_{CM} = 1000V typ.
- Low propagation delay:
  - ACPL-K71T, ACPL-K74T: 25 ns typ. @ I_F = 10 mA
  - ACPL-K72T, ACPL-K75T: 60 ns typ. @ I_F = 4 mA
- Worldwide safety approval:
  - UL 1577 approval, 5 kV_{RMS} /1 minute
  - CSA approval
  - EN IEC 60747-5-5

Applications

- CAN buses and SPI communication interfaces
- High-temperature digital/analog signal isolation
- Automotive IPM drivers for DC-DC converters and motor inverters
- Power transistor isolation

CAUTION! Take normal static precautions in the handling and assembly of this component to prevent damage, degradation, or both that might be induced by electrostatic discharge (ESD).

Functional Diagrams

Figure 1: ACPL-K71T/ACPL-K72T

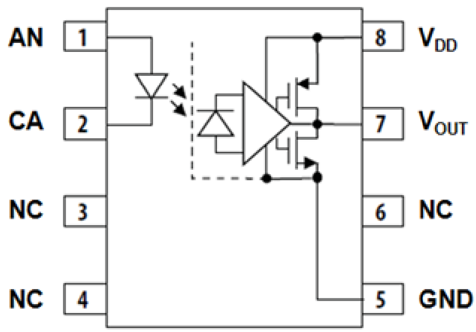


Table 1: Truth Table

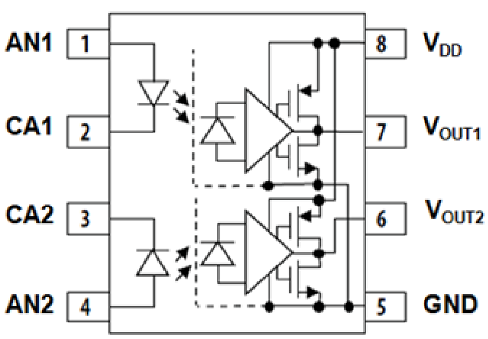
LED	V_{OUT}
ON	LOW
OFF	HIGH

NOTE: Connecting a 0.1-μF bypass capacitor between pins 5 and 8 is recommended.

Table 2: Pin Assignments for the ACPL-K71T/ACPL-K72T

Pin No.	Pin Name	Description	Pin No.	Pin Name	Description
1	AN	Anode	5	GND	Ground
2	CA	Cathode	6	NC	No Connection
3	NC	No Connection	7	V_{OUT}	Output
4	NC	No Connection	8	V_{DD}	Power Supply

Figure 2: ACPL-K74T/ACPL-K75T



NOTE: Connecting a 0.1-μF bypass capacitor between pins 5 and 8 is recommended.

Table 3: Pin Assignments for the ACPL-K74T/ACPL-K75T

Pin No.	Pin Name	Description	Pin No.	Pin Name	Description
1	AN1	Anode 1	5	GND	Ground
2	CA1	Cathode 1	6	V_{OUT2}	Output 2
3	CA2	Cathode 2	7	V_{OUT1}	Output 1
4	AN2	Anode 2	8	V_{DD}	Power Supply

Ordering Information

Part Number	Option (RoHS Compliant)	Package	Surface Mount	Tape and Reel	UL 5000 V_{RMS}/ 1-Minute Rating	EN IEC 60747-5-5	Quantity
ACPL-K71T	-000E	Stretched SO-8	X		X		80 per tube
	-060E		X		X	X	80 per tube
	-500E		X	X	X		1000 per reel
	-560E		X	X	X	X	1000 per reel
ACPL-K72T	-000E	Stretched SO-8	X		X		80 per tube
	-060E		X		X	X	80 per tube
	-500E		X	X	X		1000 per reel
	-560E		X	X	X	X	1000 per reel
ACPL-K74T	-000E	Stretched SO-8	X		X		80 per tube
	-060E		X		X	X	80 per tube
	-500E		X	X	X		1000 per reel
	-560E		X	X	X	X	1000 per reel
ACPL-K75T	-000E	Stretched SO-8	X		X		80 per tube
	-060E		X		X	X	80 per tube
	-500E		X	X	X		1000 per reel
	-560E		X	X	X	X	1000 per reel

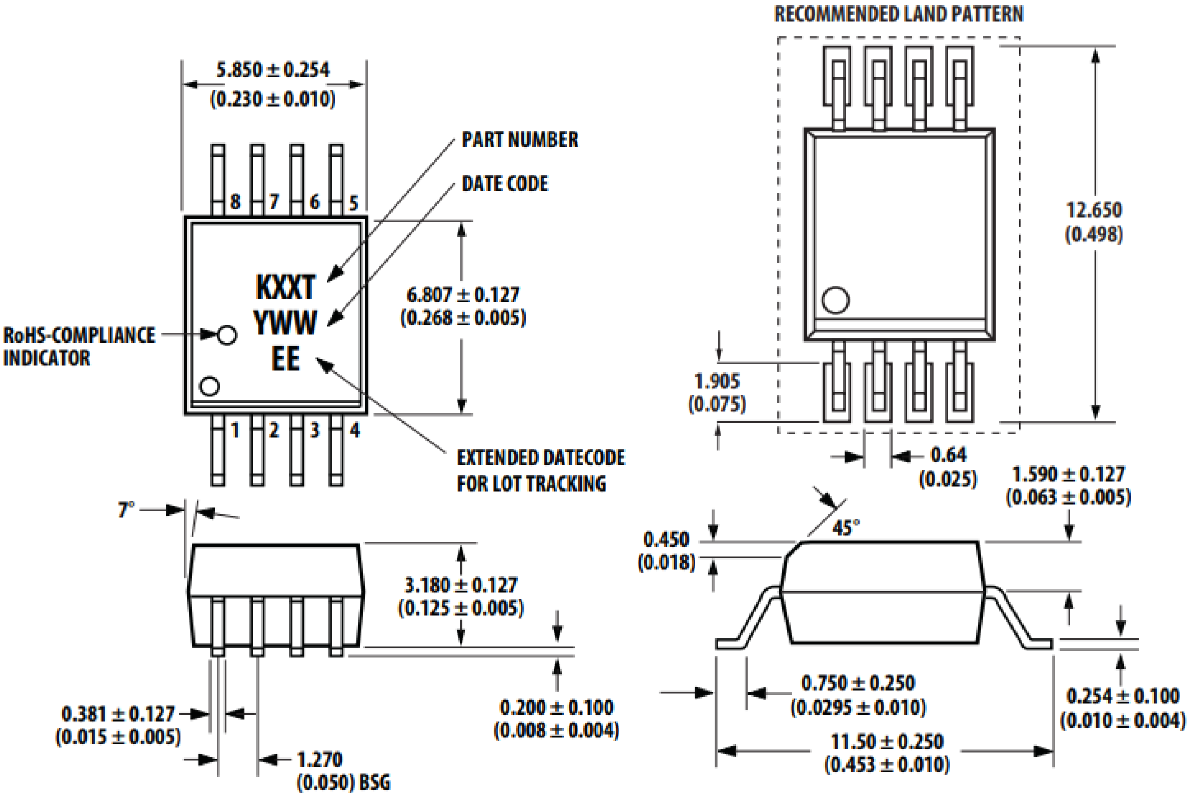
To form an order entry, choose a part number from the Part Number column and combine it with the desired option from the Option column.

Example 1:

Use ACPL-K71T-560E to order the product in an SSO-8 surface-mount package in tape and reel packaging with EN IEC 60747-5-5 safety approval and RoHS compliance.

Packaging option data sheets are available. Contact your Broadcom sales representative or authorized distributor for information.

Package Outline Dimensions (Stretched SO-8)



Dimensions in millimeters and (inches).

Note:
Lead coplanarity = 0.1 mm (0.004 inches).
Floating lead protrusion: 0.25 mm (10 mils) max.

Recommended Pb-Free IR Profile

Recommended reflow condition is as per JEDEC standard J-STD-020 (latest revision).

NOTE: Use nonhalide flux.

Regulatory Information

The ACPL-K71T, ACPL-K72T, ACPL-K74T, and ACPL-K75T are approved by the following organizations.

Table 4: Regulatory Information

UL	UL 1577, component recognition program up to V_{ISO} = 5 kV_{RMS}.
CSA	CAN/CSA-C22.2 No. 62368-1.
EN IEC	EN IEC 60747-5-5. V_{IORM} = 1140 V_{PEAK} V_{IOTM} = 8000 V_{PEAK}

Insulation and Safety-Related Specifications

Parameter	Symbol	Value	Units	Conditions
Minimum External Air Gap (Clearance)	L(101)	8	mm	Measured from input terminals to output terminals, shortest distance through the air.
Minimum External Tracking (Creepage)	L(102)	8	mm	Measured from input terminals to output terminals, shortest distance path along the body.
Minimum Internal Plastic Gap (Internal Clearance)	—	0.08	mm	The shortest straight-line distance through insulation between conductor and conductor.
Tracking Resistance (Comparative Tracking Index)	CTI	175	V	EN IEC 60112/VDE 0303-1.
Isolation Group	—	IIIa	—	Material Group (IEC 60664-1).

EN IEC 60747-5-5 Insulation Characteristics (Option 060 and 560 Only)

Description	Symbol	Characteristic	Units
Overvoltage Category per IEC 60664-1 For rated mains voltage ≤600 V_{RMS}	—	I-IV	—
Climatic Classification	—	40/125/21	—
Pollution Degree (IEC 60664-1)	—	2	—
Maximum Working Insulation Voltage	V_{IORM}	1140	V_{PEAK}
Input to Output Test Voltage, Method b $V_{IORM} \times 1.875 = V_{PR}$, 100% Production Test with t_m = 1 second, Partial Discharge < 5 pC	V_{PR}	2137	V_{PEAK}
Input to Output Test Voltage, Method a $V_{IORM} \times 1.6 = V_{PR}$, Type and Sample Test, t_m = 10 seconds, Partial Discharge < 5 pC	V_{PR}	1824	V_{PEAK}
Highest Allowable Overvoltage (Transient Overvoltage, t_{ini} = 60 seconds)	V_{IOTM}	8000	V_{PEAK}
Safety Limiting Values (Maximum Values Allowed in the Event of a Failure) Case Temperature Input Current Output Power	 T_S $I_{S,INPUT}$ $P_{S,OUTPUT}$	 175 230 600	 °C mA mW
Insulation Resistance at T_S, V_{IO} = 500V	R_S	10^9	Ω

Absolute Maximum Ratings

Parameter	Symbol	Min.	Max.	Units	Test Conditions
Storage Temperature	T_S	–55	130	°C	—
Ambient Operating Temperature	T_A	–40	125	°C	—
Supply Voltages	V_{DD}	0	6.5	V	—
Output Voltage	V_O	–0.5	V_{DD} + 0.5	V	—
Average Forward Input Current	I_F	—	20.0	mA	—
Peak Transient Input Current	$I_{F(TRAN)}$	—	1	A	≤1-μs pulse width, 300 pps
		—	80	mA	≤1-μs pulse width, <10% duty cycle
Reverse Input Voltage	V_R	—	5	V	—
Input Power Dissipation	P_I	—	40	mW	—
Output Power Dissipation	P_O	—	30	mW	—
Lead Solder Temperature	—	260°C for 10 seconds, 1.6 mm below the seating plane.			

Recommended Operating Conditions

Parameter	Symbol	Min.	Max.	Units
Supply Voltage	V_{CC}	3.0	5.5	V
Operating Temperature	T_A	–40	125	°C
Forward Input Current	$I_{F(ON)}$	4	15	mA
Forward Off State Voltage	$V_{F(OFF)}$	—	0.8	V
Input Threshold Current	I_{TH}	—	3.5	mA

Electrical Specifications

Over recommended temperature T_A = –40°C to 125°C, 3.0V ≤ V_{DD} ≤ 5.5V. All typical specifications are at T_A = 25°C, V_{DD} = 5V.

Parameter	Symbol	Min.	Typ.	Max.	Units	Test Conditions	Figure
LED Forward Voltage	V_F	1.45	1.5	1.75	V	I_F = 10 mA, T_A = 25°C	—
		1.25	1.5	1.85	V	I_F = 10 mA	
V_F Temperature Coefficient	—	—	–1.5	—	mV/°C	—	—
Input Capacitance	C_{IN}	—	90	—	pF	—	—
Input Reverse Breakdown Voltage	BV_R	5.0	—	—	V	I_R = 10 μA	—
Logic High Output Voltage	V_{OH}	V_{DD} – 0.6	—	—	V	I_{OH} = –3.2 mA	6
Logic Low Output Voltage	V_{OL}	—	—	0.6	V	I_{OL} = 4 mA	5
Logic Low Output Supply Current (Per Channel)	I_{DDL}	—	0.9	1.5	mA	—	—
Logic High Output Supply Current (Per Channel)	I_{DDH}	—	0.9	1.5	mA	—	—

ACPL-K71T, ACPL-K74T High-Speed Mode Switching Specifications

Over recommended temperature T_A = –40°C to 125°C, 4.5V ≤ V_{DD} ≤ 5.5V. All typical specifications are at T_A = 25°C, V_{DD} = 5V.

Parameter	Symbol	Min.	Typ.	Max.	Units	Test Conditions	Figure	Notes
Propagation Delay Time to Logic Low Output	t_{PHL}	—	25	35	ns	V_{IN} = 4.5V to 5.5V, R_{IN} = 390Ω ±5%, C_{IN} = 100 pF, C_L = 15 pF, V_{THL} = 0.8V, V_{TLH} = 80% of V_{DD}	7,8,13	a, b, c
Propagation Delay Time to Logic High Output	t_{PLH}	—	25	35	ns			
Pulse Width Distortion	PWD	—	0	12	ns			
Propagation Delay Skew	t_{PSK}	—	9	15	ns			
Output Rise Time (10% to 90%)	t_R	—	10	—	ns	—	—	—
Output Fall Time (90% to 10%)	t_F	—	10	—	ns	—	—	—
Common Mode Transient Immunity at Logic High Output	$\|CM_H\|$	15	25	—	kV/µs	V_{IN} = 0V, R_1 = 390Ω ±5%, C_{IN} = 100 pF, V_{CM} = 1000V, T_A = 25°C	14	d
Common Mode Transient Immunity at Logic Low Output	$\|CM_L\|$	15	25	—	kV/µs	V_{IN} = 4.5V to 5.5V, R_1 = 390Ω ±5%, C_{IN} = 100 pF, V_{CM} = 1000V, T_A = 25°C	14	e

a. The t_{PHL} propagation delay is measured from 50% (V_{IN} or I_F) on the rising edge of the input pulse to the 0.8V of V_{DD} of the falling edge of the V_O signal. The t_{PLH} propagation delay is measured from 50% (V_{IN} or I_F) on the rising edge of the input pulse to the 80% level of the rising edge of the V_O signal.

b. PWD is defined as $|t_{PHL} – t_{PLH}|$.

c. t_{PSK} is equal to the magnitude of the worst-case difference in t_{PHL} and/or t_{PLH} that will be seen between units at any given temperature within the recommended operating conditions.

d. CM_H is the maximum tolerable rate of rise of the common mode voltage to ensure that the output will remain in a high logic state.

e. CM_L is the maximum tolerable rate of fall of the common mode voltage to ensure that the output will remain in a low logic state.

ACPL-K72T, ACPL-K75T Low-Power Mode Switching Specifications

Over recommended temperature T_A = –40°C to 125°C, 3.0V ≤ V_{DD} ≤ 5.5V. All typical specifications are at T_A = 25°C, V_{DD} = 5V.

Parameter	Symbol	Min.	Typ.	Max.	Units	Test Conditions	Figure	Notes
Propagation Delay Time to Logic Low Output	t_{PHL}	—	60	100	ns	I_F = 4 mA, C_L = 15 pF, V_{THL} = 0.8V, V_{TLH} = 80% of V_{DD}	9,10,11, 12,15	a, b ,c
Propagation Delay Time to Logic High Output	t_{PLH}	—	35	100	ns			
Pulse Width Distortion	PWD	—	25	50	ns			
Propagation Delay Skew	t_{PSK}	—	—	60	ns			
Output Rise Time (10% to 90%)	t_R	—	10	—	ns	—	—	—
Output Fall Time (90% to 10%)	t_F	—	10	—	ns	—	—	—
Common Mode Transient Immunity at Logic High Output	$\|CM_H\|$	25	40	—	kV/µs	V_{IN} = 0V, R1 = 350Ω ±5%, R2 = 350Ω ±5%, V_{CM} = 1000V, T_A = 25°C	16	d
Common Mode Transient Immunity at Logic Low Output	$\|CM_L\|$	25	40	—	kV/µs	V_{IN} = 4.5V to 5.5V, R1 = 350Ω ±5%, R2 = 350Ω ±5%, V_{CM} = 1000V, T_A = 25°C	16	e

a. The t_{PHL} propagation delay is measured from 50% (V_{IN} or I_F) on the rising edge of the input pulse to the 0.8V of V_{DD} of the falling edge of the V_O signal. The t_{PLH} propagation delay is measured from 50% (V_{IN} or I_F) on the rising edge of the input pulse to the 80% level of the rising edge of the V_O signal.

b. PWD is defined as $|t_{PHL} – t_{PLH}|$.

c. t_{PSK} is equal to the magnitude of the worst-case difference in t_{PHL} and/or t_{PLH} that will be seen between units at any given temperature within the recommended operating conditions.

d. CM_H is the maximum tolerable rate of rise of the common mode voltage to ensure that the output will remain in a high logic state.

e. CM_L is the maximum tolerable rate of fall of the common mode voltage to ensure that the output will remain in a low logic state.

Package Characteristics

All typical at T_A = 25°C.

Parameter	Symbol	Min.	Typ.	Max.	Units	Test Conditions	Notes
Input-Output Momentary Withstand Voltage[a]	V_{ISO}	5000	—	—	V_{RMS}	RH ≤ 50%, t = 1 minute, T_A = 25°C	b, c
Input-Output Resistance	R_{I-O}	—	10^{14}	—	Ω	V_{I-O} = 500 V_{DC}	b
Input-Output Capacitance	C_{I-O}	—	0.6	—	pF	f = 1 MHz, T_A = 25°C	b

a. The input-output momentary withstand voltage is a dielectric voltage rating that should not be interpreted as an input-output continuous voltage rating.

b. The device is considered a two-terminal device: Pins 1, 2, 3, and 4 are shorted together, and pins 5, 6, 7, and 8 are shorted together.

c. In accordance with UL 1577, each optocoupler is proof-tested by applying an insulation test voltage > 6000 V_{RMS} for 1 second.

Performance Plots: Typical Logic Low Output Voltage vs. Logic Low Output

Figure 3: Typical Diode Input Forward Current Characteristic

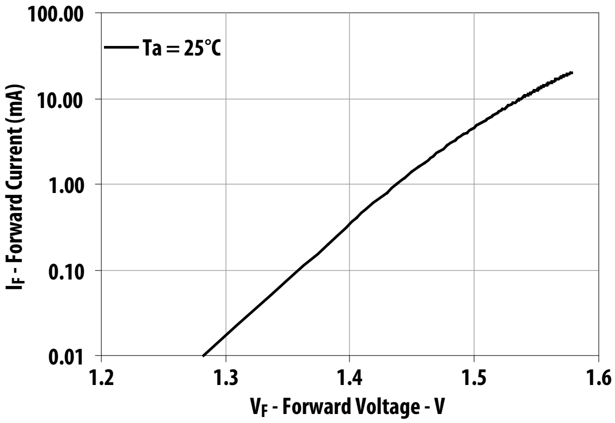


Figure 4: Typical Output Voltage vs. Input Forward Current

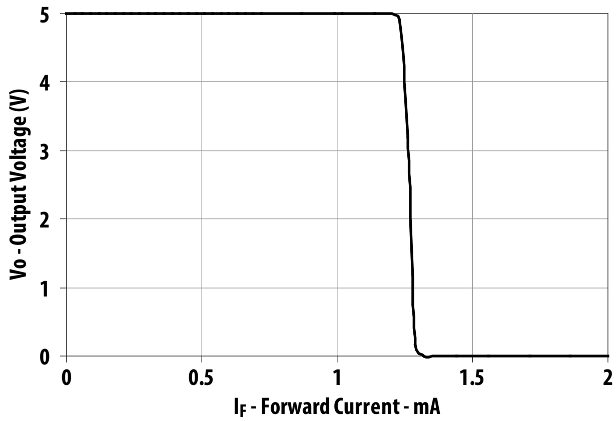


Figure 5: Typical Logic Low Output Voltage vs. Logic Low Output Current

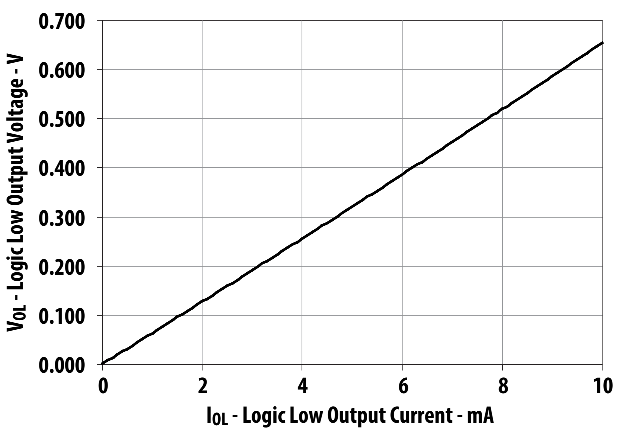


Figure 6: Typical Logic High Output Voltage vs. Logic High Output Current

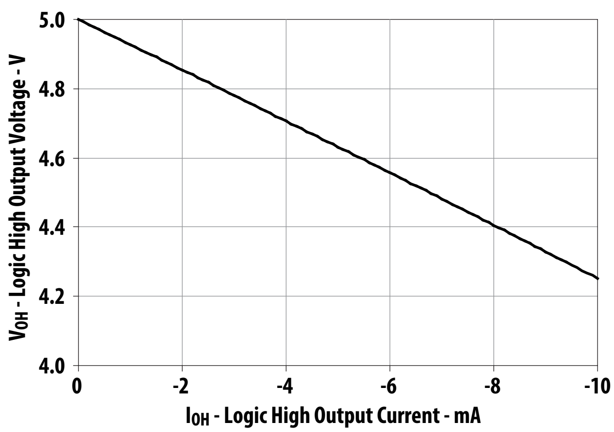


Figure 7: ACPL-K71T/K74T (High-Speed) Typical Propagation Delay vs. Temperature

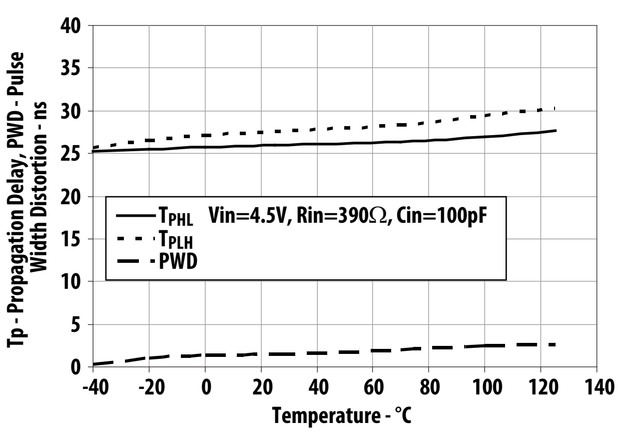


Figure 8: ACPL-K71T/K74T (High-Speed) Typical Propagation Delay vs. Input Forward Current

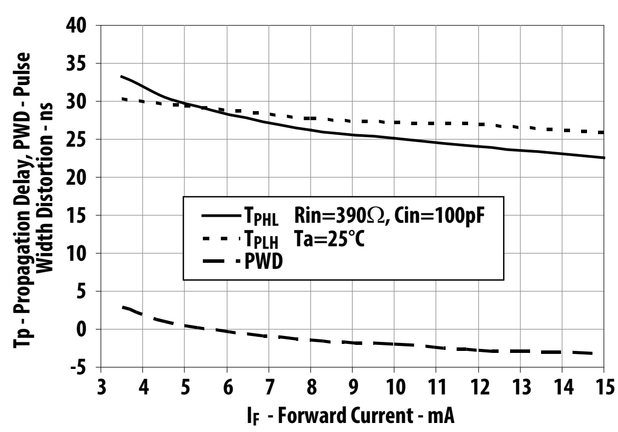


Figure 9: ACPL-K72T/K75T (5V) Typical Propagation Delay vs. Temperature

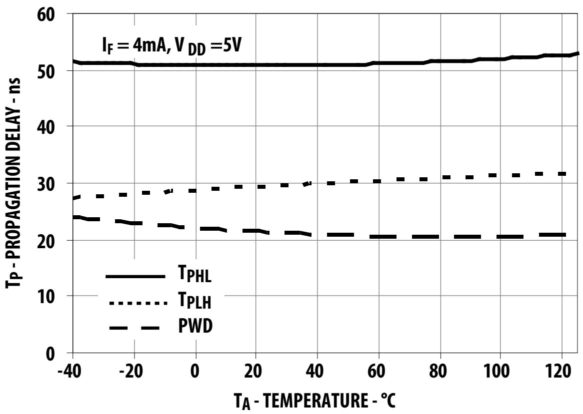


Figure 10: ACPL-K72T/K75T (5V) Typical Propagation Delay vs. Input Forward Current

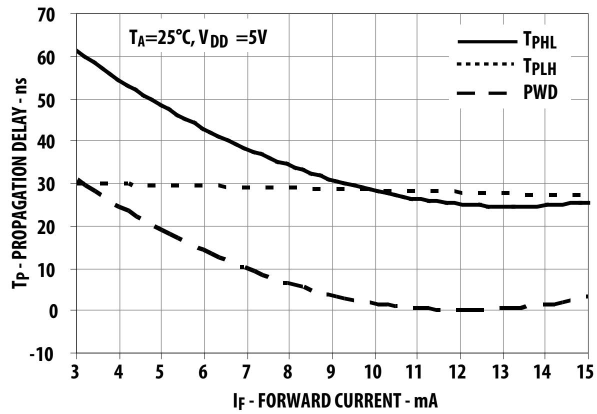


Figure 11: ACPL-K72T/K75T (3V) Typical Propagation Delay vs. Temperature

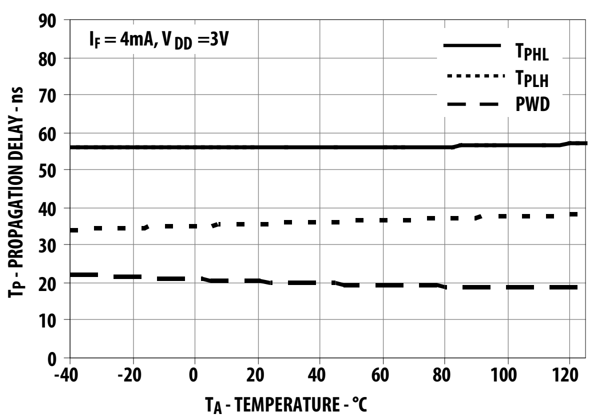
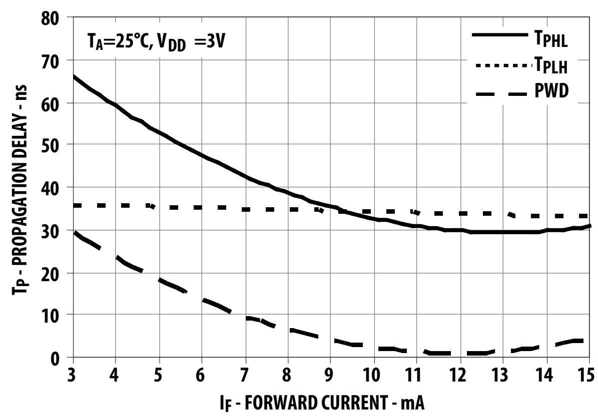


Figure 12: ACPL-K72T/K75T (3V) Typical Propagation Delay vs. Input Forward Current



ACPL-K71T/K74T High-Speed Mode

Figure 13: High-Speed Mode Switching Test Circuit and Typical Waveform

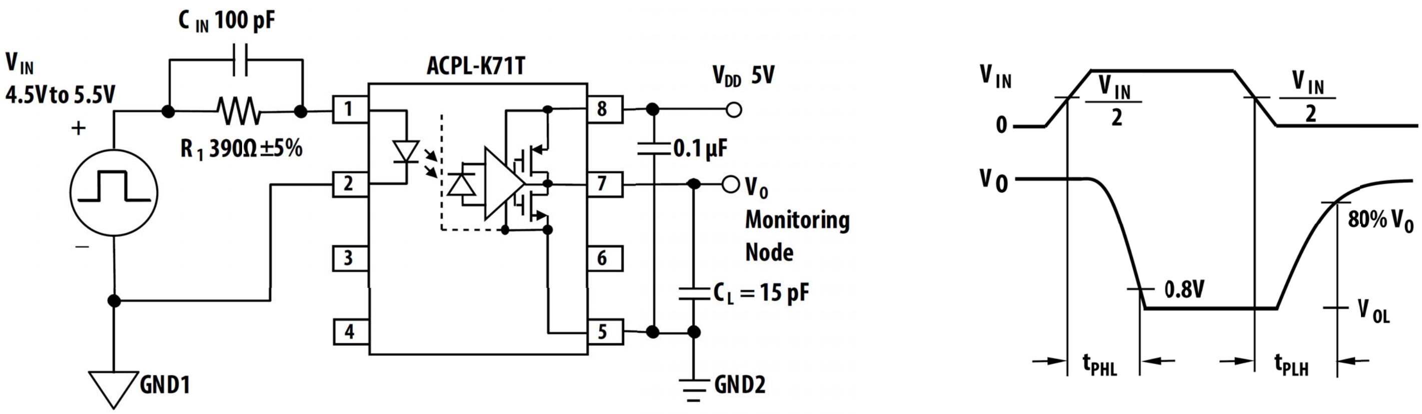
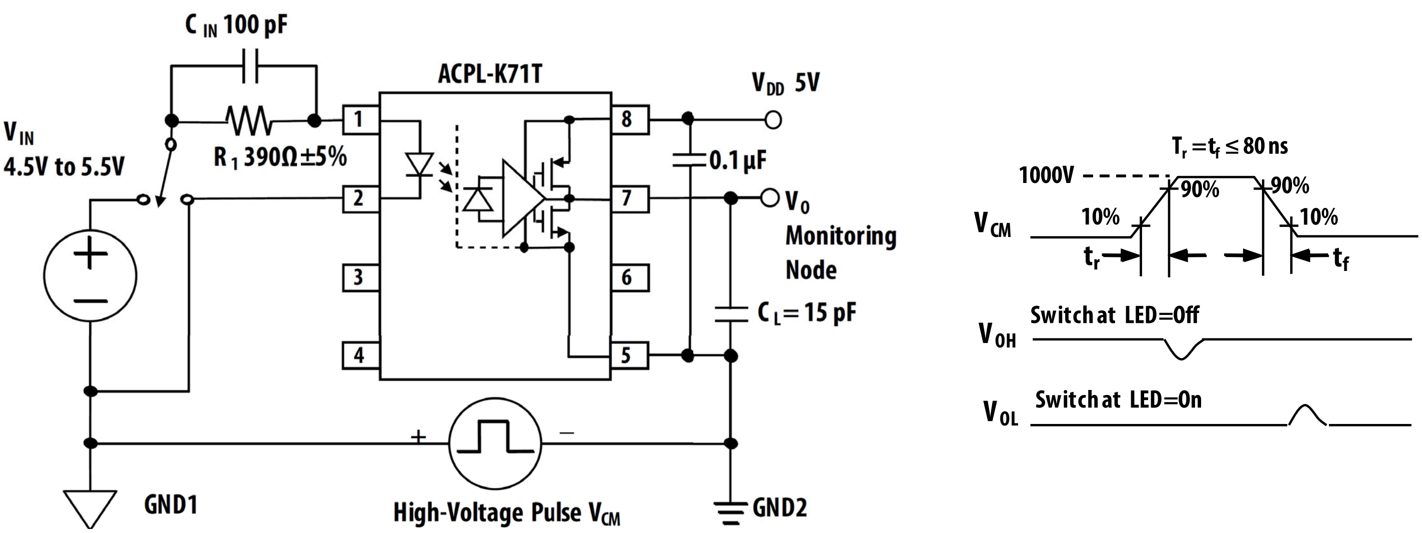
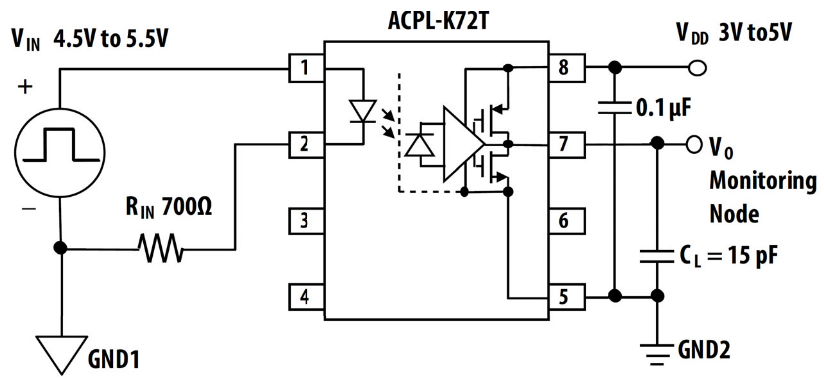


Figure 14: High-Speed Mode CMR Test Circuit and Typical Waveform



ACPL-K72T/K75T Low-Power Mode

Figure 15: Low-Power Mode Switching Test Circuit and Typical Waveform



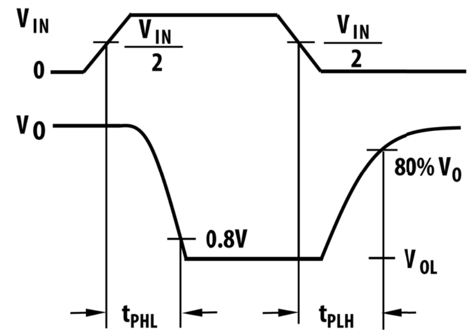
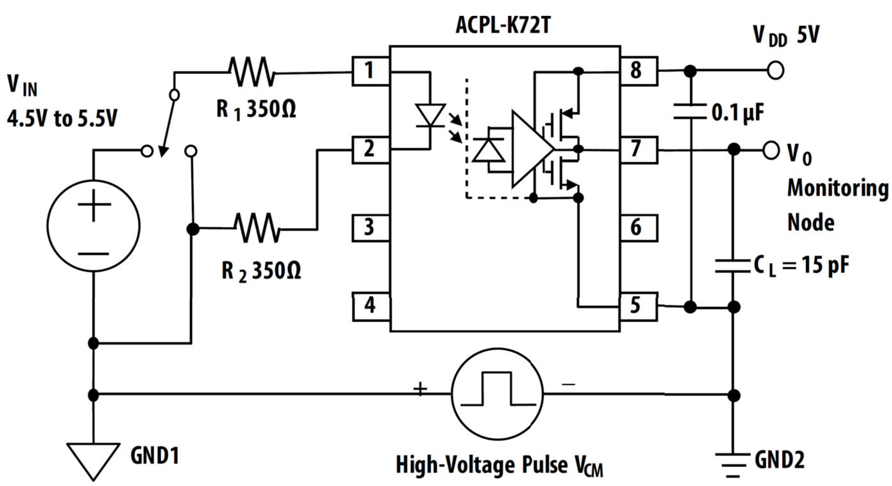
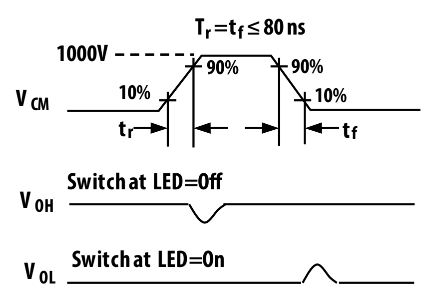


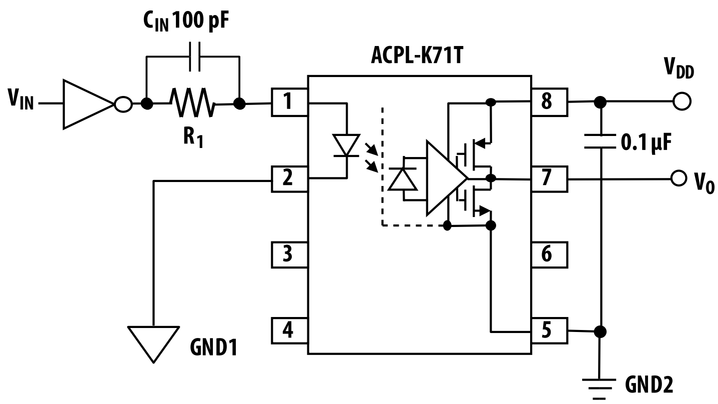
Figure 16: Low-Power Mode CMR Test Circuit





Recommended Application Circuits

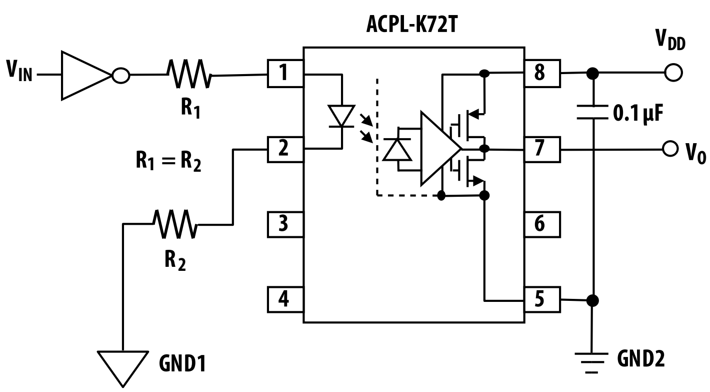
Figure 17: Recommended Application Circuit for ACPL-K71T/K74T High-Speed Performance



Truth Table

V_{IN}	LED	Vo
LOW	ON	LOW
HIGH	OFF	HIGH

Figure 18: Recommended Application Circuit for ACPL-K72T/K75T Low-Power Performance



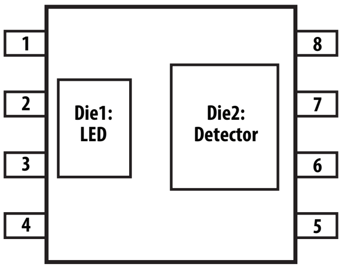
Truth Table

V_{IN}	LED	Vo
LOW	ON	LOW
HIGH	OFF	HIGH

Thermal Resistance Model for the ACPL-K71T/K72T

Figure 19 shows the diagram of the ACPL-K71T/K72T for measurement. Here, one die is heated first, and the temperatures of all the dice are recorded after thermal equilibrium is reached. Then, the second die is heated, and all the dice temperatures are recorded. With the known ambient temperature, die junction temperature, and power dissipation, the thermal resistance can be calculated. The thermal resistance calculation can be cast in matrix form. This yields a 2-by-2 matrix for our case of two heat sources.

Figure 19: Diagram of the ACPL-K71T/K72T for Measurement



$$\begin{vmatrix} R_{11} & R_{12} \\ R_{21} & R_{22} \end{vmatrix} \times \begin{vmatrix} P_1 \\ P_2 \end{vmatrix} = \begin{vmatrix} \Delta T_1 \\ \Delta T_2 \end{vmatrix}$$

R_{11}: Thermal resistance of Die1 due to heating of Die1 (°C/W)
R_{12}: Thermal resistance of Die1 due to heating of Die2 (°C/W)

R_{21}: Thermal resistance of Die2 due to heating of Die1 (°C/W)
R_{22}: Thermal resistance of Die2 due to heating of Die2 (°C/W)

P_1: Power dissipation of Die1 (W)
P_2: Power dissipation of Die2 (W)

T_1: Junction temperature of Die1 due to heat from all dice (°C)
T_2: Junction temperature of Die2 due to heat from all dice (°C)

T_a: Ambient temperature (°C)

ΔT_1: Temperature difference between Die1 junction and ambient (°C)
ΔT_2: Temperature difference between Die2 junction and ambient (°C)

$T_1 = (R_{11} \times P_1 + R_{12} \times P_2) + T_a$
$T_2 = (R_{21} \times P_1 + R_{22} \times P_2) + T_a$

Measurement data on a low K board:

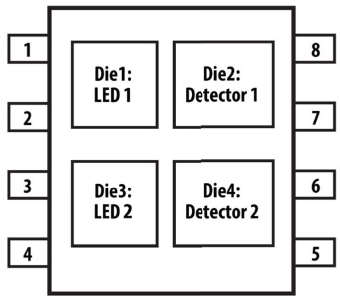
R_{11}	$R_{12} = R_{21}$	R_{22}
160°C/W	74°C/W	115°C/W

Thermal Resistance Model for the ACPL-K74T/K75T

Figure 20 shows the diagram of the ACPL-K74T/K75T for measurement. Here, one die is heated first, and the temperatures of all the dice are recorded after thermal equilibrium is reached. Then, the second, third, and fourth die are heated, and all the dice temperatures are recorded. With the known ambient temperature, die junction temperature, and power dissipation, the thermal resistance can be calculated. The thermal resistance calculation can be cast in matrix form. This yields a 4-by-4 matrix for our case of two heat sources.

$$\begin{vmatrix} R_{11} & R_{12} & R_{13} & R_{14} \\ R_{21} & R_{22} & R_{23} & R_{24} \\ R_{31} & R_{32} & R_{33} & R_{34} \\ R_{41} & R_{42} & R_{43} & R_{44} \end{vmatrix} \times \begin{vmatrix} P_1 \\ P_2 \\ P_3 \\ P_4 \end{vmatrix} = \begin{vmatrix} \Delta T_1 \\ \Delta T_2 \\ \Delta T_3 \\ \Delta T_4 \end{vmatrix}$$

Figure 20: Diagram of the ACPL-K74T/K75T for Measurement



R_{11}: Thermal resistance of Die1 due to heating of Die1 (°C/W)
R_{12}: Thermal resistance of Die1 due to heating of Die2 (°C/W)
R_{13}: Thermal resistance of Die1 due to heating of Die3 (°C/W)
R_{14}: Thermal resistance of Die1 due to heating of Die4 (°C/W)

R_{21}: Thermal resistance of Die2 due to heating of Die1 (°C/W)
R_{22}: Thermal resistance of Die2 due to heating of Die2 (°C/W)
R_{23}: Thermal resistance of Die2 due to heating of Die3 (°C/W)
R_{24}: Thermal resistance of Die2 due to heating of Die4 (°C/W)

R_{31}: Thermal resistance of Die3 due to heating of Die1 (°C/W)
R_{32}: Thermal resistance of Die3 due to heating of Die2 (°C/W)
R_{33}: Thermal resistance of Die3 due to heating of Die3 (°C/W)
R_{34}: Thermal resistance of Die3 due to heating of Die4 (°C/W)

R_{41}: Thermal resistance of Die4 due to heating of Die1 (°C/W)
R_{42}: Thermal resistance of Die4 due to heating of Die2 (°C/W)
R_{43}: Thermal resistance of Die4 due to heating of Die3 (°C/W)
R_{44}: Thermal resistance of Die4 due to heating of Die4 (°C/W)

P_1: Power dissipation of Die1 (W)
P_2: Power dissipation of Die2 (W)
P_3: Power dissipation of Die3 (W)
P_4: Power dissipation of Die4 (W)

T_1: Junction temperature of Die1 due to heat from all dice (°C)
T_2: Junction temperature of Die2 due to heat from all dice (°C)
T_3: Junction temperature of Die3 due to heat from all dice (°C)
T_4: Junction temperature of Die4 due to heat from all dice (°C)

T_a: Ambient temperature (°C)

ΔT_1: Temperature difference between Die1 junction and ambient (°C)
ΔT_2: Temperature difference between Die2 junction and ambient (°C)
ΔT_3: Temperature difference between Die3 junction and ambient (°C)
ΔT_4: Temperature difference between Die4 junction and ambient (°C)

$$T_1 = (R_{11} \times P_1 + R_{12} \times P_2 + R_{13} \times P_3 + R_{14} \times P_4) + T_a$$
$$T_2 = (R_{21} \times P_1 + R_{22} \times P_2 + R_{23} \times P_3 + R_{24} \times P_4) + T_a$$
$$T_3 = (R_{31} \times P_1 + R_{32} \times P_2 + R_{33} \times P_3 + R_{34} \times P_4) + T_a$$
$$T_4 = (R_{41} \times P_1 + R_{42} \times P_2 + R_{43} \times P_3 + R_{44} \times P_4) + T_a$$

Measurement data on a low K board:

R_{11}	R_{12}	R_{13}	R_{14}	R_{21}	R_{22}	R_{23}	R_{24}	R_{31}	R_{32}	R_{33}	R_{34}	R_{41}	R_{42}	R_{43}	R_{44}
160°C/W	76°C/W	76°C/W	76°C/W	76°C/W	115°C/W	76°C/W	76°C/W	76°C/W	76°C/W	160°C/W	76°C/W	76°C/W	76°C/W	76°C/W	115°C/W

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