

MOSFET – Power, Single, P-Channel, SOT-23

-30 V, -3.5 A

NTR4171P

Features

- Low $R_{DS(on)}$ at Low Gate Voltage
- Low Threshold Voltage
- High Power and Current Handling Capability
- This is a Pb-Free Device

Applications

- Load Switch
- Optimized for Battery and Load Management Applications in Portable Equipment like Cell Phones, PDA's, Media Players, etc.

MAXIMUM RATINGS ($T_J = 25^\circ\text{C}$ unless otherwise noted)

Parameter		Symbol	Value	Unit
Drain-to-Source Voltage		V_{DSS}	-30	V
Gate-to-Source Voltage		V_{GS}	± 12	V
Continuous Drain Current (Note 2)	Steady State	I_D	$T_A = 25^\circ\text{C}$	A
			$T_A = 85^\circ\text{C}$	
	$t \leq 5\text{ s}$		$T_A = 25^\circ\text{C}$	
Power Dissipation (Note 2)	Steady State	P_D	$T_A = 25^\circ\text{C}$	W
	$t \leq 5\text{ s}$			
Pulsed Drain Current	$t_p = 10\text{ }\mu\text{s}$	I_{DM}	-15.0	A
Operating Junction and Storage Temperature		T_J, T_{stg}	-55 to 150	$^\circ\text{C}$
Source Current (Body Diode)		I_S	-1.0	A
Lead Temperature for Soldering Purposes (1/8" from case for 10 s)		T_L	260	$^\circ\text{C}$

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

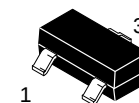
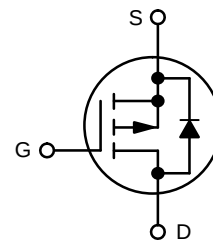
THERMAL RESISTANCE RATINGS

Parameter	Symbol	Max	Unit
Junction-to-Ambient – Steady State (Note 2)	$R_{\theta JA}$	260	$^\circ\text{C/W}$
Junction-to-Ambient – $t \leq 10\text{ s}$ (Note 2)	$R_{\theta JA}$	100	

2. Surface-mounted on FR4 board using 1 in sq pad size (Cu area = 1.127 in sq [2 oz] including traces)

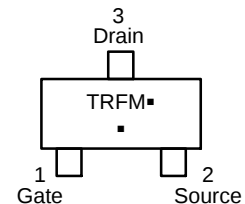
$V_{(BR)DSS}$	$R_{DS(on)} \text{ MAX}$	$I_D \text{ MAX}$
-30 V	75 m Ω @ -10 V	-2.2 A
	110 m Ω @ -4.5 V	-1.8 A
	150 m Ω @ -2.5 V	-1.0 A

P-CHANNEL MOSFET



**SOT-23
CASE 318
STYLE 21**

MARKING DIAGRAM/ PIN ASSIGNMENT



TRF = Specific Device Code
M = Date Code
■ = Pb-Free Package
(Note: Microdot may be in either location)

ORDERING INFORMATION

Device	Package	Shipping [†]
NTR4171PT1G	SOT-23 (Pb-Free)	3000/Tape & Reel

DISCONTINUED (Note 1)

NTR4171PT3G	SOT-23 (Pb-Free)	10000/Tape & Reel
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[†] For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, [BRD8011/D](#).

1. **DISCONTINUED:** This device is not recommended for new design. Please contact your onsemi representative for information. The most current information on this device may be available on [www.onsemi.com](#).

NTR4171P

MOSFET ELECTRICAL CHARACTERISTICS ($T_J = 25\text{ }^{\circ}\text{C}$ unless otherwise noted)

Parameter	Symbol	Test Condition	Min	Typ	Max	Units
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OFF CHARACTERISTICS

Drain-to-Source Breakdown Voltage	$V_{(BR)DSS}$	$V_{GS} = 0\text{ V}, I_D = -250\text{ }\mu\text{A}$	-30			V
Drain-to-Source Breakdown Voltage Temperature Coefficient	$V_{(BR)DSS}/T_J$	$I_D = -250\text{ }\mu\text{A}$, Reference to $25\text{ }^{\circ}\text{C}$		24		mV/ $^{\circ}\text{C}$
Zero Gate Voltage Drain Current	I_{DSS}	$V_{GS} = 0\text{ V}, V_{DS} = -24\text{ V}, T_J = 25\text{ }^{\circ}\text{C}$ $V_{GS} = 0\text{ V}, V_{DS} = -24\text{ V}, T_J = 85\text{ }^{\circ}\text{C}$			-1.0 -5.0	μA
Gate-to-Source Leakage Current	I_{GSS}	$V_{DS} = 0\text{ V}, V_{GS} = \pm 12\text{ V}$			± 0.1	μA

ON CHARACTERISTICS (Note 4)

Gate Threshold Voltage	$V_{GS(TH)}$	$V_{GS} = V_{DS}, I_D = -250\text{ }\mu\text{A}$	-0.7	-1.15	-1.4	V
Negative Threshold Temperature Coefficient	$V_{GS(TH)}/T_J$			3.5		mV/ $^{\circ}\text{C}$
Drain-to-Source On-Resistance	$R_{DS(on)}$	$V_{GS} = -10\text{ V}, I_D = -2.2\text{ A}$		50	75	m Ω
		$V_{GS} = -4.5\text{ V}, I_D = -1.8\text{ A}$		60	110	
		$V_{GS} = -2.5\text{ V}, I_D = -1.0\text{ A}$		90	150	
Forward Transconductance	g_{FS}	$V_{DS} = -5.0\text{ V}, I_D = -2.2\text{ A}$		7.0		S

CHARGES, CAPACITANCES AND GATE RESISTANCE

Input Capacitance	C_{iss}	$V_{GS} = 0\text{ V}, f = 1.0\text{ MHz},$ $V_{DS} = -15\text{ V}$		720		pF
Output Capacitance	C_{oss}			95		
Reverse Transfer Capacitance	C_{rss}			65		
Total Gate Charge	$Q_{G(TOT)}$	$V_{GS} = -10\text{ V}, V_{DS} = -15\text{ V},$ $I_D = -3.5\text{ A}$		15.6		nC
Threshold Gate Charge	$Q_{G(TH)}$			0.7		
Gate-to-Source Charge	Q_{GS}			1.6		
Gate-to-Drain Charge	Q_{GD}			2.6		
Total Gate Charge	$Q_{G(TOT)}$	$V_{GS} = -4.5\text{ V}, V_{DS} = -15\text{ V},$ $I_D = -3.5\text{ A}$		7.4		nC
Threshold Gate Charge	$Q_{G(TH)}$			0.7		
Gate-to-Source Charge	Q_{GS}			1.6		
Gate-to-Drain Charge	Q_{GD}			2.6		
Gate Resistance	R_G			6.1		Ω

SWITCHING CHARACTERISTICS, $V_{GS} = 4.5\text{ V}$ (Note 5)

Turn-On Delay Time	$t_{d(on)}$	$V_{GS} = -10\text{ V}, V_{DS} = -15\text{ V},$ $I_D = -3.5\text{ A}, R_G = 6\text{ }\Omega$		8.0		ns
Rise Time	t_r			11		
Turn-Off Delay Time	$t_{d(off)}$			32		
Fall Time	t_f			14		
Turn-On Delay Time	$t_{d(on)}$	$V_{GS} = -4.5\text{ V}, V_{DS} = -15\text{ V},$ $I_D = -3.5\text{ A}, R_G = 6\text{ }\Omega$		9.0		ns
Rise Time	t_r			16		
Turn-Off Delay Time	$t_{d(off)}$			25		
Fall Time	t_f			22		

DRAIN-SOURCE DIODE CHARACTERISTICS

Forward Diode Voltage	V_{SD}	$V_{GS} = 0\text{ V}, I_S = -1.0\text{ A}, T_J = 25\text{ }^{\circ}\text{C}$		-0.8	-1.2	V
Reverse Recovery Time	t_{RR}	$V_{GS} = 0\text{ V}, I_S = -1.0\text{ A},$ $dI_{SD}/dt = 100\text{ A}/\mu\text{s}$		14		ns
Charge Time	t_a			10		
Discharge Time	t_b			4.0		
Reverse Recovery Charge	Q_{RR}			8.0		nC

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

3. Surface-mounted on FR4 board using 1 in sq pad size (Cu area = 1.127 in sq [2 oz] including traces)

4. Pulse Test: Pulse Width $\leq 300\text{ }\mu\text{s}$, Duty Cycle $\leq 2\%$

5. Switching characteristics are independent of operating junction temperatures



TYPICAL CHARACTERISTICS

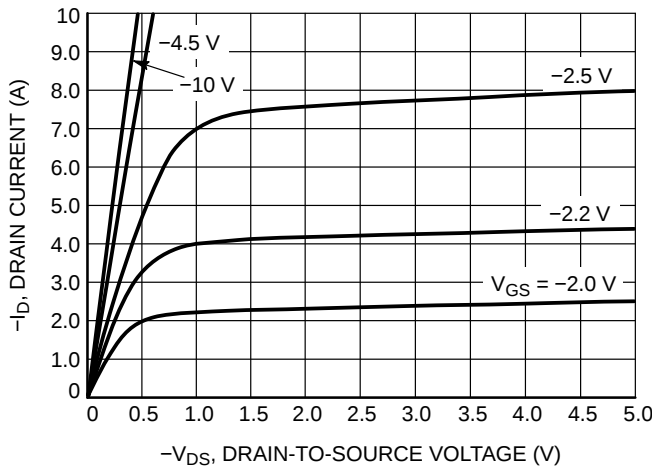


Figure 1. On-Region Characteristics

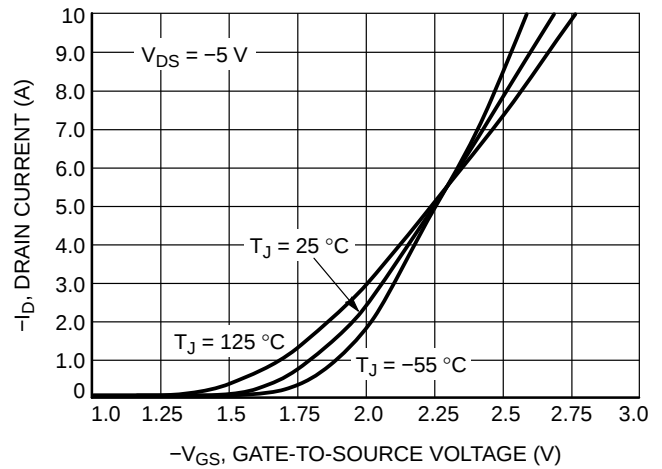


Figure 2. Transfer Characteristics

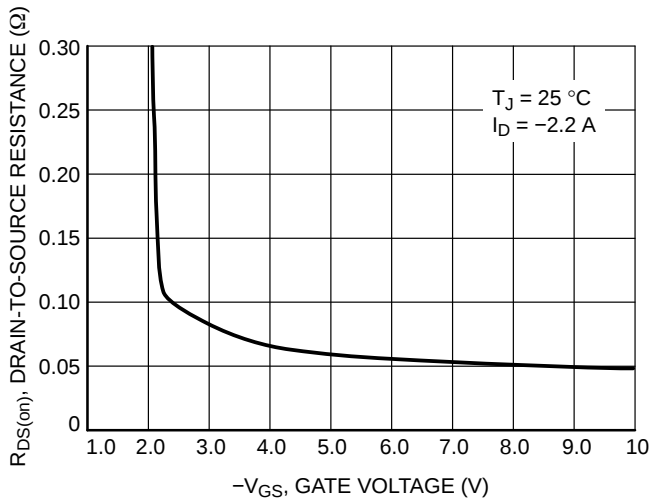


Figure 3. On-Resistance vs. Gate-to-Source Voltage

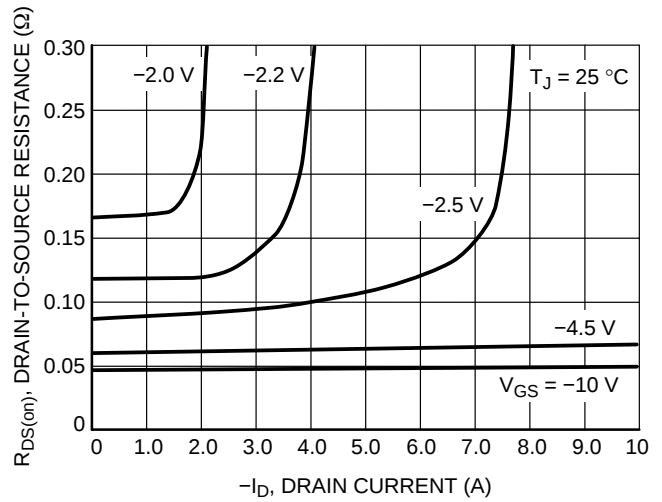


Figure 4. On-Resistance vs. Drain Current and Gate Voltage

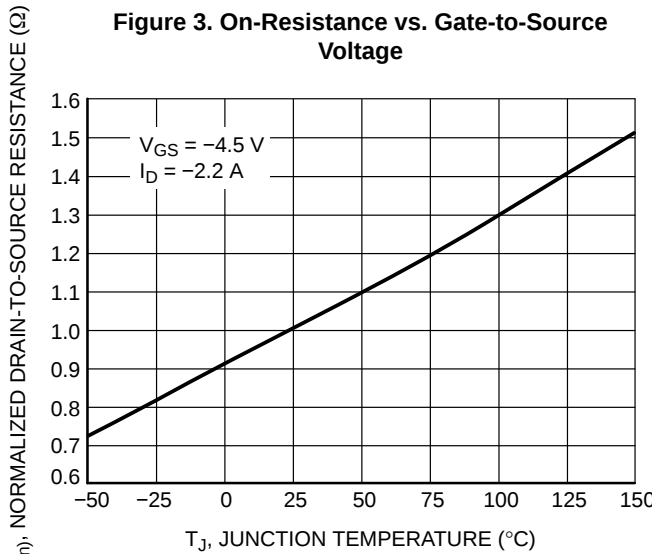


Figure 5. On-Resistance Variation with Temperature

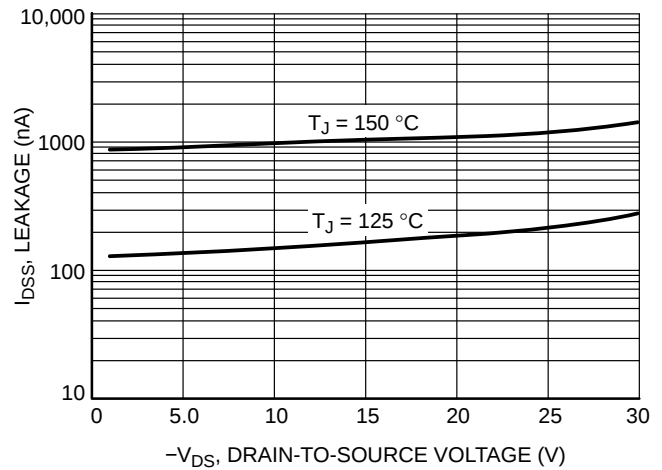
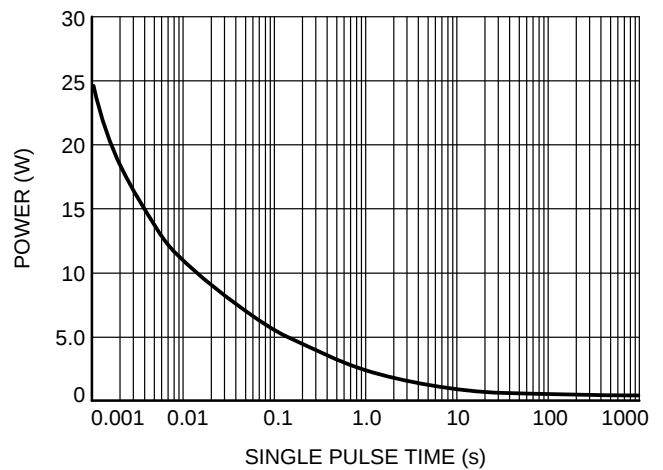
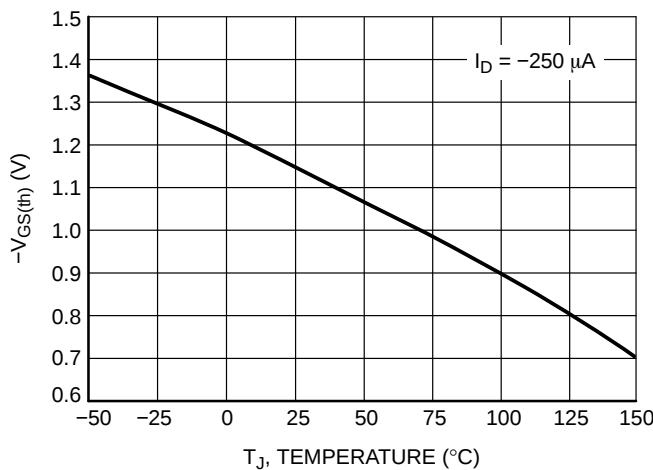
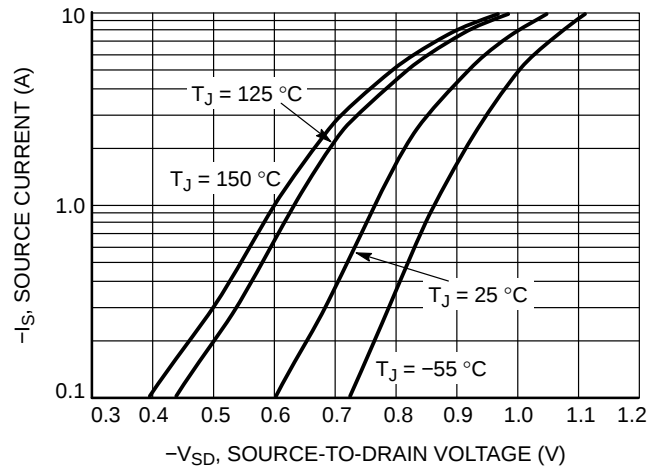
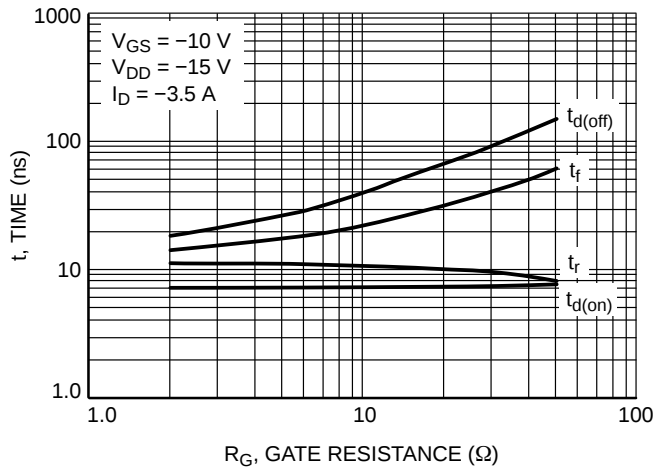
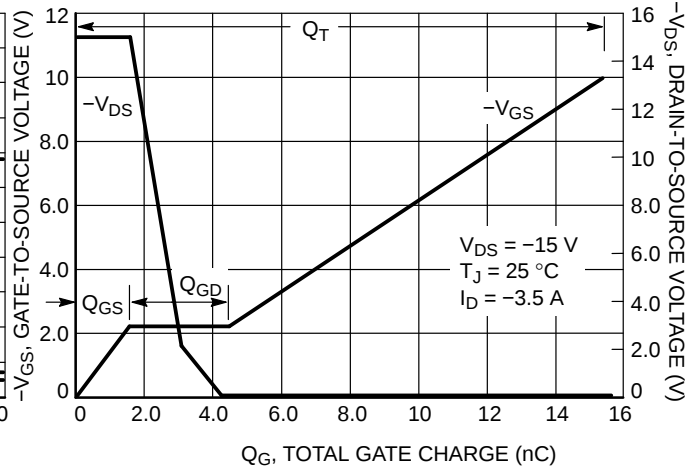
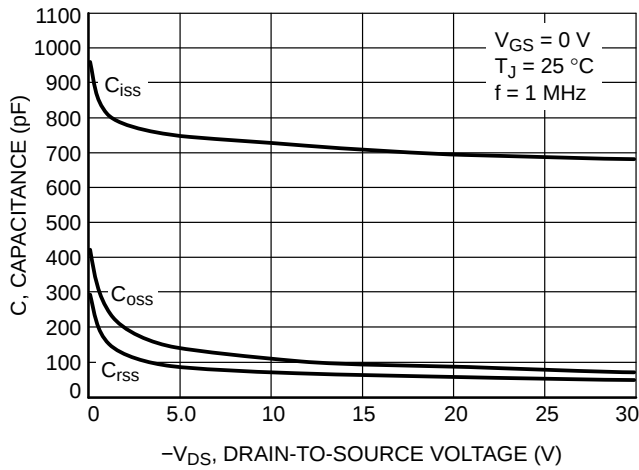


Figure 6. Drain-to-Source Leakage Current vs. Voltage

TYPICAL CHARACTERISTICS



TYPICAL CHARACTERISTICS

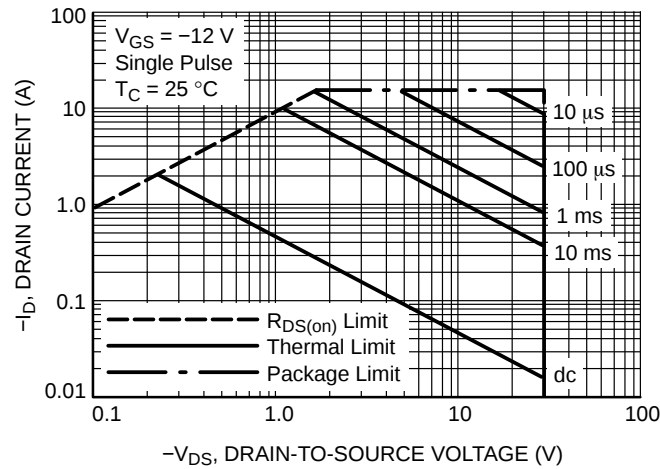


Figure 13. Maximum Rated Forward Biased Safe Operating Area

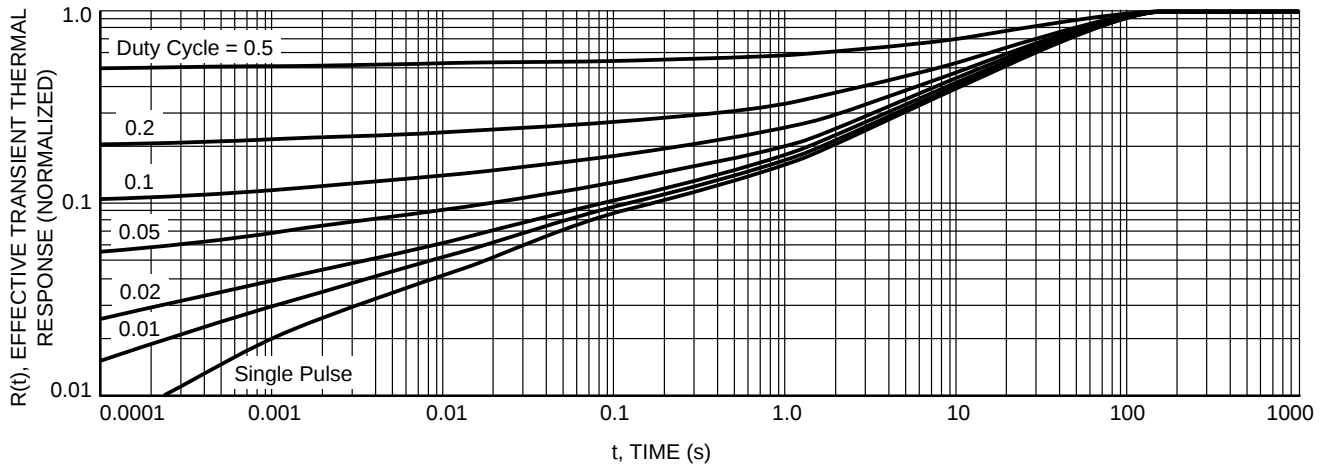


Figure 14. FET Thermal Response

NTR4171P

REVISION HISTORY

Revision	Description of Changes	Date
3	Rebranded the document to onsemi format. NTR4171PT3G OPN marked as Discontinued.	2/4/2026

This document has undergone updates prior to the inclusion of this revision history table. The changes tracked here only reflect updates made on the noted approval dates.

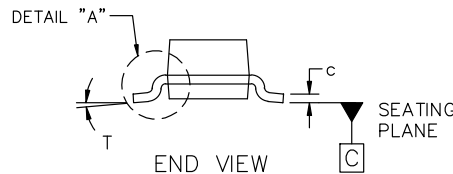
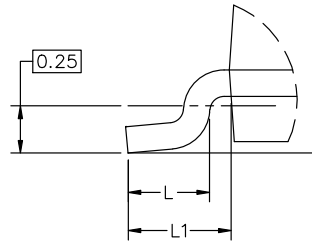




SCALE 4:1

SOT-23 (TO-236) 2.90x1.30x1.00 1.90P
CASE 318
ISSUE AU

DATE 14 AUG 2024



MILLIMETERS			
DIM	MIN	NOM	MAX
A	0.89	1.00	1.11
A1	0.01	0.06	0.10
b	0.37	0.44	0.50
c	0.08	0.14	0.20
D	2.80	2.90	3.04
E	1.20	1.30	1.40
e	1.78	1.90	2.04
L	0.30	0.43	0.55
L1	0.35	0.54	0.69
HE	2.10	2.40	2.64
T	0°	---	10°

NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 2018.
2. CONTROLLING DIMENSIONS: MILLIMETERS.
3. MAXIMUM LEAD THICKNESS INCLUDES LEAD FINISH. MINIMUM LEAD THICKNESS IS THE MINIMUM THICKNESS OF THE BASE MATERIAL.
4. DIMENSIONS D AND E DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS.

GENERIC
MARKING DIAGRAM*



XXX = Specific Device Code
M = Date Code
▪ = Pb-Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "▪", may or may not be present. Some products may not follow the Generic Marking.



RECOMMENDED
MOUNTING FOOTPRINT

* For additional information on our Pb-Free strategy and soldering details, please download the onsemi Soldering and Mounting Techniques Reference Manual, SOLDERM/D.

STYLES ON PAGE 2

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CASE 318
ISSUE AU

DATE 14 AUG 2024

STYLE 1 THRU 5: CANCELLED	STYLE 6: PIN 1. BASE 2. EMITTER 3. COLLECTOR	STYLE 7: PIN 1. EMITTER 2. BASE 3. COLLECTOR	STYLE 8: PIN 1. ANODE 2. NO CONNECTION 3. CATHODE		
STYLE 9: PIN 1. ANODE 2. ANODE 3. CATHODE	STYLE 10: PIN 1. DRAIN 2. SOURCE 3. GATE	STYLE 11: PIN 1. ANODE 2. CATHODE 3. CATHODE-ANODE	STYLE 12: PIN 1. CATHODE 2. CATHODE 3. ANODE	STYLE 13: PIN 1. SOURCE 2. DRAIN 3. GATE	STYLE 14: PIN 1. CATHODE 2. GATE 3. ANODE
STYLE 15: PIN 1. GATE 2. CATHODE 3. ANODE	STYLE 16: PIN 1. ANODE 2. CATHODE 3. CATHODE	STYLE 17: PIN 1. NO CONNECTION 2. ANODE 3. CATHODE	STYLE 18: PIN 1. NO CONNECTION 2. CATHODE 3. ANODE	STYLE 19: PIN 1. CATHODE 2. ANODE 3. CATHODE-ANODE	STYLE 20: PIN 1. CATHODE 2. ANODE 3. GATE
STYLE 21: PIN 1. GATE 2. SOURCE 3. DRAIN	STYLE 22: PIN 1. RETURN 2. OUTPUT 3. INPUT	STYLE 23: PIN 1. ANODE 2. ANODE 3. CATHODE	STYLE 24: PIN 1. GATE 2. DRAIN 3. SOURCE	STYLE 25: PIN 1. ANODE 2. CATHODE 3. GATE	STYLE 26: PIN 1. CATHODE 2. ANODE 3. NO CONNECTION
STYLE 27: PIN 1. CATHODE 2. CATHODE 3. CATHODE	STYLE 28: PIN 1. ANODE 2. ANODE 3. ANODE				

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