

MOSFET – Dual, N-Channel, POWERTRENCH®

30 V, 4.6 A, 31 mΩ

FDC30N20DZ

General Description

This N-Channel MOSFET is produced using onsemi's advanced POWERTRENCH process. This process has been optimized for $r_{DS(on)}$, switching performance and ruggedness.

Features

- Max $r_{DS(on)}$ = 31 mΩ at $V_{GS} = 10$ V, $I_D = 4.6$ A
- Max $r_{DS(on)}$ = 38 mΩ at $V_{GS} = 4.5$ V, $I_D = 4.2$ A
- High Performance Trench Technology for Extremely Low $r_{DS(on)}$
- Fast Switching Speed
- 100% UIL Tested
- Typical CDM ESD Protection Level > 2.0 kV (Note 5)
- This Device is Pb-Free and is RoHS Compliant

Applications

- Load Switch
- Synchronous Rectifier

MOSFET MAXIMUM RATINGS ($T_A = 25^\circ\text{C}$ unless otherwise noted)

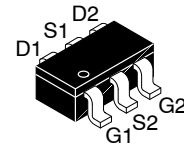
Symbol	Parameter	Ratings	Units
V_{DS}	Drain to Source Voltage	30	V
V_{GS}	Gate to Source Voltage	± 20	V
I_D	Drain Current	Continuous (Note 1a)	4.6 A
		Pulsed (Note 4)	30 A
E_{AS}	Single Pulse Avalanche Energy (Note 3)	3	mJ
P_D	Power Dissipation	(Note 1a)	0.96 W
		(Note 1b)	0.69 W
T_J, T_{STG}	Operating and Storage Junction Temperature Range	-55 to +150	$^\circ\text{C}$

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

THERMAL CHARACTERISTICS

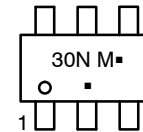
Symbol	Parameter	Ratings	Units
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient (Note 1a)	130	$^\circ\text{C}/\text{W}$
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient (Note 1b)	180	$^\circ\text{C}/\text{W}$

V_{DS}	$r_{DS(on)}$ MAX	I_D MAX
30 V	31 mΩ @ 10 V	4.6 A
	38 mΩ @ 4.5 V	



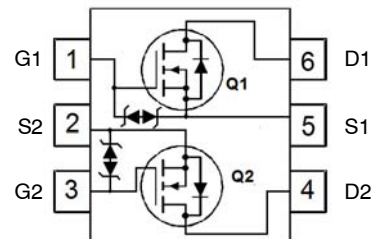
TSOT23 6-Lead
SUPERSOT™-6
CASE 419BL

MARKING DIAGRAM



30N = Specific Device Code
M = Date Code
▪ = Pb-Free Package
(Note: Microdot may be in either location)

PINOUT



ORDERING INFORMATION

See detailed ordering and shipping information on page 5 of this data sheet.

FDC30N20DZ

ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise noted)

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
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OFF CHARACTERISTICS

BV _{DSS}	Drain to Source Breakdown Voltage	I _D = 250 μA, V _{GS} = 0 V	30	–	–	V
$\frac{\Delta BV_{DSS}}{\Delta T_J}$	Breakdown Voltage Temperature Coefficient	I _D = 250 μA, referenced to 25°C	–	22	–	mV/°C
I _{DSS}	Zero Gate Voltage Drain Current	V _{DS} = 24 V, V _{GS} = 0 V	–	–	1	μA
I _{GSS}	Gate to Source Leakage Current	V _{GS} = ±20 V, V _{DS} = 0 V	–	–	±10	μA

ON CHARACTERISTICS

V _{GS(th)}	Gate to Source Threshold Voltage	V _{GS} = V _{DS} , I _D = 250 μA	1	1.7	3	V
$\frac{\Delta V_{GS(th)}}{\Delta T_J}$	Gate to Source Threshold Voltage Temperature Coefficient	I _D = 250 μA, referenced to 25°C	–	–4	–	mV/°C
r _{DS(on)}	Static Drain to Source On Resistance	V _{GS} = 10 V, I _D = 4.6 A	–	23	31	mΩ
		V _{GS} = 4.5 V, I _D = 4.2 A	–	27	38	
		V _{GS} = 10 V, I _D = 4.6 A, T _J = 125°C	–	31	42	
g _{FS}	Forward Transconductance	V _{DS} = 5 V, I _D = 4.6 A	–	23	–	S

DYNAMIC CHARACTERISTICS

C _{iss}	Input Capacitance	V _{DS} = 15 V, V _{GS} = 0 V, f = 1 MHz	–	356	535	pF
C _{oss}	Output Capacitance		–	110	165	pF
C _{rss}	Reverse Transfer Capacitance		–	18	30	pF
R _g	Gate Resistance		0.1	3.5	7.0	Ω

SWITCHING CHARACTERISTICS

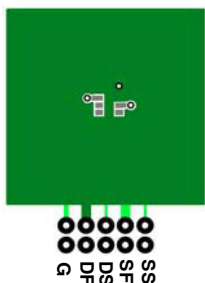
t _{d(on)}	Turn-On Delay Time	V _{DD} = 15 V, I _D = 4.6 A, V _{GS} = 10 V, R _{GEN} = 6 Ω	–	6	12	ns
t _r	Rise Time		–	2	10	ns
t _{d(off)}	Turn-Off Delay Time		–	13	21	ns
t _f	Fall Time		–	2	10	ns
Q _{g(TOT)}	Total Gate Charge	V _{GS} = 0 V to 10 V, V _{DD} = 15 V, I _D = 4.6 A	–	5.6	7.9	nC
		V _{GS} = 0 V to 4.5 V, V _{DD} = 15 V, I _D = 4.6 A	–	2.7	3.8	nC
Q _{gs}	Gate to Source Charge	V _{DD} = 15 V, I _D = 4.6 A	–	0.9	–	nC
Q _{gd}	Gate to Drain "Miller" Charge		–	0.8	–	nC

DRAIN-SOURCE DIODE CHARACTERISTICS

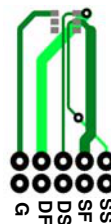
V _{SD}	Source-Drain Diode Forward Voltage	V _{GS} = 0 V, I _S = 4.6 A (Note 2)	–	0.85	1.2	V
t _{rr}	Reverse Recovery Time	I _F = 4.6 A, di/dt = 100 A/μs	–	10	20	ns
Q _{rr}	Reverse Recovery Charge		–	2	10	nC

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

1. R_{θJA} is the sum of the junction-to-case and case-to-ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the drain pins. R_{θJC} is guaranteed by design while R_{θCA} is determined by the user's board design.



a. 130°C/W when mounted on a 1 in² pad of 2 oz. copper



b. 180°C/W when mounted on a minimum pad of 2 oz. copper

2. Pulse Test: Pulse Width < 300 μs, Duty cycle < 2.0 %.
3. E_{AS} of 3 mJ starting T_J = 25°C; N-ch: L = 0.1 mH, I_{AS} = 8 A, V_{DD} = 27 V, V_{GS} = 10 V.
4. Pulse I_d measured at t_d ≤ 250 μs, refer to SOA graph for more details.
5. The diode connected between the gate and source serves only as protection against ESD. No gate overvoltage rating is implied.

TYPICAL CHARACTERISTICS

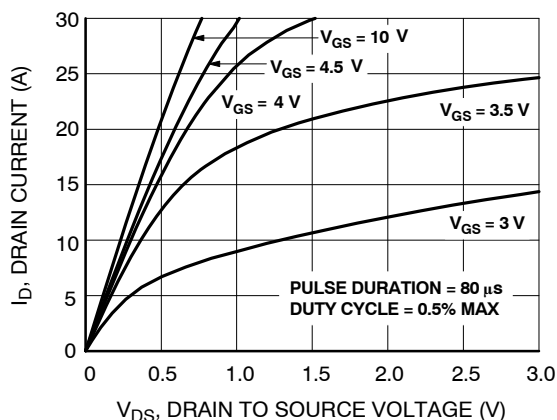
(T_J = 25°C unless otherwise noted)

Figure 1. On-Region Characteristics

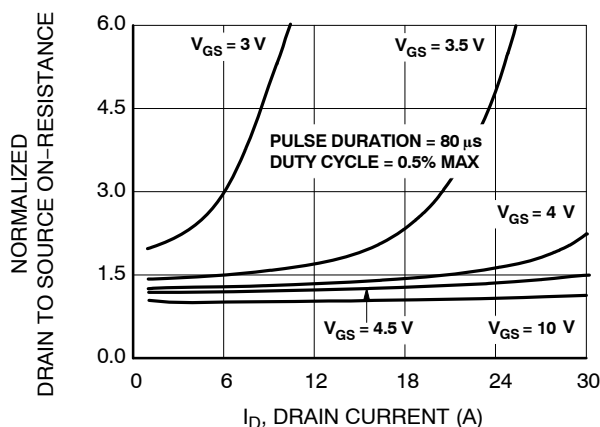


Figure 2. Normalized On-Resistance vs Drain Current and Gate Voltage

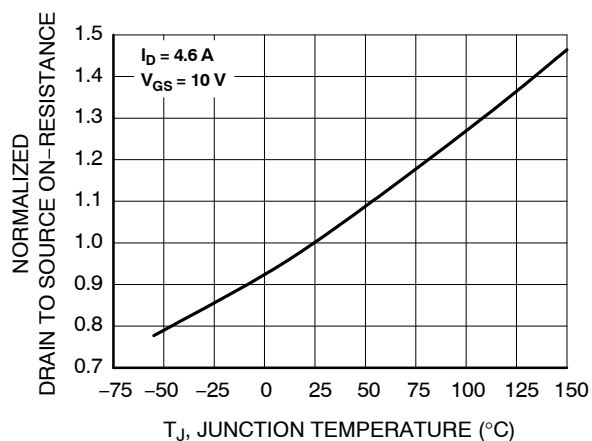


Figure 3. Normalized On-Resistance vs Junction Temperature

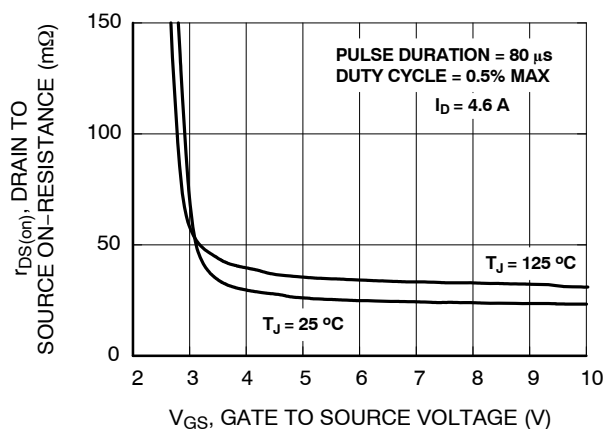


Figure 4. On-Resistance vs Gate to Source Voltage

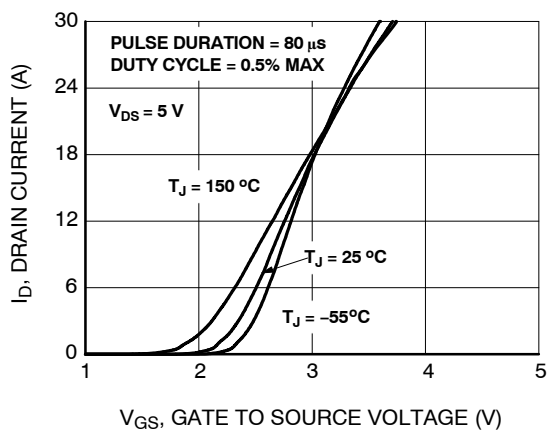


Figure 5. Transfer Characteristics

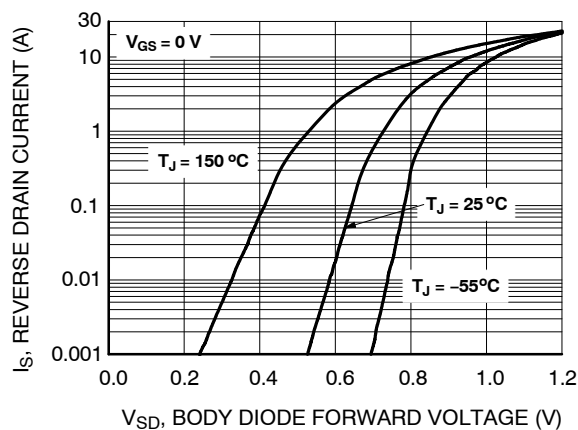


Figure 6. Source to Drain Diode Forward Voltage vs Source Current

FDC30N20DZ

TYPICAL CHARACTERISTICS (continued)

($T_J = 25^\circ\text{C}$ unless otherwise noted)

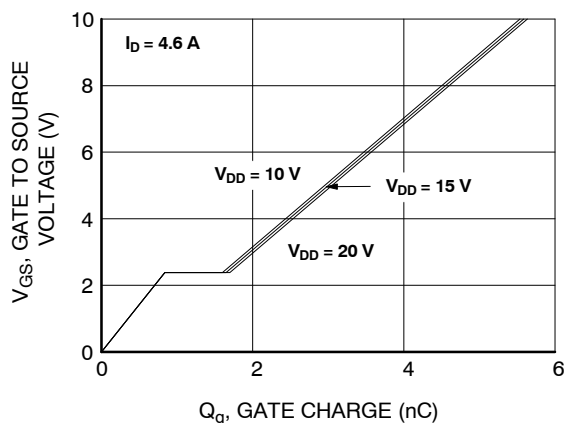


Figure 7. Gate Charge Characteristics

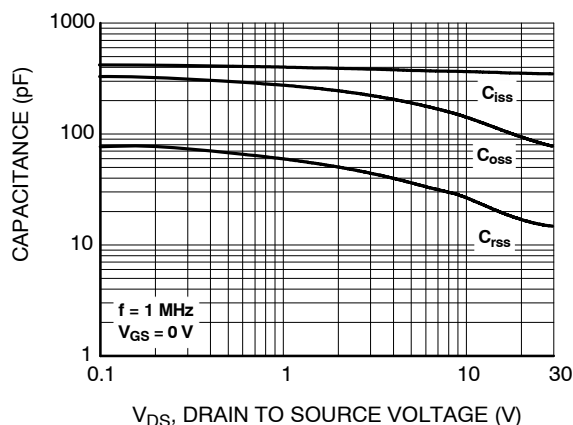


Figure 8. Capacitance vs Drain to Source Voltage

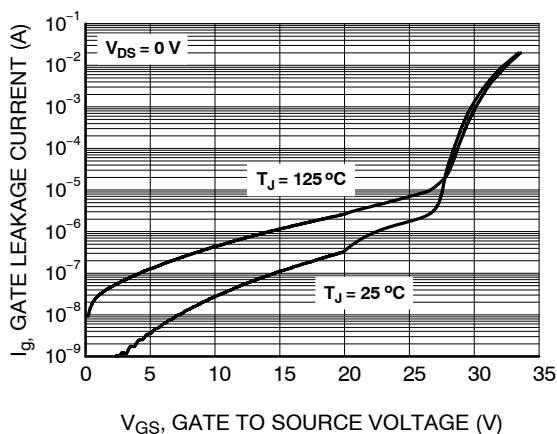


Figure 9. Gate Leakage Current vs. Gate to Source Voltage

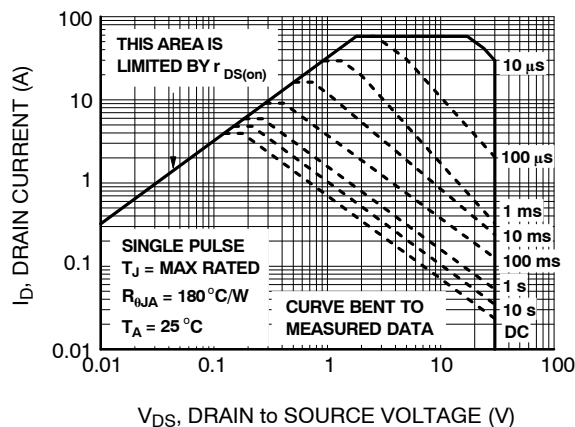


Figure 10. Forward Bias Safe Operating Area

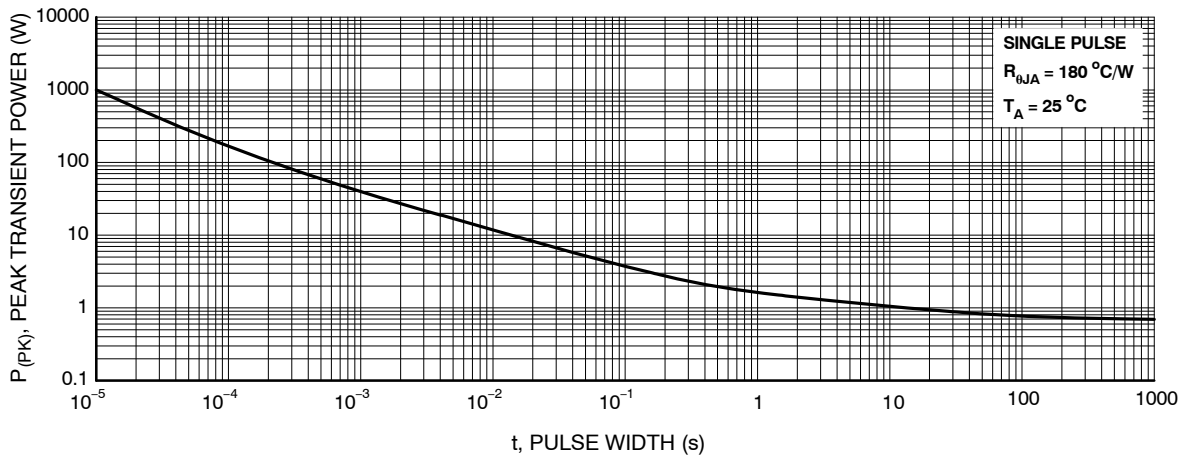


Figure 11. Single Pulse Maximum Power Dissipation

FDC30N20DZ

TYPICAL CHARACTERISTICS (continued)

($T_J = 25^\circ\text{C}$ unless otherwise noted)

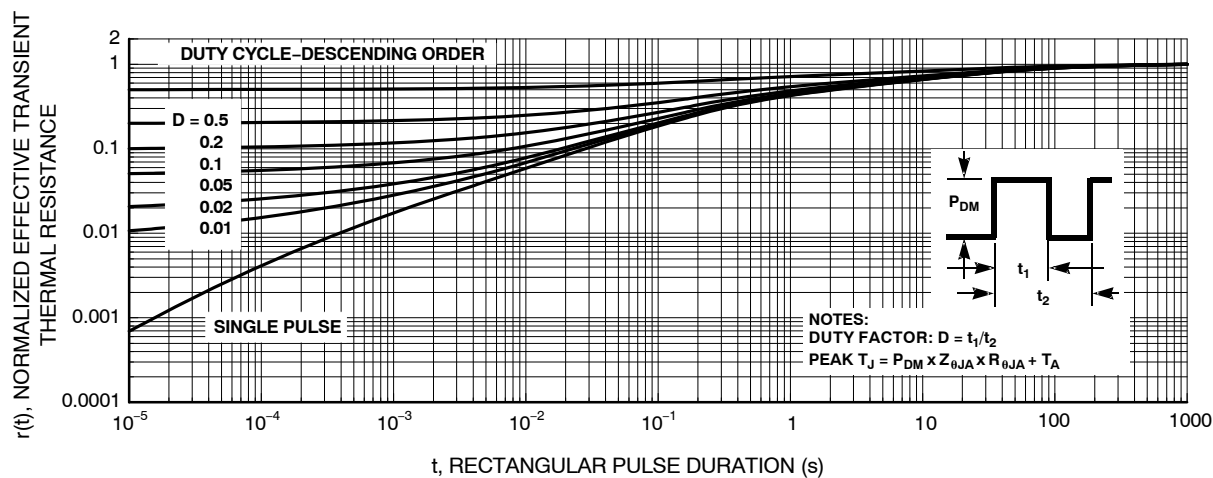


Figure 12. Junction to Ambient Transient Thermal Response Curve

ORDERING INFORMATION

Device	Device Marking	Package Type	Shipping [†]
FDC30N20DZ	30N	TSOT-23-6 (Pb-free)	3000 / Tape & Reel

[†]For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

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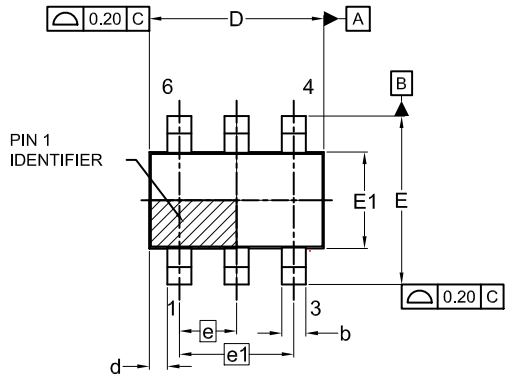
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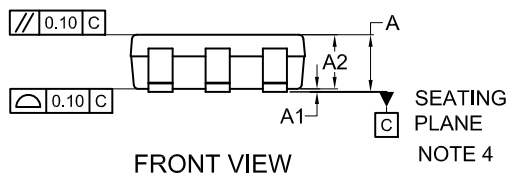
SCALE 2:1

TSOT23 6-Lead
CASE 419BL
ISSUE A

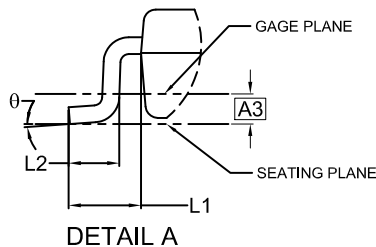
DATE 31 AUG 2020



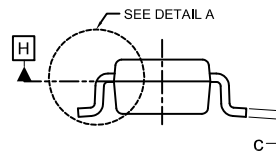
TOP VIEW



FRONT VIEW

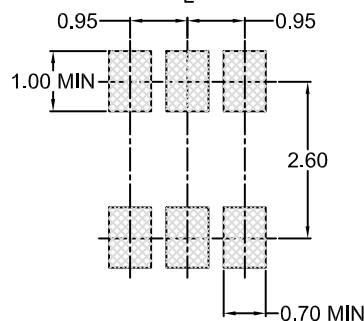


DETAIL A



SIDE VIEW

SYMM

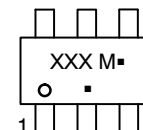

LAND PATTERN
RECOMMENDATION

*FOR ADDITIONAL INFORMATION ON OUR
PB-FREE STRATEGY AND SOLDERING DETAILS,
PLEASE DOWNLOAD THE ON SEMICONDUCTOR
SOLDERING AND MOUNTING TECHNIQUES
REFERENCE MANUAL, SOLDERM/D.

NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 2009.
2. CONTROLLING DIMENSION: MILLIMETERS
3. DIMENSIONS D AND E1 DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS. MOLD FLASH, PROTRUSIONS OR GATE BURRS SHALL NOT EXCEED 0.25MM PER END. DIMENSIONS D AND E1 ARE DETERMINED AT DATUM H.
4. SEATING PLANE IS DEFINED BY THE TERMINALS. "A1" IS DEFINED AS THE DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT ON THE PACKAGE BODY.

DIM	MILLIMETERS		
	MIN.	NOM.	MAX.
A	0.90	1.00	1.10
A1	0.00	0.05	0.10
A2	0.70	0.85	1.00
A3	0.25 BSC		
b	0.25	0.38	0.50
c	0.10	0.18	0.26
D	2.80	2.95	3.10
d	0.30 REF		
E	2.50	2.75	3.00
E1	1.30	1.50	1.70
e	0.95 BSC		
e1	1.90 BSC		
L1	0.60 REF		
L2	0.20	0.40	0.60
Θ	0°	—	10°

GENERIC
MARKING DIAGRAM*


XXX = Specific Device Code

M = Date Code

▪ = Pb-Free Package

(Note: Microdot may be in either location)

*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "▪", may or may not be present. Some products may not follow the Generic Marking.

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DESCRIPTION:	TSOT23 6-Lead	PAGE 1 OF 1

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