

XC8109 Series

ETR33004-006

85mΩ High-performance Power Switch

■ GENERAL DESCRIPTION

The XC8109 series is a P-channel MOSFET power switch IC with a low ON resistance. A current limit, reverse current prevention (prevents reverse current from V_{OUT} to V_{IN}), soft start, thermal shutdown, and an under-voltage lockout (UVLO) are incorporated as protective functions. A flag function monitors the power switch status. The flag output has N-channel open drain structure, and outputs Low level signal while over-current or overheating is detected, or while the reverse current prevention is operated.

A variable current limiting function is integrated, allowing the current limit value to be set, using an external resistor. The voltage level which is fed to CE pin determines the status of XC8109. The logic level of CE pin is selectable between either one of active high or active low.

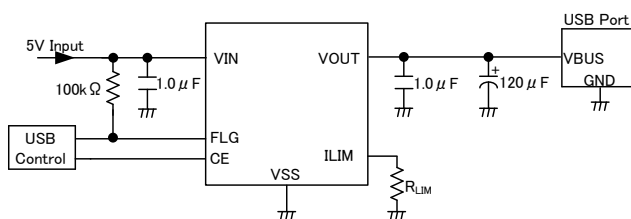
■ APPLICATIONS

- Set Top Boxes
- Digital TVs
- PCs
- USB Ports/USB Hubs
- HDMI

■ FEATURES

Input Voltage	: 2.5V ~ 5.5V
Maximum Output Current	: 0.9A
ON Resistance	: 85mΩ@ $V_{IN}=5.0V$
Supply Current	: 40 μA @ $V_{IN}=5.0V$
Stand-by Current	: 0.01 μA
Flag Delay Time	: 7.5ms
	* At over-current detection
	: 4ms
	* At reverse voltage detection
Protection Circuit	: Reverse Current Prevention
	75mA ~ 1.3A
	Thermal Shutdown
	Under Voltage Lockout (UVLO)
Functions	: Flag Output
	CE Pin Input Logic Selectable
	C_L Discharge
	Soft-start
Current Limit Response Time	: 2 μs *Reference value
Operating Ambient Temperature	: -40°C ~ 105°C
Package	: USP-6C
Environmentally Friendly	: EU RoHS Compliant, Pb Free

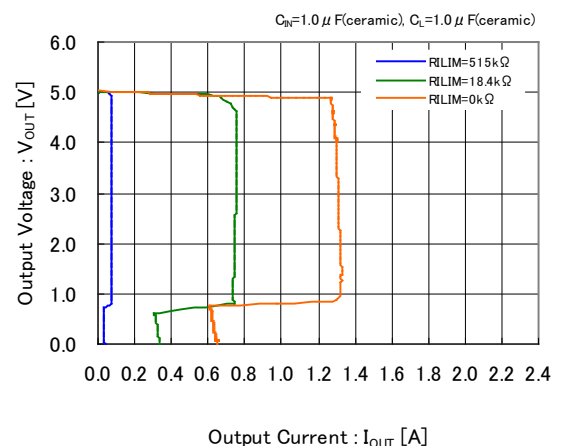
■ TYPICAL APPLICATION CIRCUIT



* The Typical circuit is based on USB high side switch.
The XC8109 series can accommodate 1 μF output capacitor (C_L).

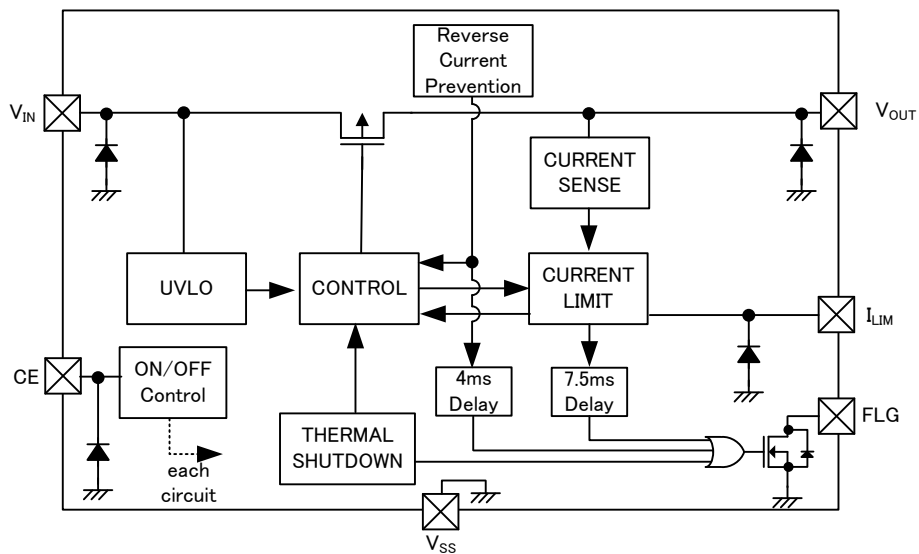
■ TYPICAL PERFORMANCE CHARACTERISTICS

XC8109XC10ER

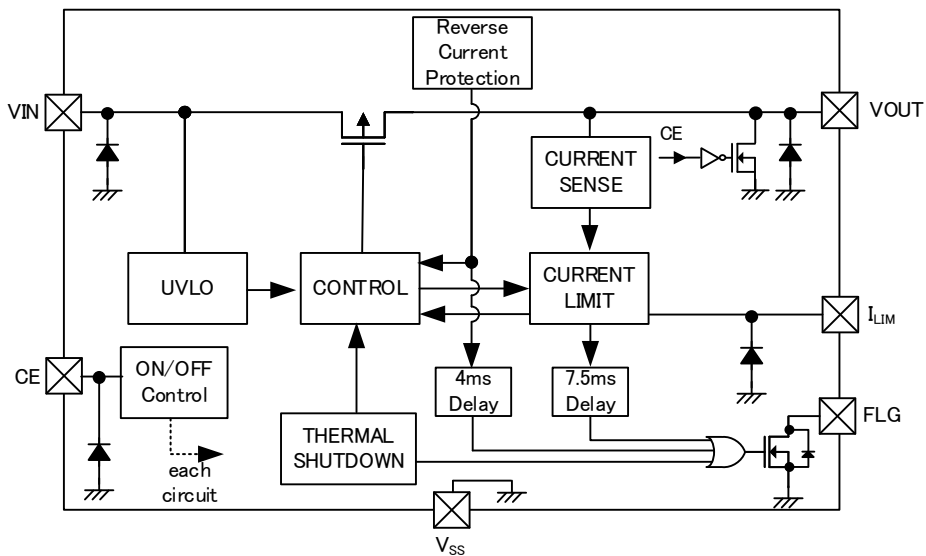


■ BLOCK DIAGRAM

XC8109xC / XC8109xD



XC8109xE / XC8109xF



* Diodes inside the circuit are an ESD protection diode and a parasitic diode.

■PRODUCT CLASSIFICATION

●Ordering Information

XC8109①②③④⑤⑥-⑦

DESIGNATOR	ITEM	SYMBOL	DESCRIPTION
①	CE Logic	A	Refer to Selection Guide
		B	
②	Protection Circuits Type	C	
		D	
		E	
		F	
③④	Maximum Output Current	10	0.9A * Adjustable current limit range:75mA~1300mA
⑤⑥-⑦ (*1)	Package (Order Unit)	ER-G	USP-6C (3,000pcs/Reel)

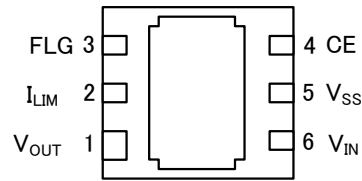
(*1) The "-G" suffix denotes Halogen and Antimony free as well as being fully EU RoHS compliant.

●Selection Guide

TYPE ①②	Current Limit / Reverse Current Prevention	CE Logic	C _L Discharge
AC (*2)	Automatic Recovery	Active High	-
AE (*2)			Yes
BC		Active Low	-
BE			Yes
AD (*2)	Latch Protection	Active High	-
AF (*2)			Yes
BD		Active Low	-
BF			Yes

(*2) AC/AD/AE/AF is the standard type.

PIN CONFIGURATION



USP-6C
(BOTTOM VIEW)

* The dissipation pad for the USP-6C packages should be solder-plated for mounting strength and heat dissipation.
Please refer to the reference mount pattern and metal masking. The dissipation pad should be connected to the V_{SS} (No. 5) pin.

PIN ASSIGNMENT

PIN NUMBER	PIN NAME	FUNCTIONS
USP-6C		
1	V _{OUT}	Output
2	I _{LIM}	Current Limit Adjustment
3	FLG	Fault Report
4	CE	ON/OFF Control
5	V _{SS}	Ground
6	V _{IN}	Power Input

FUNCTION

PIN NAME	SIGNAL	STATUS	Applied voltage to V _{IN}	Applied voltage to V _{OUT}	Pch Driver FET	Reverse Protection
CE	XC8109A:H XC8109B:L	Active	2.5V ~ 5.5V	-	ON	-
			(V _{OUT} - V _{REV}) ~ V _{OUT}	2.5V ~ 5.5V	ON	Backflow from V _{IN} to V _{OUT}
			0V ~ (V _{OUT} - V _{REV})	2.5V ~ 5.5V	OFF	Yes
			0V ~ 2.5V	-	Undefined	Undefined
			-	0V ~ 5.5V		
	XC8109A:L XC8109B:H	Stand-by	2.5V ~ 5.5V	-	OFF	-
			0V ~ V _{OUT}	2.5V ~ 5.5V	OFF	Yes
			0V ~ 2.5V	-	Undefined	Undefined
			-	0V ~ 5.5V		
	OPEN	Undefined	-	-	Undefined	Undefined

■ ABSOLUTE MAXIMUM RATINGS

PARAMETER		SYMBOL	RATINGS	UNITS
Input Voltage		V _{IN}	-0.3 ~ 6.0	V
Output Voltage		V _{OUT}	-0.3 ~ 6.0	V
Output Current		I _{OUT}	1.7	A
CE Input Voltage		V _{CE}	-0.3 ~ 6.0	V
FLG Pin Voltage		V _{FLG}	-0.3 ~ 6.0	V
FLG Pin Current		I _{FLG}	15	mA
I _{LIM} Pin Voltage		V _{ILIM}	-0.3 ~ 6.0	V
I _{LIM} Pin Current		I _{ILIM}	±1	mA
Power Dissipation (Ta=25°C)	USP-6C	Pd	120 (IC only)	mW
			1000 (40mm x 40mm Standard board) ^{(*)2}	
			1250 (JESD51-7 board) ^{(*)2}	
Operating Ambient Temperature		Topr	-40 ~ 105	°C
Storage Temperature		Tstg	-55 ~ 125	°C

* All voltages are described based on the V_{SS} .

(*)1 Use with I_{OUT} less than $P_d/(V_{IN}-V_{OUT})$.

(*)2 The power dissipation figure shown is PCB mounted and is for reference only.
Please refer to PACKAGING INFORMATION for the mounting condition.

ELECTRICAL CHARACTERISTICS

Ta=25°C

PARAMETER	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNITS	CIRCUIT
Input Voltage	V _{IN}	-	2.5	-	5.5	V	①
On Resistance	R _{ON}	V _{IN} =3.3V, I _{OUT} =0.5A	-	100	110	mΩ	①
		V _{IN} =5.0V, I _{OUT} =0.5A	-	85	104	mΩ	
Supply Current	I _{SS}	V _{OUT} =OPEN	-	40	75	μA	②
Stand-by Current	I _{STBY}	V _{IN} =5.5V, V _{OUT} =OPEN V _{CE} =V _{SS} (XC8109A) V _{CE} =V _{IN} (XC8109B)	-	0.01	1.0	μA	②
Switch Leakage Current	I _{LEAK}	V _{IN} =5.5V, V _{OUT} =0V V _{CE} =V _{SS} (XC8109A) V _{CE} =V _{IN} (XC8109B)	-	0.01	1.0	μA	②
Current Limit	I _{LIMIT}	V _{OUT} =V _{IN} -0.3V I _{LIM} shorted to V _{SS}	1.170	1.300	1.430	A	①
		V _{OUT} =V _{IN} -0.3V R _{LIM} =18.4kΩ	0.621	0.730	0.840		
Short-Circuit Current	I _{SHORT}	V _{OUT} =0V I _{LIM} shorted to V _{SS}	-	0.650	-	A	①
		V _{OUT} =0V R _{LIM} =18.4kΩ	-	0.365	-		
Current Limit Circuit Response Time ^(*)	t _{CLR}	V _{IN} =5.0V, V _{OUT} : OPEN→0V Measure from V _{OUT} =0V to when current falls below a certain I _{LIMIT} value	-	2.0	-	μs	①
CE "H" Level Voltage	V _{CEH}	V _{IN} =5.5V, XC8109A	1.5	-	5.5	V	①
		V _{IN} =5.5V, XC8109B	V _{SS}	-	0.8		
CE "L" Level Voltage	V _{CEL}	V _{IN} =5.5V, XC8109A	V _{SS}	-	0.8	V	①
		V _{IN} =5.5V, XC8109B	1.5	-	5.5		
CE "H" Level Current	I _{CEH}	V _{IN} =5.5V, V _{CE} =5.5V	-0.1	-	0.1	μA	①
CE "L" Level Current	I _{CEL}	V _{IN} =5.5V, V _{CE} =0V	-0.1	-	0.1	μA	①
UVLO Detected Voltage	V _{UVLOD}	V _{IN} : 2.2V→1.7V	1.8	1.9	2.0	V	①
UVLO Released Voltage	V _{UVLOR}	V _{IN} : 1.7V→2.2V	1.9	2.0	2.1	V	①
UVLO Hysteresis	V _{UHYS}	-	-	0.1	-	V	①

NOTE:

Unless otherwise stated, V_{IN}=5.0V, I_{OUT}=1mA, I_{LIM}=V_{SS}, V_{CE}=V_{IN} (XC8109A) or V_{CE}=V_{SS} (XC8109B)

^(*) Design reference value. This parameter is provided only for reference.

■ ELECTRICAL CHARACTERISTICS (Continued)

Ta=25°C

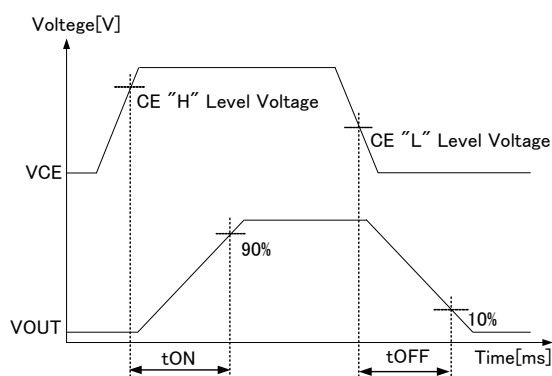
PARAMETER	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNITS	CIRCUIT
turn-on time	t _{ON}	R _{LOAD} =10Ω, V _{CE} =0V→2.2V	-	0.60	1.00	ms	①
turn-off time	t _{OFF}	R _{LOAD} =10Ω, V _{CE} =2.2V→0V	-	0.08	0.13	ms	①
FLG output FET On-resistance	R _{FLG}	I _{FLG} =10mA, V _{OUT} =5.5V	-	15	20	Ω	③
FLG output FET Leakage Current	I _{FOFF}	V _{IN} =5.5V, V _{FLG} =5.5V, V _{OUT} =OPEN	-	0.01	0.1	μA	③
FLG delay time	t _{FD1}	over-current condition	6.5	7.5	8.5	ms	①
	t _{FD2}	reverse-voltage condition	2.7	4.0	4.7	ms	①
Reverse Current	I _{REV}	V _{IN} =0V, V _{OUT} =5.5V V _{CE} =5.0V (XC8109A) V _{CE} =V _{SS} (XC8109B)	-	0.1	1.0	μA	①
Reverse Current Prevention Detect Voltage	V _{REV_D}	V _{IN} : 5.0V→4.7V V _{OUT} =5.0V	-	140	-	mV	①
Thermal Shutdown Detect Temperature	T _{TSD}	Junction Temperature	-	150	-	°C	①
Thermal Shutdown Release Temperature	T _{TSR}	Junction Temperature	-	130	-	°C	①
Thermal Shutdown Hysteresis Width	T _{HYS}	Junction Temperature	-	20	-	°C	①
C _L Discharge Resistance (XC8109xE, XC8109xF)	R _{DCHG}	V _{IN} =2.5V, V _{OUT} =2.5V V _{CE} =V _{SS} (XC8109A) V _{CE} =V _{IN} (XC8109B)	-	150	210	Ω	①

NOTE:

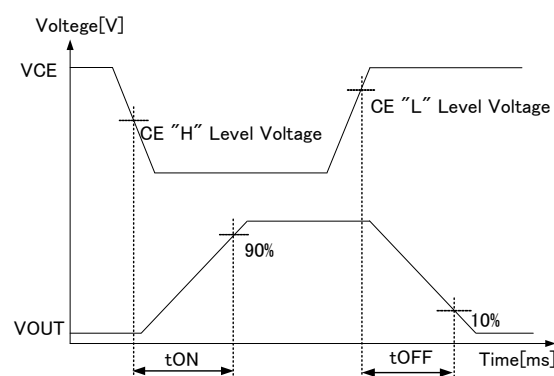
Unless otherwise stated, V_{IN}=5.0V, I_{OUT}=1mA, I_{LIM}=V_{SS}, V_{CE}=V_{IN} (XC8109A) or V_{CE}=V_{SS} (XC8109B)

■ TIMING CHART

● turn-on time, turn-off time



XC8109A

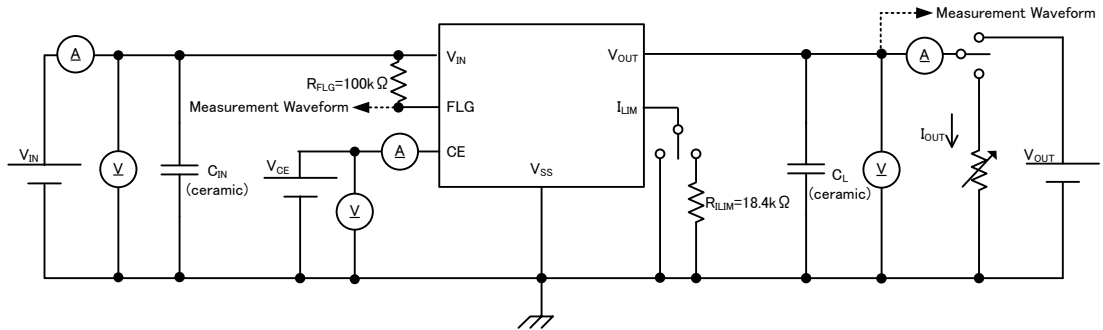


XC8109B

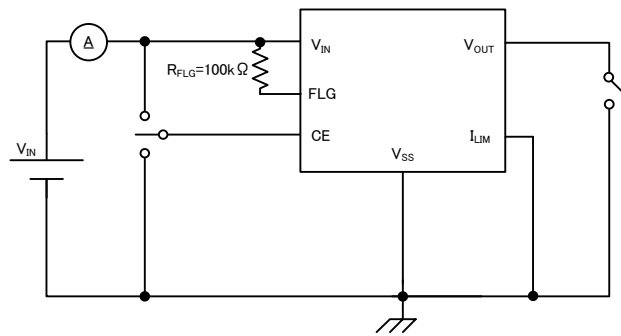
TEST CIRCUITS

$C_{IN}=1.0\ \mu\text{F}$, $C_L=1.0\ \mu\text{F}$

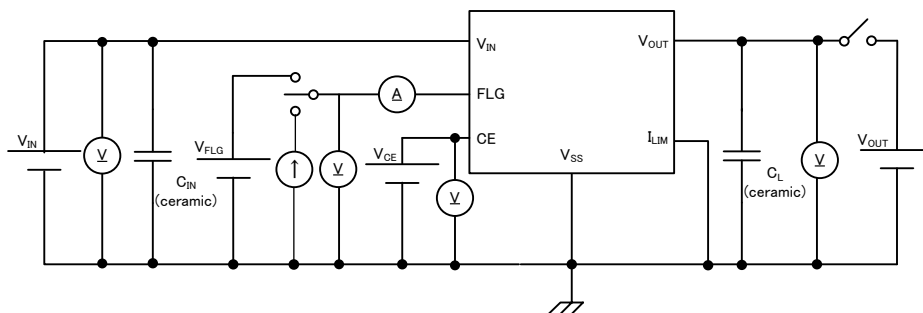
CIRCUIT①



CIRCUIT②



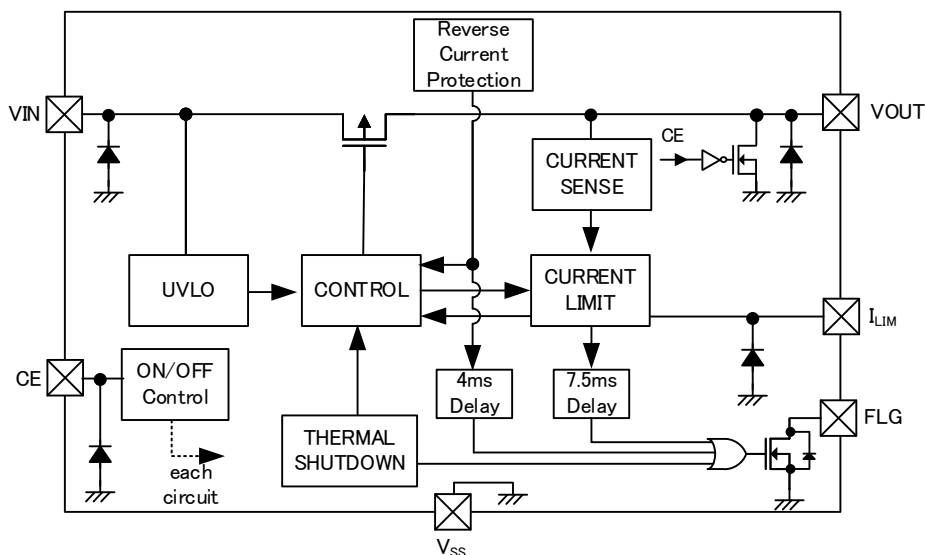
CIRCUIT③



■ OPERATIONAL EXPLANATION

The XC8109 series is a P-channel MOSFET power switch IC.

The XC8109 series consists of a CE circuit, UVLO circuit, thermal shutdown circuit, current limiter circuit, reverse current prevention circuit, control block and others. The gate voltage of the power switch transistor is controlled with control block. The current limiter circuit and reverse current prevention circuit will operate based on the output voltage and output current.



BLOCK DIAGRAM (XC8109xE, XC8109xF)

<CE Pin>

The voltage level which is fed to CE pin controls the status of this IC. If either "H" level or "L" level which is defined as the electrical specification is fed to CE pin, then XC8109 can operate in standard manner. However, if the middle voltage which is neither "H" level nor "L" level is fed to CE pin, the consumption current will increase due to the shoot-through current at internal circuits. Also if CE pin is open, the status of XC8109 cannot be fixed and the behavior will be unstable.

<Thermal Shutdown>

For protection against heat damage of the ICs, thermal shutdown function is built in. When the internal junction temperature reaches the temperature limit, the thermal shutdown circuit operates and the power switch transistor will turn OFF. The IC resumes its operation when the thermal shutdown function is released and the IC's operation is automatically restored because the junction temperature drops to the level of the thermal shutdown release temperature. When the thermal shutdown circuit detects higher junction temperature than the detect temperature, the voltage level of FLG pin is low level. When the thermal shutdown circuit detects lower junction temperature than the release temperature, the thermal shutdown function is released and the voltage level of FLG pin is high level.

<Under Voltage Lockout (UVLO) >

When the V_{IN} pin voltage goes down to lower voltage than UVLO detected voltage, the power switch transistor turns OFF by UVLO function in order to prevent false output caused by unstable operation of the internal circuitry. When the V_{IN} pin voltage goes up to higher voltage than UVLO released voltage, the UVLO function is released and the power switch transistor can turn ON.

<Soft-start Function>

The soft-start circuit can reduce the in-rush current charged on the output capacitor when IC starts up. Additionally, due to the reduction of the in-rush current, the circuit can reduce the fluctuation of the input voltage as well. The soft-start time is optimized internally and defined as turn-on time. (TYP: 0.6ms)

■ OPERATIONAL EXPLANATION (Continued)

<Current limiter, short-circuit protection>

When the output current reaches the current limit value, the current limit function is activated.

When the current limiting function operates, the constant current limiting circuit operates to reduce the output voltage while maintaining the output current.

The short-circuit protection function operates when the output voltage drops below 0.7V (TYP.).

The behavior after the current limit or short circuit protection function is activated differs depending on the product type. The operation of each type is as follows.

Automatic Recovery type: XC8109xC, XC8109xE

After the short-circuit protection function operates, the output current is reduced to the short-circuit current.

The FLG pin outputs a Low-level signal after 7.5ms (TYP.) has passed since the short-circuit protection function was activated.

If the overcurrent state continues, the above-mentioned state will continue to be maintained.

When the overcurrent state is released, the output voltage rises, and if it continues to be 0.7V (TYP.) or higher for 7.5ms (TYP.), the FLG pin returns to the High-level output.

Latch off type: XC8109xD, XC8109xF

After the short-circuit protection function is activated, the output current is reduced to the short-circuit current.

After 7.5ms (TYP.) elapses after the short-circuit protection function is activated, the FLG pin outputs a Low level and turns off the switch transistor.

The off-state is maintained regardless of whether the overcurrent state is resolved.

Latch operation is released by turning off the IC with the CE pin signal and then restarting, or by lowering the input voltage below the UVLO detected voltage once and after that raising it higher than UVLO released voltage.

■ OPERATIONAL EXPLANATION (Continued)

<Current limit external adjustment function>

By connecting a resistor to the current limit external adjustment pin (I_{LIM} pin), the current limit can be set to any value.

By the following equations, the current limit value can be set to any value within a range of 75mA to 1300mA. When the I_{LIM} pin is open, the switch transistor is forcibly turned off.

(In the case of $I_{LIMIT(T)} \geq 500\text{mA}$.)

$$\text{equation 1. } R_{ILIM}(\text{k}\Omega) = 32164 / I_{LIMIT(T)}(\text{mA}) - 25.71(\text{k}\Omega)$$

(In the case of $I_{LIMIT(T)} < 500\text{mA}$.)

$$\text{equation 2. } R_{ILIM}(\text{k}\Omega) = 130170 / I_{LIMIT(T)}(\text{mA})^{1.2814}(\text{k}\Omega)$$

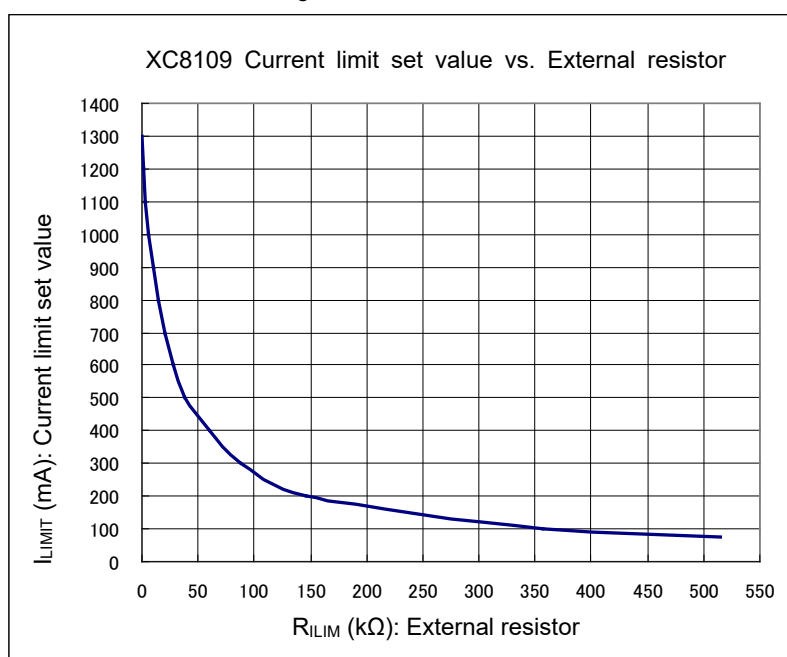
R_{ILIM} : External resistance value $I_{LIMIT(T)}$: Current limit set value

Table1. Current limit set value

$I_{LIMIT(T)}$ (mA)	R_{ILIM} (k Ω)	E96 External resistance value (k Ω)	Current limit value when use E96 external resistance (mA) ^(*)		
			MIN.	TYP.	MAX.
75	515	511	49	75	102
100	356	357	69	100	131
200	147	147	156	200	243
300	87.2	86.6	241	302	362
400	60.3	60.4	314	399	485
500	38.6	38.3	427	503	578
600	27.9	28.0	509	599	689
700	20.2	20.0	598	704	809
800	14.5	14.7	716	796	876
900	10.0	10.0	811	901	991
1000	6.46	6.49	899	999	1099
1100	3.53	3.57	989	1099	1208
1200	1.09	1.10	1080	1200	1320
1300	I_{LIM} shorted to V_{SS}		1170	1300	1430

^(*) MIN. value and MAX. value are reference values.

Fig1. Current limit set value



■ OPERATIONAL EXPLANATION (Continued)

<Current limit external adjustment function> (Continued)

The TYP value of dropout Voltage which is the voltage difference between V_{IN} and V_{OUT} is defined by the equation 3 using output current (I_{OUT}).

$$\text{equation 3. } V_{dif}(mV) = I_{OUT}(mA) \times 0.085(\Omega)$$

The maximum value of dropout voltage has the influence of the setting of a current limit circuit. (Refer to Table 2)

【Example】 In the case of $I_{LIMIT(T)}=500mA$, When output current is 200mA, dropout voltage MAX. value is 22mV.

Table2. Dropout voltage MAX. value (*)

unit: (mV)

Output Current: I_{OUT}	Dropout voltage MAX. value						
	Current limit set value: $I_{LIMIT(T)}$						
	75mA	100mA	200mA	300mA	400mA	500mA	600mA
10mA	4	3	1	1	1	1	1
30mA	15	10	5	4	3	3	3
50mA	41	24	9	6	5	5	5
70mA	-	49	14	10	8	7	7
100mA	-	-	28	15	12	10	10
150mA	-	-	71	29	20	15	15
200mA	-	-	-	55	33	22	20
250mA	-	-	-	112	58	32	26
300mA	-	-	-	-	100	46	35
400mA	-	-	-	-	-	105	67
500mA	-	-	-	-	-	-	143

unit: (mV)

Output Current: I_{OUT}	Dropout voltage MAX. value						
	Current limit set value: $I_{LIMIT(T)}$						
	700mA	800mA	900mA	1000mA	1100mA	1200mA	1300mA
10mA	1	1	1	1	1	1	1
30mA	3	3	3	3	3	3	3
50mA	5	5	5	5	5	5	5
70mA	7	7	7	7	7	7	7
100mA	10	10	10	10	10	10	10
150mA	15	15	15	15	15	15	15
200mA	20	20	20	20	20	20	20
250mA	26	26	26	26	26	26	26
300mA	30	30	30	30	30	30	30
400mA	48	41	41	41	41	41	41
500mA	85	60	51	51	51	51	51
600mA	167	100	75	61	61	61	61
700mA	-	183	122	85	71	71	71
800mA	-	-	214	132	97	82	81
900mA	-	-	-	223	144	107	92

(*) MAX. value is reference value.

■ OPERATIONAL EXPLANATION (Continued)

<Reverse current prevention>

An internal circuit is built in that prevents reverse current from the V_{OUT} pin to the V_{IN} pin.

When the difference between input voltage and V_{OUT} pin voltage is higher than the detect voltage set internally, the reverse current prevention circuit activates, and the power switch transistor turns off, then the reverse current from the V_{OUT} pin to the V_{IN} pin is reduced to $0.1 \mu A$ (TYP.).

If the reverse-voltage state lasts for 4ms (TYP.), the FLG pin changes to Low level output.

The behavior after the reverse current prevention function is activated differs depending on the product type. The operation of each type is as follows.

Automatic Recovery type: XC8109xC, XC8109xE

On the auto recovery type, when the output voltage drops below the input voltage, the reverse current prevention circuit stops immediately, and the power switch transistor turns on again. If the output voltage remains lower than the input voltage for 4ms (TYP.), the FLG pin returns to High level output.

Latch off type: XC8109xD, XC8109xF

On the latch off type, the power switch transistor remains in the off state even if the reverse voltage state is released.

Latch operation is released by turning off the IC with the CE pin signal and then restarting, or by lowering the input voltage below the UVLO detected voltage once and after that raising it higher than UVLO released voltage.

<Flag function>

The flag circuit is built in which monitors the state of the power switch.

The FLG pin outputs Low level when the reverse current prevention function is operating. A resistance of $10k\Omega$ to $100k\Omega$ is recommended for the FLG pin pull-up resistance.

The pull-up voltage should be 5.5V or less.

Automatic Recovery type: XC8109xC, XC8109xE

CONDITION	FLG pin Low level output Condition	FLG pin High level output Condition
Short Protection	7.5ms(TYP.) after maintaining short protection release state	7.5ms(TYP.) after short protection release
Reverse current prevention	4.0ms(TYP.) after maintaining reverse voltage detection state	4.0ms(TYP.) after reverse voltage release
Thermal shutdown	Same time as overheat state is detected	Same time as overheat state is released
Current limiter	Always High level output	
UVLO		
Stand-by		

Latch off type: XC8109xD, XC8109xF

CONDITION	FLG pin Low level output Condition	FLG pin High level output Condition
Short Protection	7.5ms(TYP.) after maintaining short protection release state	When latch operation is released
Reverse current prevention	4.0ms(TYP.) after maintaining reverse voltage release state	When latch operation is released
Thermal shutdown	Same time as overheat state is detected	Same time as overheat state is released
Current limiter	Always High level output	
UVLO		
Stand-by		

■ OPERATIONAL EXPLANATION (Continued)

<C_L discharge function>

The XC8109xE and XC8109xF series feature a C_L discharge function to prevent application malfunction caused by residual charge on the output capacitor during standby (XC8109A: CE="L", XC8109B: CE="H").

This function discharges the output capacitor by activating an N-channel FET between the V_{OUT} and V_{SS} pins. The discharge resistance is R_{DCHG}=150Ω(TYP.).

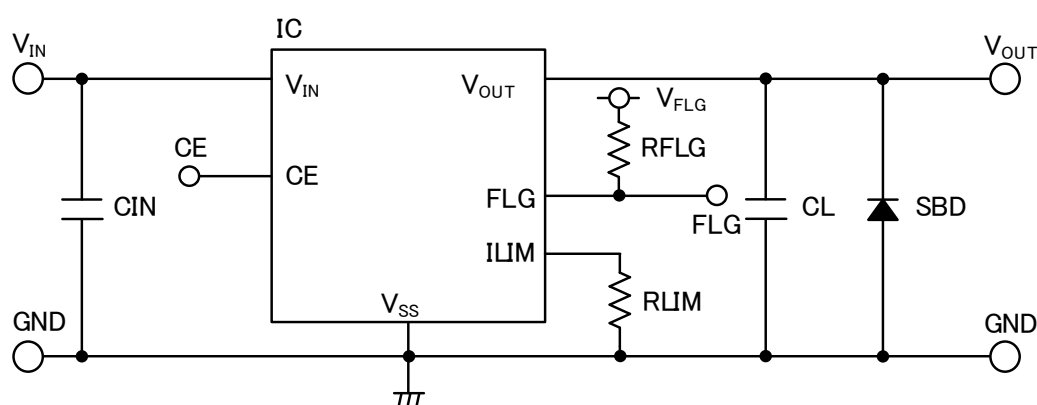
Additionally, the C_L discharge function remains active for a duration of t_{OFF}=0.08ms (TYP.) until the P-channel FET switch between V_{IN} and V_{OUT} is completely turned off. During this period, the input current increases by the amount of the discharge current, as power supply from the input via the P-channel FET and discharge via the N-channel FET occur simultaneously.

■NOTES ON USE

1. For the phenomenon of temporal and transitional voltage decrease or voltage increase, the IC may be damaged or deteriorated if IC is used beyond the absolute MAX. specifications.
2. Where wiring impedance is high, operations may become unstable due to noise depending on output current.
Please keep the resistance low between V_{IN} and V_{SS} wiring in particular.
3. Please place the input capacitor (C_{IN}) and the output capacitor (C_L) as close to the IC as possible.
For the input or output capacitor, a capacitance of $1.0\ \mu\text{F}$ or higher is recommended.
4. The IC can be broken if the V_{OUT} pin voltage suddenly undershoots to a negative voltage due to an output short circuit between the V_{OUT} pin and GND, or if the V_{IN} pin voltage overshoots after the current limiting operation and exceeds the rated voltage.

We recommend the following counter measures so that the rated voltage is not exceeded.

- (a) To suppress the amount of the undershoot by increasing the output capacitance and slowing down the rate of decreasing V_{OUT} at the time of short circuit.
- (b) To add a SBD between V_{OUT} pin and GND to suppress the undershoot of V_{OUT} pin voltage.
- (c) To increase the input capacitor to suppress the overshoot of the V_{IN} pin voltage after the current limiter is activated.

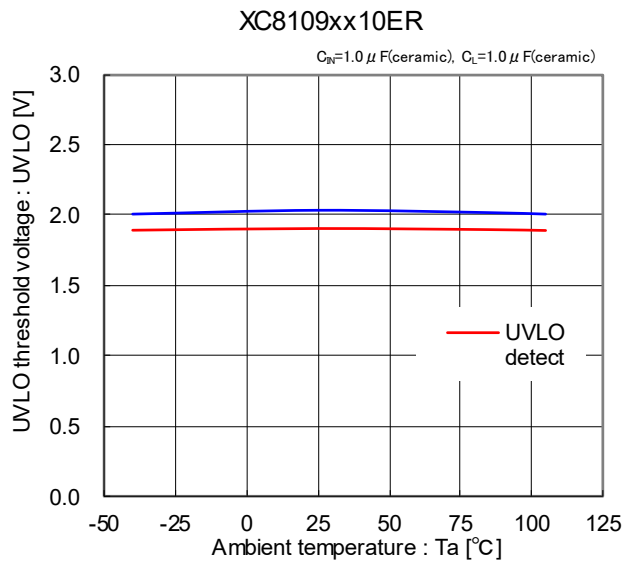


Recommended countermeasure circuit diagram

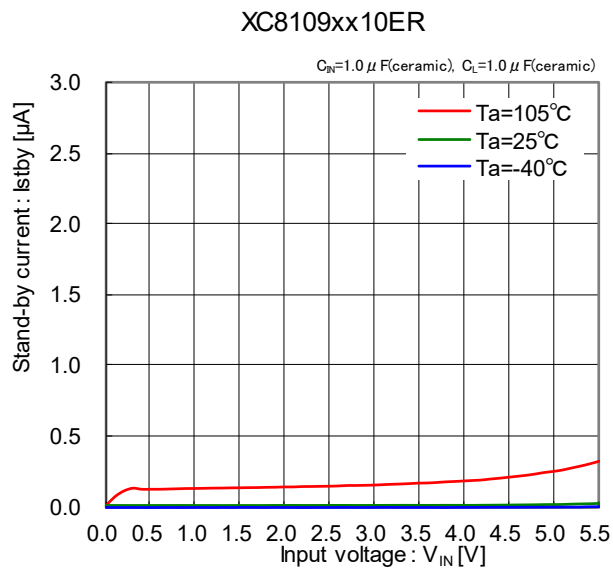
5. The current limit value can be adjusted by external resistor (R_{LIM}). The characteristics of the resistor influence the current limit value. Therefore, please choose the resistor with small tolerance and temperature coefficient.
6. It is recommended to use the output current at 80% or less of the current limit set value ($I_{LIMIT(T)}$).
7. Torex places an importance on improving our products and its reliability.
However, by any possibility, we would request user fail-safe design and post-aging treatment on system or equipment.

TYPICAL PERFORMANCE CHARACTERISTICS

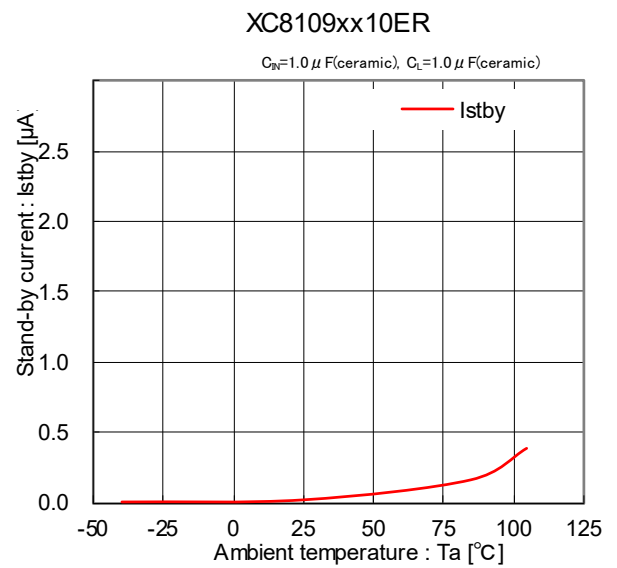
(1) UVLO threshold voltage vs. Ambient temperature



(2) Stand-by current vs. Input voltage

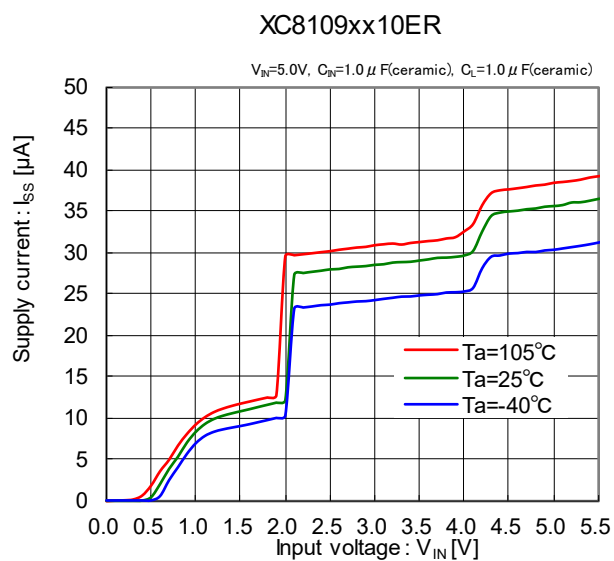


(3) Stand-by current vs. Ambient temperature

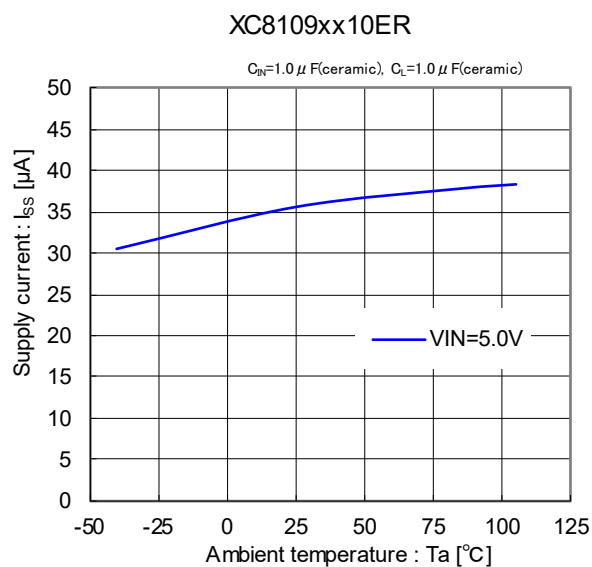


■ TYPICAL PERFORMANCE CHARACTERISTICS (Continued)

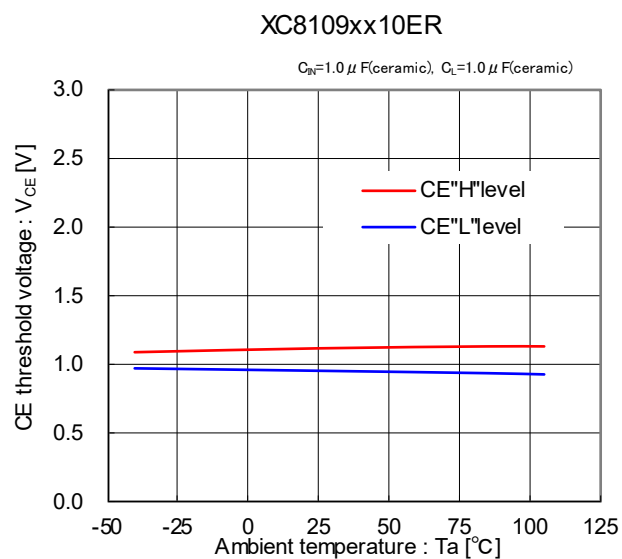
(4) Supply current vs. Input voltage(sweep up)



(5) Supply current vs. Ambient temperature

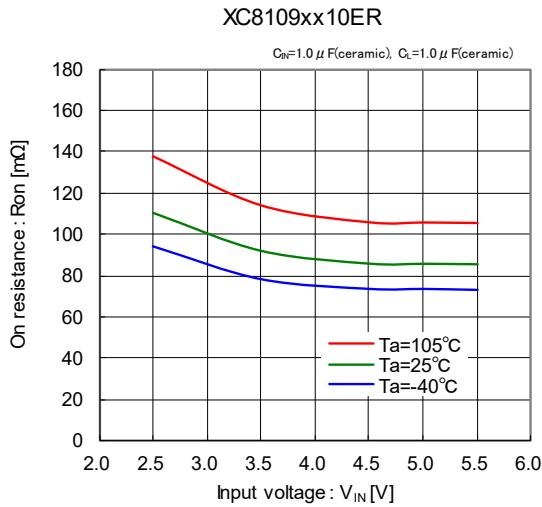


(6) CE threshold voltage vs. Ambient temperature

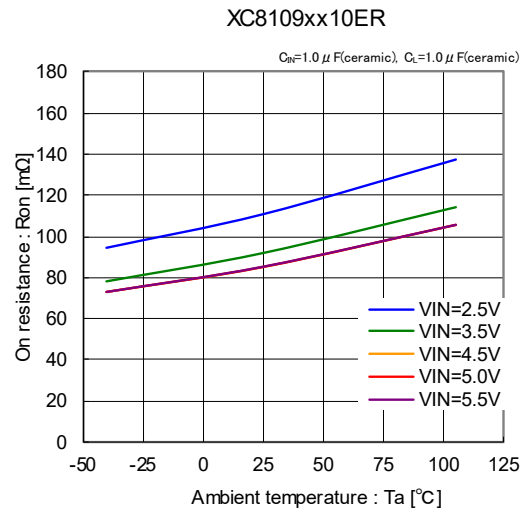


TYPICAL PERFORMANCE CHARACTERISTICS (Continued)

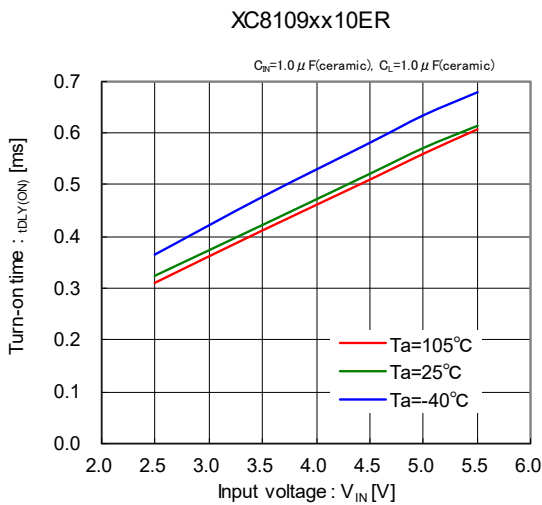
(7) On resistance vs. Input voltage



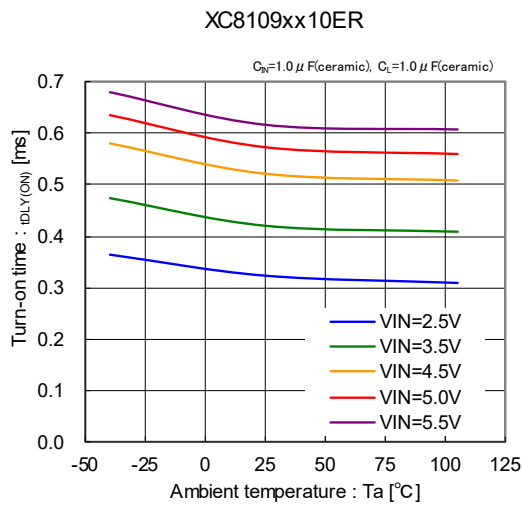
(8) On resistance vs. Ambient temperature



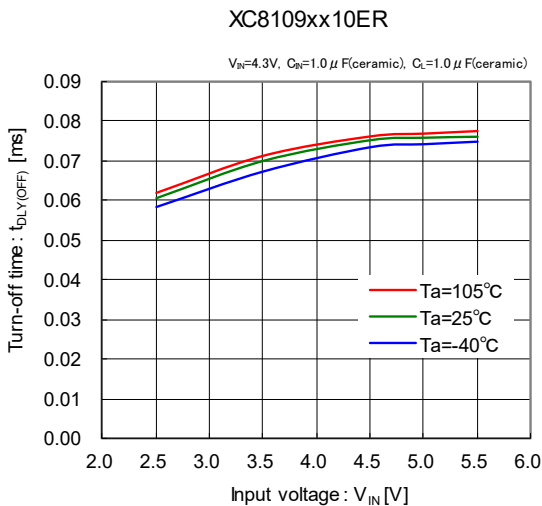
(9) Turn-on time vs. Input voltage



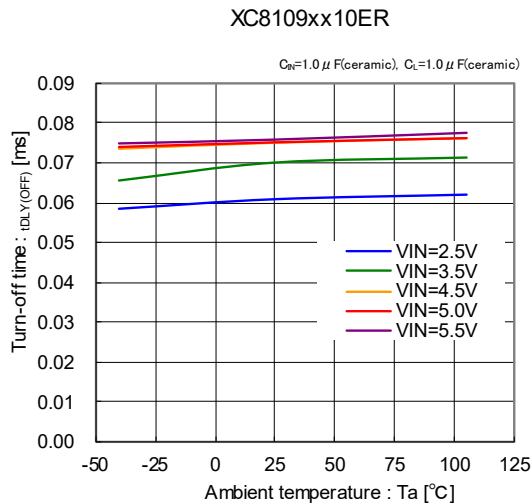
(10) Turn-on time vs. Ambient temperature



(11) Turn-off time vs. Input voltage

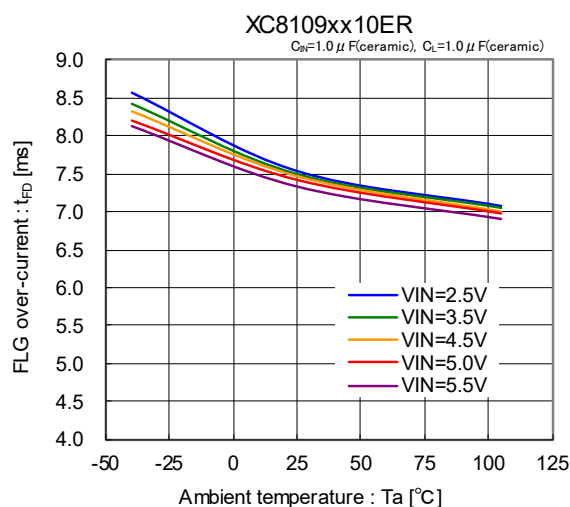


(12) Turn-off time vs. Ambient temperature

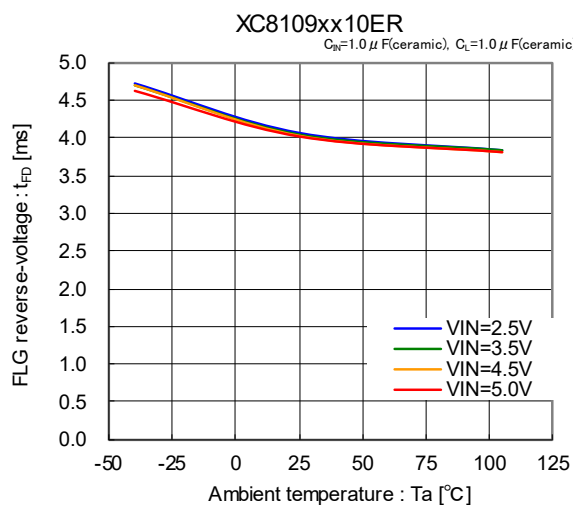


■ TYPICAL PERFORMANCE CHARACTERISTICS (Continued)

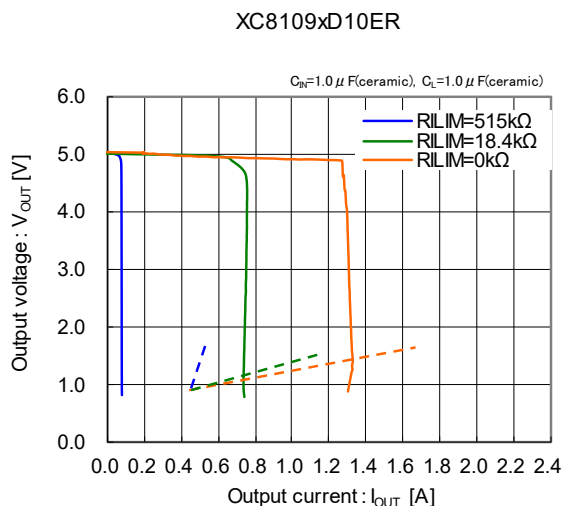
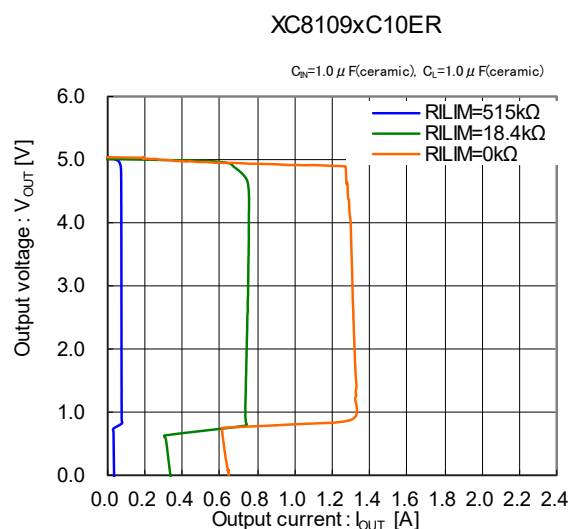
(13) FLG delay time over-current
vs. Ambient temperature



(14) FLG delay time reverse-voltage
vs. Ambient temperature

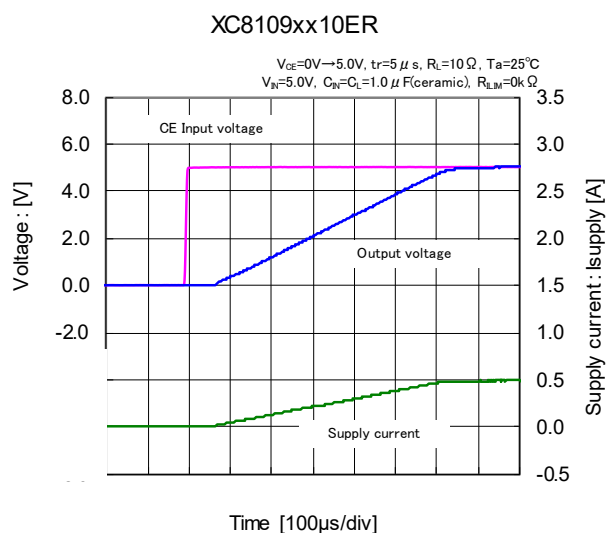


(15) Output voltage vs. Output current

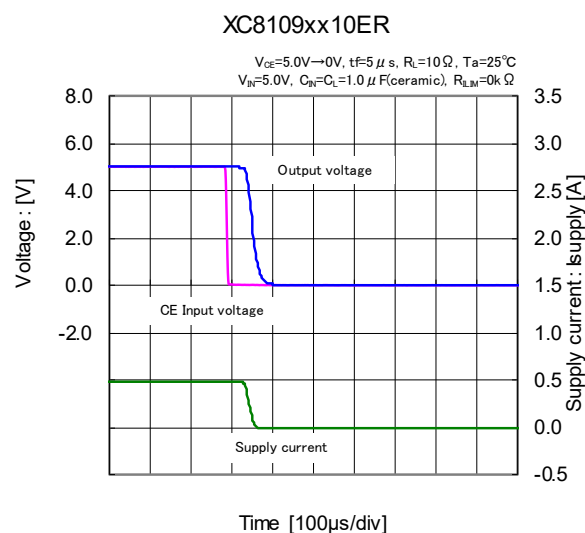


In over-current states, after output voltage drops and the lapse of 7.5ms, the latch off type turns off the power switch transistor.

(16) Turn-on delay vs. Rise time ($C_L=1.0\mu F$)

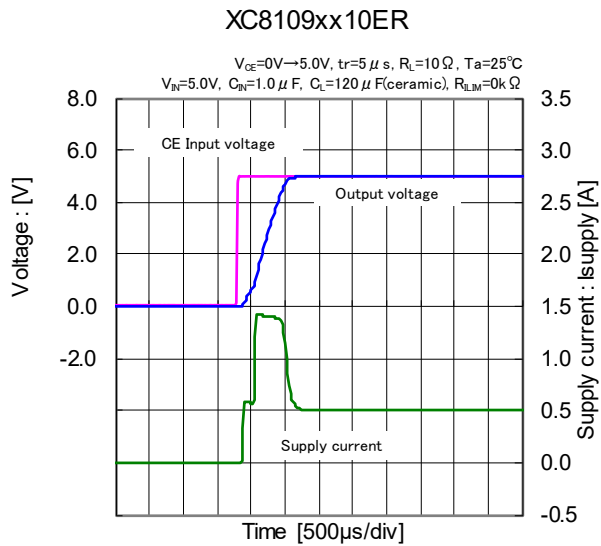


(17) Turn-off delay vs. Fall time ($C_L=1.0\mu F$)

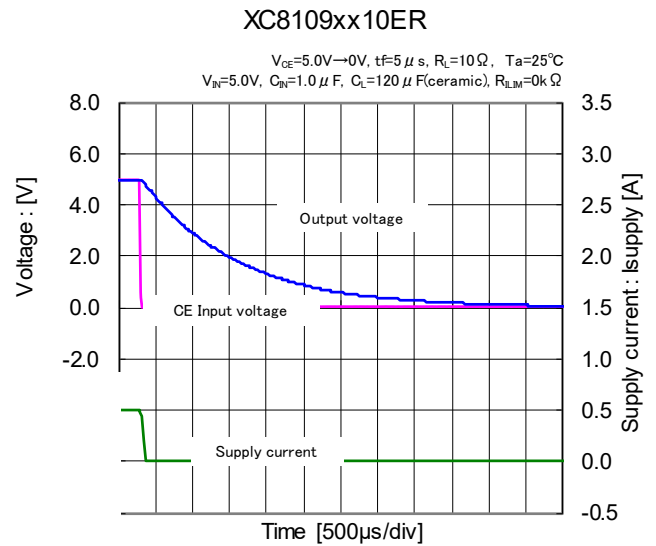


TYPICAL PERFORMANCE CHARACTERISTICS (Continued)

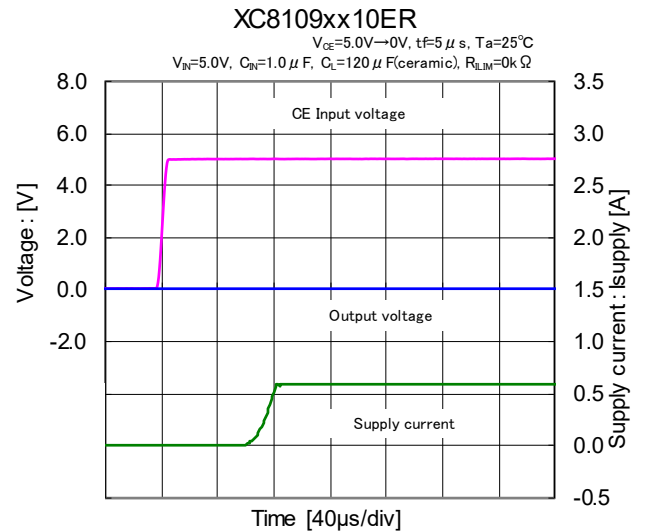
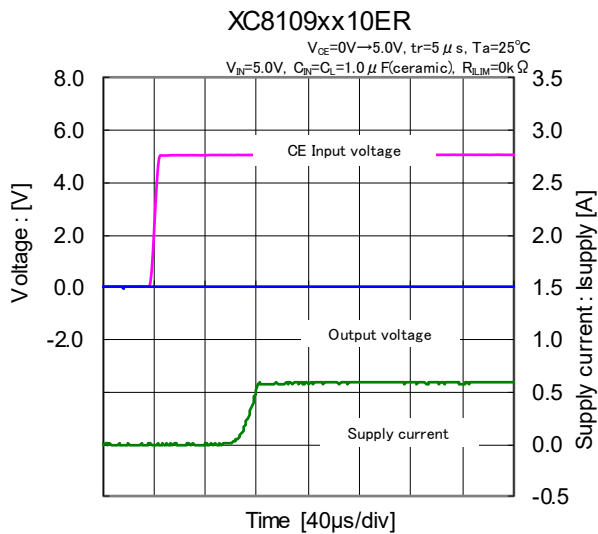
(18) Turn-on delay vs. Rise time (CL=120μF)



(19) Turn-off delay vs. Fall time (CL=120μF)

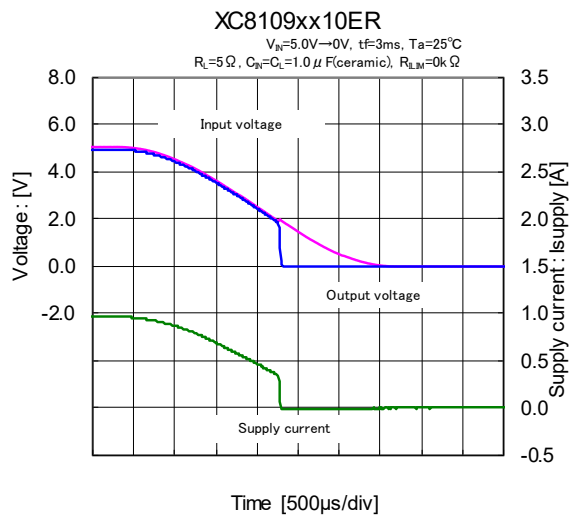
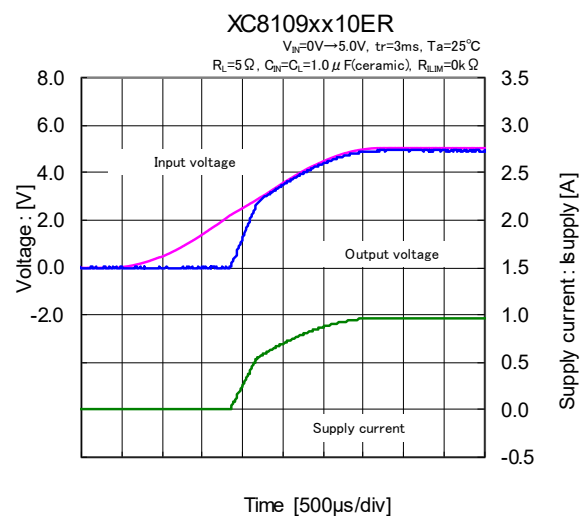


(20) Short circuit current, Device enabled into short

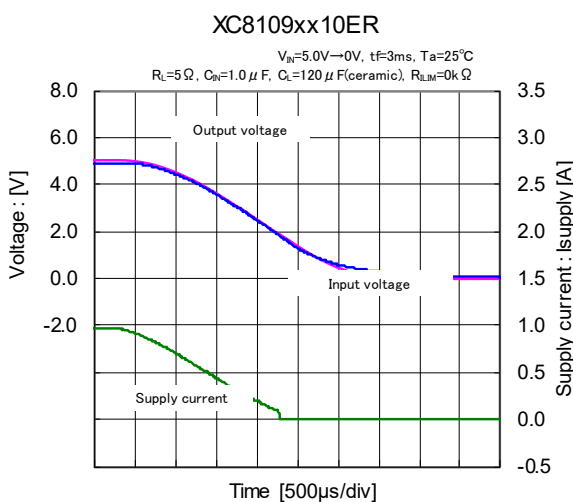
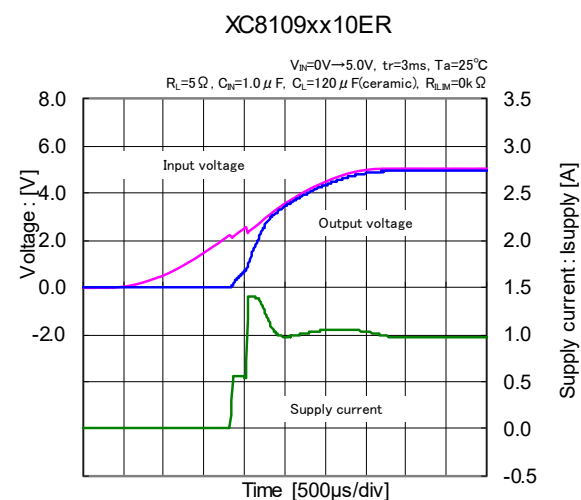


■ TYPICAL PERFORMANCE CHARACTERISTICS (Continued)

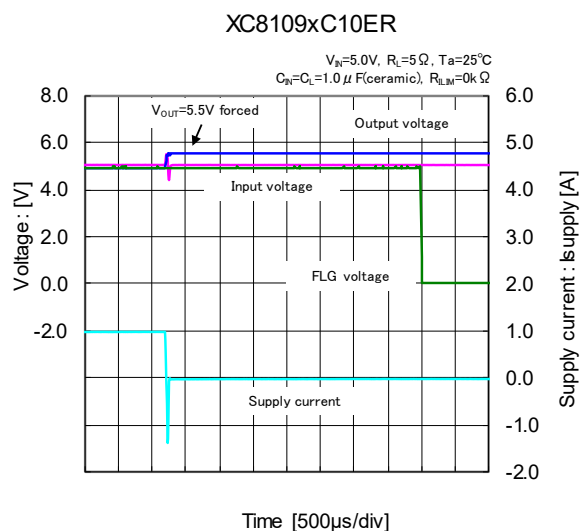
(21) UVLO transient response (CL=1.0μF)



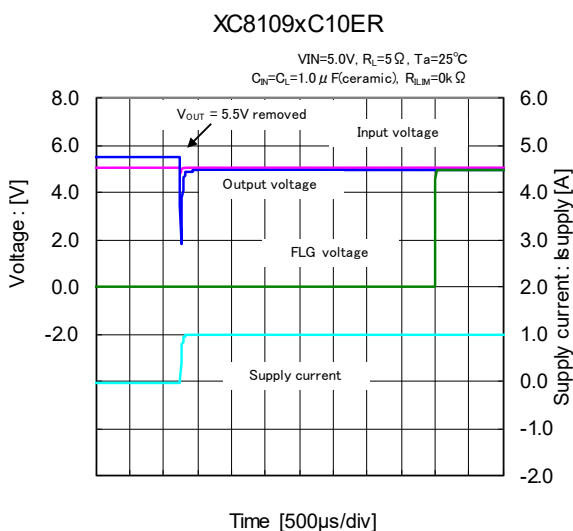
(22) UVLO transient response (CL=120μF)



(23) Reverse voltage detected voltage (CL=1.0μF)

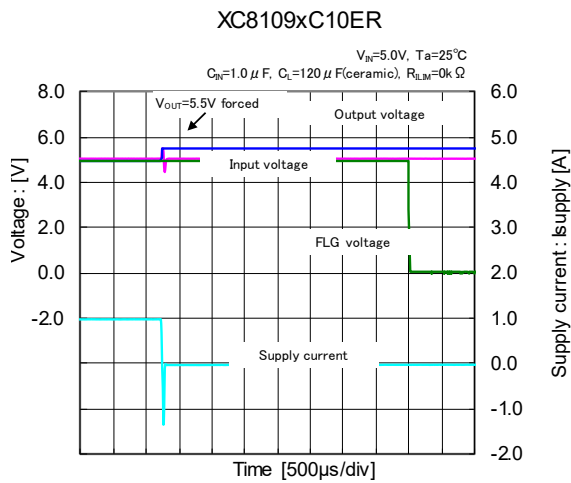


(24) Reverse voltage released voltage (CL=1.0μF)

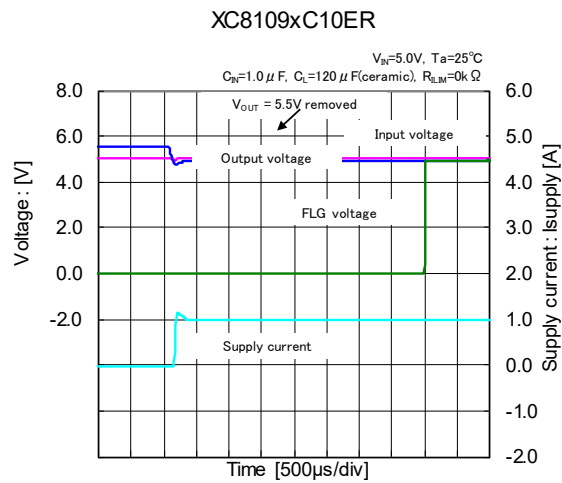


TYPICAL PERFORMANCE CHARACTERISTICS (Continued)

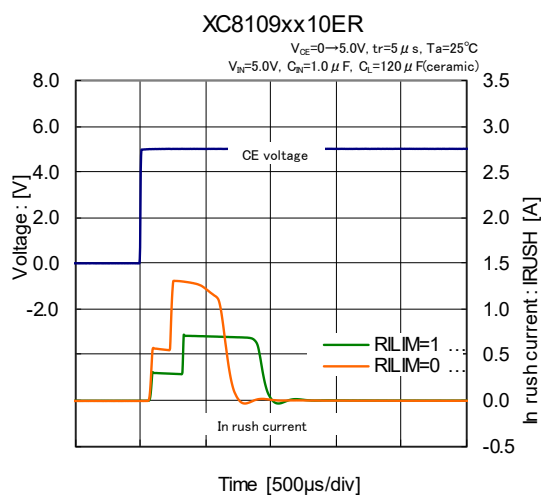
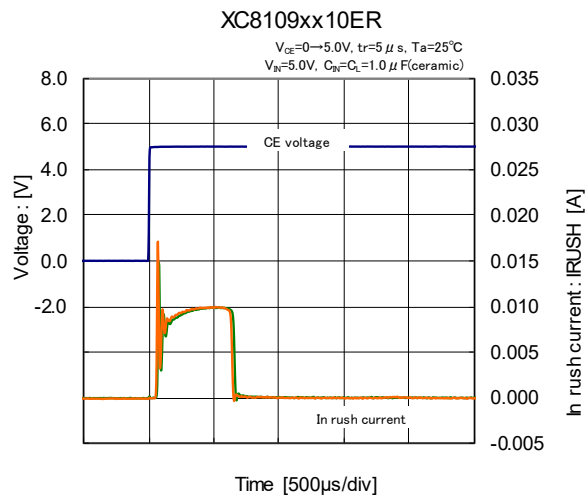
(25) Reverse voltage detected voltage (CL=120μF)



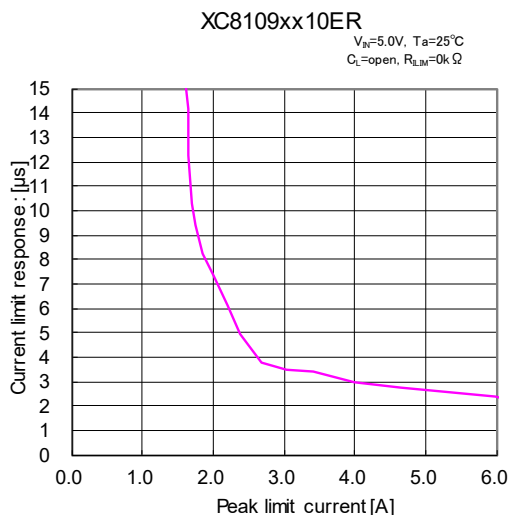
(26) Reverse voltage released voltage (CL=120μF)



(27) CE transient response

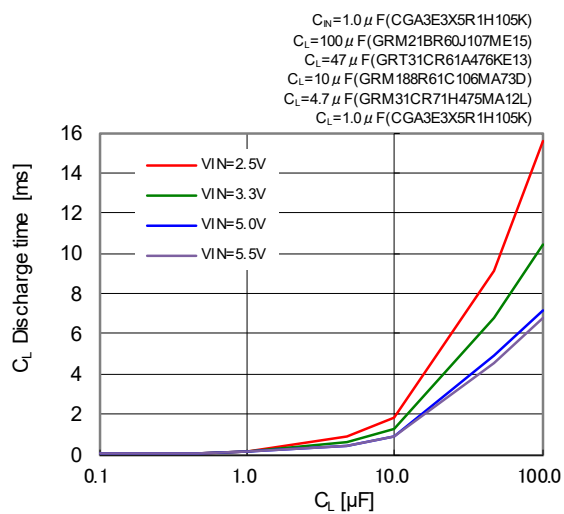


(28) Current limit adapted time

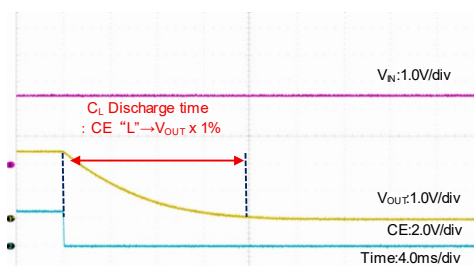


■ TYPICAL PERFORMANCE CHARACTERISTICS (Continued)

(29) C_L Discharge time



$V_{IN} = 2.5\text{V}$, $C_E = 2.5\text{V} \rightarrow 0\text{V}$, $R_L = \text{OPEN}$, $C_L = 100 \mu\text{F}$ (GRM21BR60J107ME15)



■ PACKAGING INFORMATION

For the latest package information go to, www.torexsemi.com/technical-support/packages

PACKAGE	OUTLINE / LAND PATTERN	THERMAL CHARACTERISTICS
USP-6C	USP-6C PKG	USP-6C Power Dissipation

■ MARKING RULE

① represents products series

MARK	PRODUCT SERIES
Z	XC8109*****-G

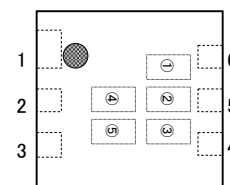
② represents type

MARK	CE LOGIC	Protection Circuits Type	PRODUCT SERIES
1	Active High	Auto-recovery	XC8109AC****-G
8	Active High	Auto-recovery , CL Discharge available	XC8109AE****-G
2	Active High	Latch-off	XC8109AD****-G
9	Active High	Latch-off , CL Discharge available	XC8109AF****-G
3	Active Low	Auto-recovery	XC8109BC****-G
V	Active Low	Auto-recovery , CL Discharge available	XC8109BE****-G
4	Active Low	Latch-off	XC8109BD****-G
X	Active Low	Latch-off , CL Discharge available	XC8109BF****-G

③ represents lout

MARK	lout(A)	PRODUCT SERIES
6	0.9	XC8109**10**-G

USP-6C



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