

MOSFET - N-Channel, POWERTRENCH®

30 V, 13.2 A, 9.5 mΩ

FDMS7694, FDMS7694-NC

General Description

This N-Channel MOSFET has been designed specifically to improve the overall efficiency and to minimize switch node ringing of DC/DC converters using either synchronous or conventional switching PWM controllers. It has been optimized for low gate charge, low $R_{DS(on)}$, fast switching speed and body diode reverse recovery performance.

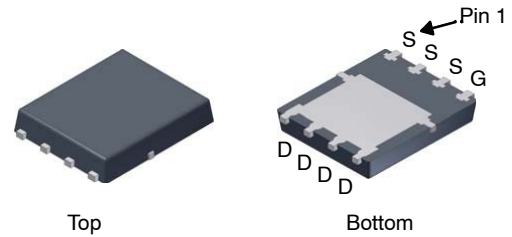
Features

- Max $R_{DS(on)}$ = 9.5 mΩ at $V_{GS} = 10$ V, $I_D = 13.2$ A
- Max $R_{DS(on)}$ = 14.5 mΩ at $V_{GS} = 4.5$ V, $I_D = 10.5$ A
- Advanced Package and Silicon Combination for Low $R_{DS(on)}$ and High Efficiency
- Next Generation Enhanced Body Diode Technology, Engineered for Soft Recovery
- MSL1 Robust Package Design
- 100% UIL Tested
- This Device is Halide Free and RoHS Compliant with Exemption 7a, Pb-Free 2LI (on second level interconnection)

Applications

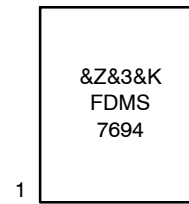
- IMVP Vcore Switching for Notebook
- VRM Vcore Switching for Desktop and Server
- OringFET / Load Switching
- DC-DC Conversion

V_{DS}	$R_{DS(on)}$ MAX	I_D Max
30 V	14.5 mΩ @ $V_{GS} = 4.5$ V	10.5 A
	9.5 mΩ @ $V_{GS} = 10$ V	13.2 A



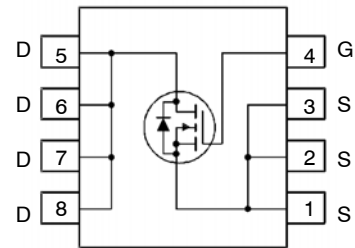
PQFN8 5X6, 1.27P
Power 56
CASE 483AE

MARKING DIAGRAM



&Z = Assembly Plant Code
& = 3-Digit Date Code
&K = 2-Digits Lot Run Code
FDMS7694 = Specific Device Code

PIN CONNECTIONS



ORDERING INFORMATION

See detailed ordering and shipping information on page 6 of this data sheet.

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MAXIMUM RATINGS (T_A = 25 °C unless otherwise noted)

Symbol	Parameter	Rating	Unit	
V _{DS}	Drain to Source Voltage	30	V	
V _{GS}	Gate to Source Voltage (Note 3)	±20	V	
I _D	Drain Current	Continuous (Package Limited), T _C = 25 °C	20	A
		Continuous (Silicon Limited), T _C = 25 °C	44	
		Continuous, T _A = 25 °C (Note 1a)	13.2	
		Pulsed	50	
E _{AS}	Single Pulse Avalanche Energy (Note 4)	21	mJ	
P _D	Power Dissipation	T _C = 25 °C	27	W
		T _A = 25 °C (Note 1a)	2.5	
T _J , T _{STG}	Operating and Storage Junction Temperature Range	-55 to +150	°C	

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

THERMAL CHARACTERISTICS

Symbol	Parameter	Rating	Unit
R _{θJC}	Thermal Resistance, Junction-to-Case	4.5	°C/W
R _{θJA}	Thermal Resistance, Junction-to-Ambient (Note 1a)	50	

ELECTRICAL CHARACTERISTICS (T_J = 25 °C unless otherwise noted)

Symbol	Parameter	Test Condition	Min	Typ	Max	Unit
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OFF CHARACTERISTICS

BV _{DSS}	Drain-to-Source Breakdown Voltage	I _D = 250 μA, V _{GS} = 0 V	30			V
$\frac{\Delta BV_{DSS}}{\Delta T_J}$	Breakdown Voltage Temperature Coefficient	I _D = 250 μA, referenced to 25 °C		16		mV/°C
I _{DSS}	Zero Gate Voltage Drain Current	V _{DS} = 24 V, V _{GS} = 0 V			1	μA
I _{GSS}	Gate-to-Source Leakage Current, Forward	V _{GS} = 20 V, V _{DS} = 0 V			100	nA

ON CHARACTERISTICS

V _{GS(th)}	Gate-to-Source Threshold Voltage	V _{GS} = V _{DS} , I _D = 250 μA	1.0	2.0	3.0	V
$\frac{\Delta V_{GS(th)}}{\Delta T_J}$	Gate-to-Source Threshold Voltage Temperature Coefficient	I _D = 250 μA, referenced to 25 °C		-6		mV/°C
R _{DS(on)}	Static Drain-to-Source On Resistance	V _{GS} = 10 V, I _D = 13.2 A		7.6	9.5	mΩ
		V _{GS} = 4.5 V, I _D = 10.5 A		11.1	14.5	
		V _{GS} = 10 V, I _D = 13.2 A, T _J = 125 °C		10.6	13.3	
g _{FS}	Forward Transconductance	V _{DS} = 5 V, I _D = 13.2 A		55		S

DYNAMIC CHARACTERISTICS

C _{iss}	Input Capacitance	V _{DS} = 15 V, V _{GS} = 0 V, f = 1 MHz		1060	1410	pF
C _{oss}	Output Capacitance			353	470	pF
C _{rss}	Reverse Transfer Capacitance			36	55	pF
R _g	Gate Resistance			0.8	1.6	Ω

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ELECTRICAL CHARACTERISTICS ($T_J = 25\text{ }^\circ\text{C}$ unless otherwise noted) (continued)

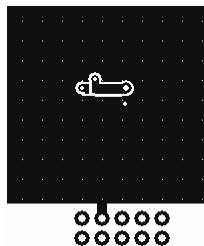
Symbol	Parameter	Test Condition	Min	Typ	Max	Unit
SWITCHING CHARACTERISTICS						
$t_{d(on)}$	Turn-On Delay Time	$V_{DD} = 15\text{ V}$, $I_D = 13.2\text{ A}$, $V_{GS} = 10\text{ V}$, $R_{GEN} = 6\ \Omega$		8.4	17	ns
t_r	Rise Time			2	10	ns
$t_{d(off)}$	Turn-Off Delay Time			18	33	ns
t_f	Fall Time			1.6	10	ns
$Q_{g(TOT)}$	Total Gate Charge	$V_{GS} = 0\text{ V to }10\text{ V}$, $V_{DD} = 15\text{ V}$, $I_D = 13.2\text{ A}$		15	22	nC
	Total Gate Charge	$V_{GS} = 0\text{ V to }4.5\text{ V}$, $V_{DD} = 15\text{ V}$, $I_D = 13.2\text{ A}$		7	10	nC
Q_{gs}	Gate-to-Source Charge	$V_{DD} = 15\text{ V}$, $I_D = 13.2\text{ A}$		3.3		nC
Q_{gd}	Gate-to-Drain "Miller" Charge			2.0		nC

DRAIN-SOURCE DIODE CHARACTERISTICS

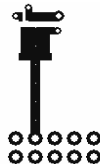
V_{SD}	Source to Drain Diode Forward Voltage	$V_{GS} = 0\text{ V}$, $I_S = 2.1\text{ A}$ (Note 2)		0.76	1.1	V
		$V_{GS} = 0\text{ V}$, $I_S = 13.2\text{ A}$ (Note 2)		0.85	1.1	
t_{rr}	Reverse Recovery Time	$I_F = 13.2\text{ A}$, $di/dt = 100\text{ A}/\mu\text{s}$		23	37	ns
Q_{rr}	Reverse Recovery Charge			7	14	nC
t_{rr}	Reverse Recovery Time	$I_F = 13.2\text{ A}$, $di/dt = 300\text{ A}/\mu\text{s}$		18	33	ns
Q_{rr}	Reverse Recovery Charge			14	26	nC

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

- $R_{\theta JA}$ is determined with the device mounted on a 1 in² pad 2 oz copper pad on a 1.5 x 1.5 in. board of FR-4 material. $R_{\theta JC}$ is guaranteed by design while $R_{\theta CA}$ is determined by the user's board design.



a. 50 °C/W when mounted on a 1 in² pad of 2 oz copper.



b. 125 °C/W when mounted on a minimum pad of 2 oz copper.

- Pulse Test: Pulse Width < 300 μs , Duty cycle < 2.0%.
- E_{AS} of 21 mJ is based on starting $T_J = 25\text{ }^\circ\text{C}$, $L = 0.3\text{ mH}$, $I_{AS} = 12\text{ A}$, $V_{DD} = 27\text{ V}$, $V_{GS} = 10\text{ V}$. 100% test at $L = 0.1\text{ mH}$, $I_{AS} = 20\text{ A}$.
- As an N-ch device, the negative V_{gs} rating is for low duty cycle pulse occurrence only. No continuous rating is implied.

TYPICAL CHARACTERISTICS ($T_J = 25\text{ }^\circ\text{C}$ unless otherwise noted)

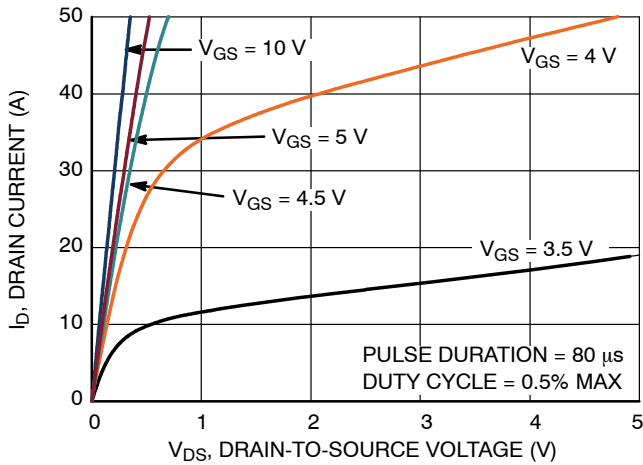


Figure 1. On Region Characteristics

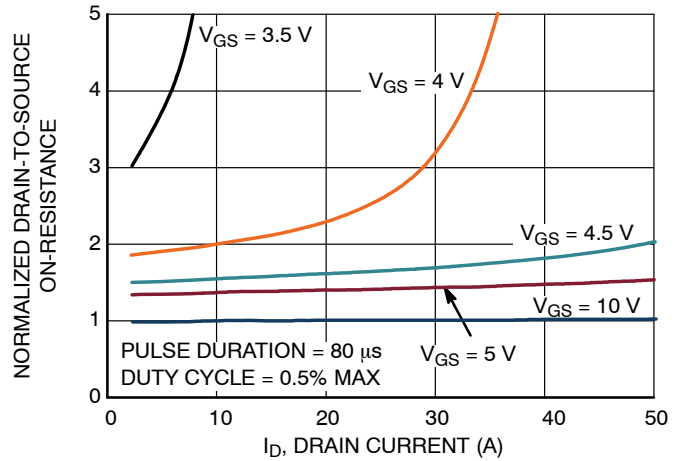


Figure 2. Normalized On-Resistance vs. Drain Current and Gate Voltage

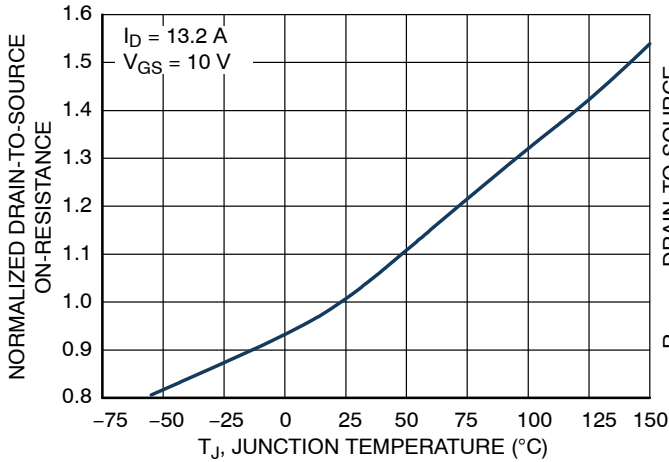


Figure 3. Normalized On Resistance vs. Junction Temperature

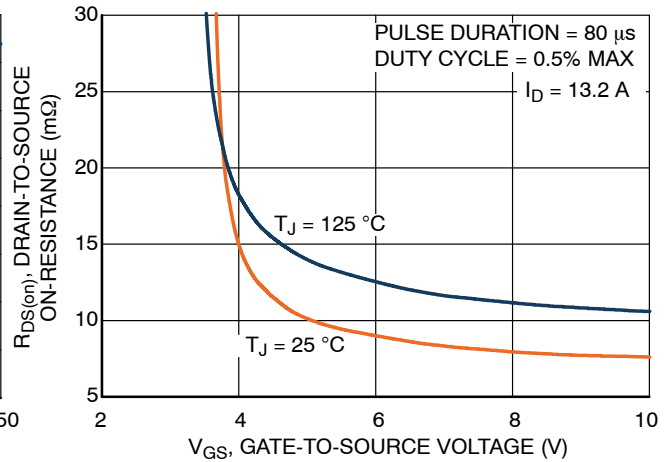


Figure 4. On-Resistance vs. Gate-to-Source Voltage

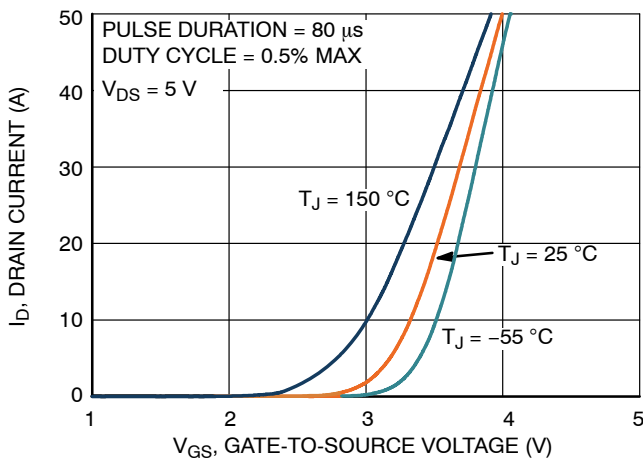


Figure 5. Transfer Characteristics

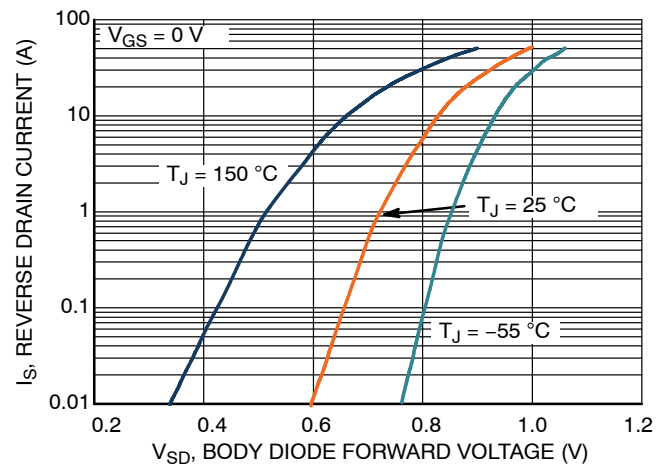


Figure 6. Source-to-Drain Diode Forward Voltage vs. Source Current

TYPICAL CHARACTERISTICS ($T_J = 25\text{ }^\circ\text{C}$ unless otherwise noted) (continued)

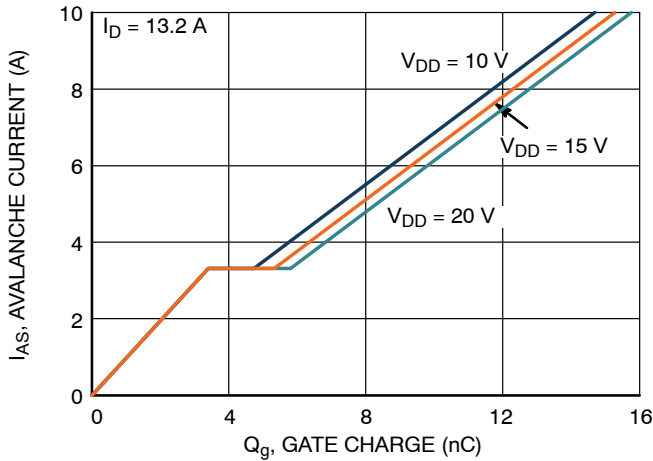


Figure 7. Gate Charge Characteristics

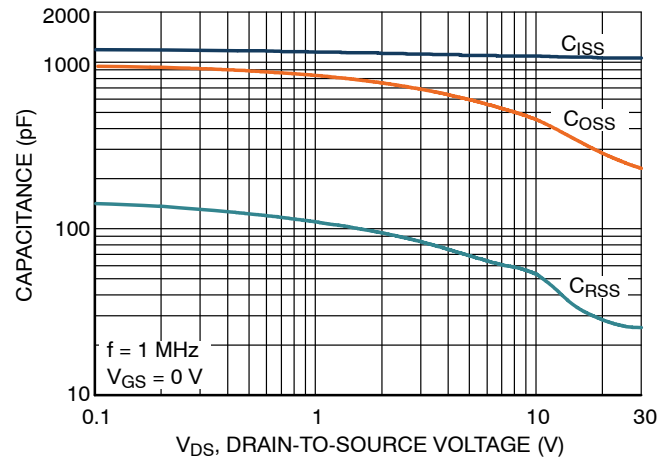


Figure 8. Capacitance vs. Drain to Source Voltage

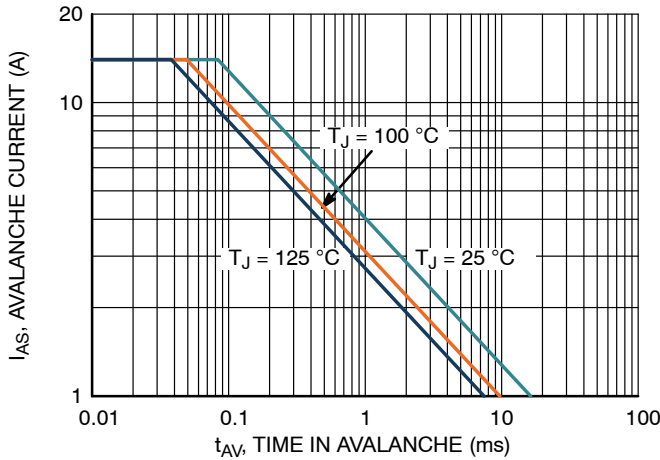


Figure 9. Unclamped Inductive Switching Capability

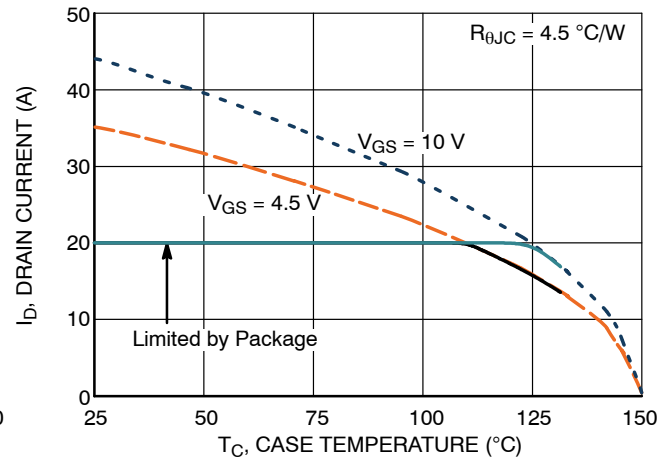


Figure 10. Maximum Continuous Drain Current vs. Case Temperature

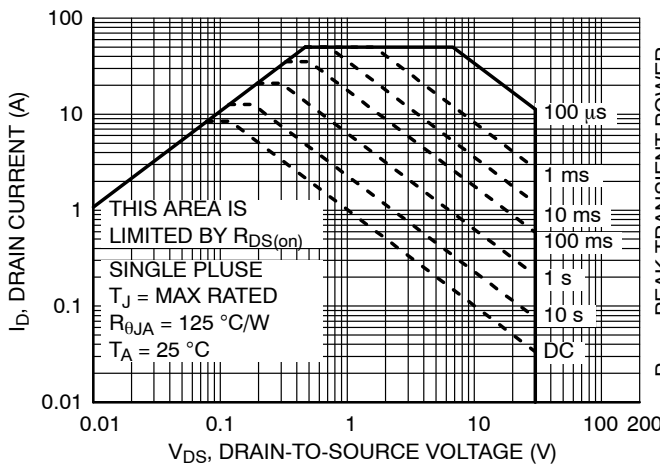


Figure 11. Forward Bias Safe Operating Area

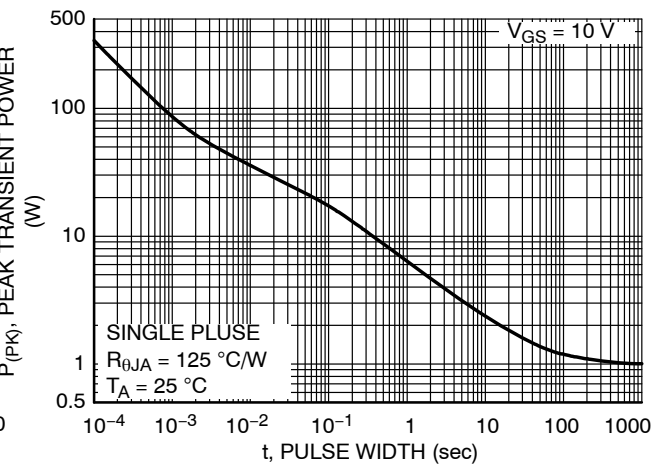


Figure 12. Single Pulse Maximum Power Dissipation

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TYPICAL CHARACTERISTICS ($T_J = 25\text{ }^\circ\text{C}$ unless otherwise noted) (continued)

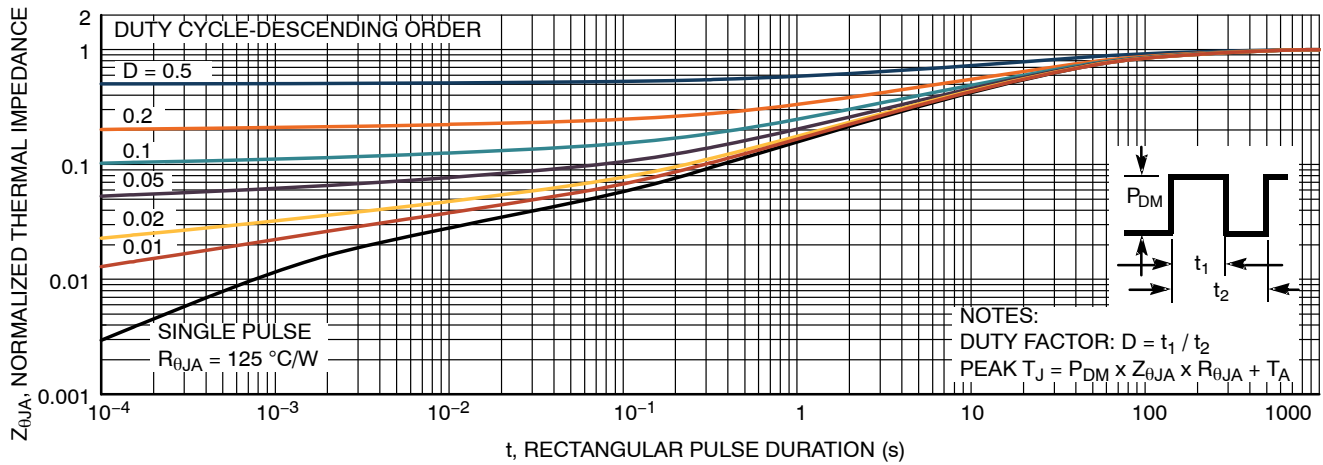


Figure 13. Junction-to-Ambient Transient Thermal Response Curve

PACKAGE MARKING AND ORDERING INFORMATION

Device	Device Marking	Package Type	Reel Size	Tape Width	Shipping [†]
FDMS7694	FDMS7694	PQFN8 5X6, 1.27P Power 56	13"	12 mm	3000 / Tape & Reel
FDMS7694-NC					

[†] For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, [BRD8011/D](#).

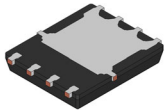
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REVISION HISTORY

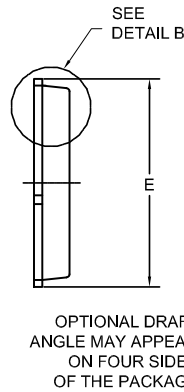
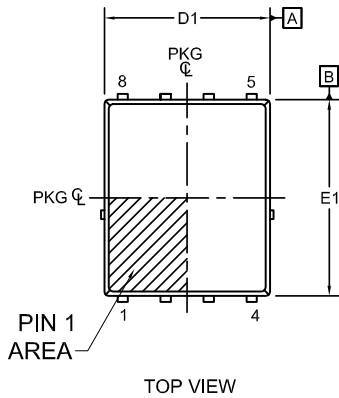
Revision	Description of Changes	Date
4	Converted the document to onsemi format. Added new OPN.	6/19/2026

This document has undergone updates prior to the inclusion of this revision history table. The changes tracked here only reflect updates made on the noted approval dates.



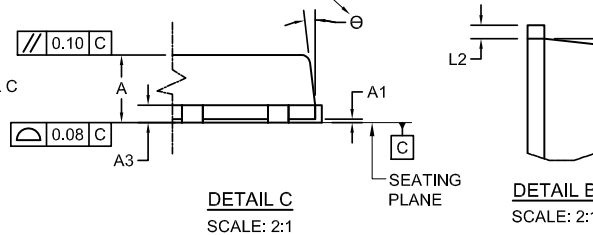
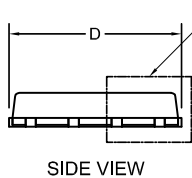
PQFN8 5X6, 1.27P
CASE 483AE
ISSUE C

DATE 21 JAN 2022

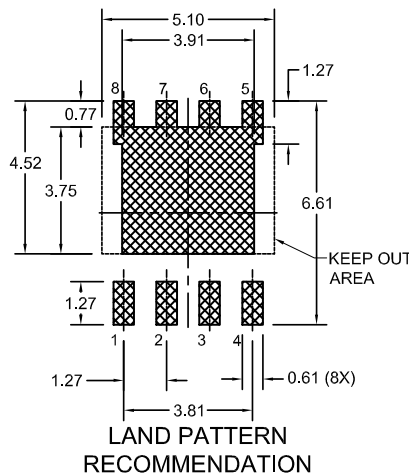
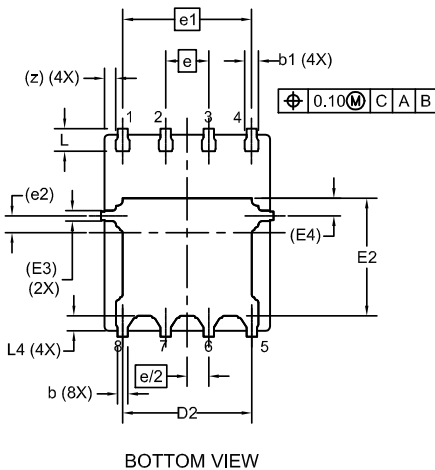


NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 2009.
2. CONTROLLING DIMENSION: MILLIMETERS
3. COPLANARITY APPLIES TO THE EXPOSED PADS AS WELL AS THE TERMINALS.
4. DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS.
5. SEATING PLANE IS DEFINED BY THE TERMINALS. "A1" IS DEFINED AS THE DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT ON THE PACKAGE BODY.
6. IT IS RECOMMENDED TO HAVE NO TRACES OR VIAS WITHIN THE KEEP OUT AREA.



DIM	MILLIMETERS		
	MIN.	NOM.	MAX.
A	0.90	1.00	1.10
A1	0.00	-	0.05
b	0.21	0.31	0.41
b1	0.31	0.41	0.51
A3	0.15	0.25	0.35
D	4.90	5.00	5.20
D1	4.80	4.90	5.00
D2	3.61	3.82	3.96
E	5.90	6.15	6.25
E1	5.70	5.80	5.90
E2	3.38	3.48	3.78
E3	0.30 REF		
E4	0.52 REF		
e	1.27 BSC		
e/2	0.635 BSC		
e1	3.81 BSC		
e2	0.50 REF		
L	0.51	0.66	0.76
L2	0.05	0.18	0.30
L4	0.34	0.44	0.54
z	0.34 REF		
θ	0°	-	12°



*FOR ADDITIONAL INFORMATION ON OUR PB-FREE STRATEGY AND SOLDERING DETAILS, PLEASE DOWNLOAD THE ON SEMICONDUCTOR SOLDERING AND MOUNTING TECHNIQUES REFERENCE MANUAL, SOLDERRM/D.

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