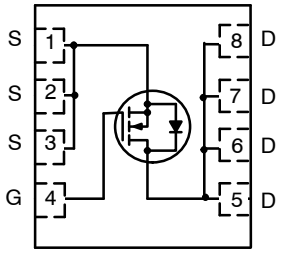
MOSFET – N-Channel, Shielded Gate, POWERTRENCH®

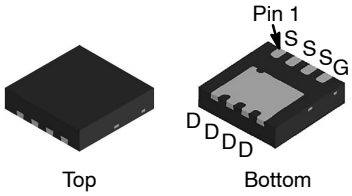
100 V, 18 A, 23 mΩ

FDMC86102L

V_{DS}	$R_{DS(ON)}$ MAX	I_D MAX
100 V	23 mΩ @ 10 V	18 A
	34 mΩ @ 4.5 V	



N-CHANNEL MOSFET



WDFN8 3.3 × 3.3, 0.65P
CASE 511DH

General Description

This N−Channel MOSFET is produced using **onsemi**'s advanced POWERTRENCH process that incorporates Shielded Gate technology. This process has been optimized for the on−state resistance and yet maintain superior switching performance.

Features

- Shielded Gate MOSFET Technology
- Max $R_{DS(on)}$ = 23 mΩ at V_{GS} = 10 V, I_D = 7 A
- Max $R_{DS(on)}$ = 34 mΩ at V_{GS} = 4.5 V, I_D = 5.5 A
- Low Profile – 1 mm Max in Power 33
- Pb−Free, Halide Free and RoHS Compliant

Applications

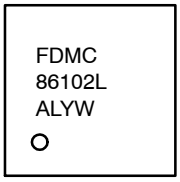
- DC−DC Conversion

MAXIMUM RATINGS (T_A = 25°C unless otherwise noted)

Symbol	Parameter	Value	Unit
V_{DS}	Drain to Source Voltage	100	V
V_{GS}	Gate to Source Voltage	±20	V
I_D	Drain Current: Continuous, T_C = 25°C Continuous, T_A = 25°C (Note 1a) Pulsed	 18 7 30	A
E_{AS}	Single Pulse Avalanche Energy (Note 3)	63	mJ
P_D	Power Dissipation: T_C = 25°C T_A = 25°C (Note 1a)	 41 2.3	W
T_J, T_{STG}	Operating and Storage Junction Temperature Range	−55 to +150	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

MARKING DIAGRAM



FDMC86102L = Specific Device Code
A = Assembly Site
L = Wafer Lot Number
YW = Assembly Start Week

ORDERING INFORMATION

Device	Package	Shipping†
FDMC86102L	WDFN8 (Pb−Free, Halide Free)	3000 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

THERMAL CHARACTERISTICS

Symbol	Parameter	Value	Unit
$R_{\theta JC}$	Thermal Resistance, Junction to Case	3	°C/W
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient (Note 1a)	53	

ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise noted)

Symbol	Parameter	Test Condition	Min	Typ	Max	Unit
OFF CHARACTERISTICS						
BV_{DSS}	Drain to Source Breakdown Voltage	I_D = 250 μA, V_{GS} = 0 V	100	–	–	V
$\Delta BV_{DSS}/\Delta T_J$	Breakdown Voltage Temperature Coefficient	I_D = 250 μA, referenced to 25°C	–	71	–	mV/°C
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS} = 80 V, V_{GS} = 0 V	–	–	1	μA
I_{GSS}	Gate to Source Leakage Current	V_{GS} = ±20 V, V_{DS} = 0 V	–	–	±100	nA
ON CHARACTERISTICS						
$V_{GS(th)}$	Gate to Source Threshold Voltage	V_{GS} = V_{DS}, I_D = 250 μA	1	1.8	3	V
$\Delta V_{GS(th)}/\Delta T_J$	Gate to Source Threshold Voltage Temperature Coefficient	I_D = 250 μA, referenced to 25°C	–	–6	–	mV/°C
$R_{DS(on)}$	Static Drain to Source On Resistance	V_{GS} = 10 V, I_D = 7 A	–	18.9	23	mΩ
		V_{GS} = 4.5 V, I_D = 5.5 A	–	24.9	34	
		V_{GS} = 10 V, I_D = 7 A, T_J = 125°C	–	31.9	39	
g_{FS}	Forward Transconductance	V_{DS} = 5 V, I_D = 7 A	–	26	–	S
DYNAMIC CHARACTERISTICS						
C_{iss}	Input Capacitance	V_{DS} = 50 V, V_{GS} = 0 V, f = 1 MHz	–	999	1330	pF
C_{oss}	Output Capacitance		–	178	240	pF
C_{rss}	Reverse Transfer Capacitance		–	7.6	15	pF
R_g	Gate Resistance		–	0.5	–	Ω
SWITCHING CHARACTERISTICS						
$t_{d(on)}$	Turn-On Delay Time	V_{DD} = 50 V, I_D = 7 A, V_{GS} = 10 V, R_{GEN} = 6 Ω	–	7.7	16	ns
t_r	Rise Time		–	2.2	10	ns
$t_{d(off)}$	Turn-Off Delay Time		–	19	34	ns
t_f	Fall Time		–	2.4	10	ns
$Q_{g(TOT)}$	Total Gate Charge	V_{GS} = 0 V to 10 V, V_{DD} = 50 V, I_D = 7 A	–	15	22	nC
		V_{GS} = 0 V to 4.5 V, V_{DD} = 50 V, I_D = 7 A	–	7.3	11	nC
Q_{gs}	Gate to Source Charge	V_{DD} = 50 V, I_D = 7 A	–	2.7	–	nC
Q_{gd}	Gate to Drain “Miller” Charge	V_{DD} = 50 V, I_D = 7 A	–	2.3	–	nC

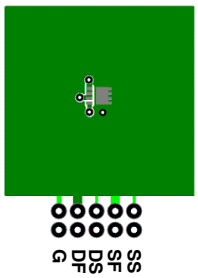
ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise noted) (continued)

Symbol	Parameter	Test Condition	Min	Typ	Max	Unit
DRAIN-SOURCE DIODE CHARACTERISTICS						
V_{SD}	Source to Drain Diode Forward Voltage	V_{GS} = 0 V, I_S = 7 A (Note 2)	–	0.81	1.3	V
		V_{GS} = 0 V, I_S = 2 A (Note 2)	–	0.74	1.2	
t_{rr}	Reverse Recovery Time	I_F = 7 A, di/dt = 100 A/μs	–	45	72	ns
Q_{rr}	Reverse Recovery Charge		–	45	72	nC

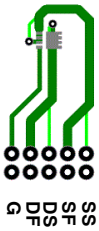
Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

NOTES:

1. $R_{\theta JA}$ is determined with the device mounted on a 1 in2 pad 2 oz copper pad on a 1.5 x 1.5 in. board of FR−4 material. $R_{\theta JC}$ is guaranteed by design while $R_{\theta CA}$ is determined by the user's board design.



a) 53°C/W when mounted on a 1 in^2 pad of 2 oz copper.



b) 125°C/W when mounted on a minimum pad of 2 oz copper.

2. Pulse Test: Pulse Width < 300 μs, Duty cycle < 2.0%.
3. Starting T_J = 25°C; N-ch: L = 1 mH, I_{AS} = 11.3 A, V_{DD} = 90 V, V_{GS} = 10 V.

TYPICAL CHARACTERISTICS

(T_J = 25°C unless otherwise noted)

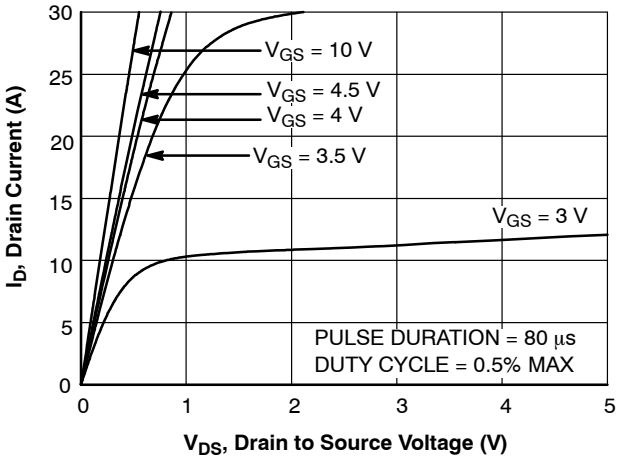


Figure 1. On−Region Characteristics

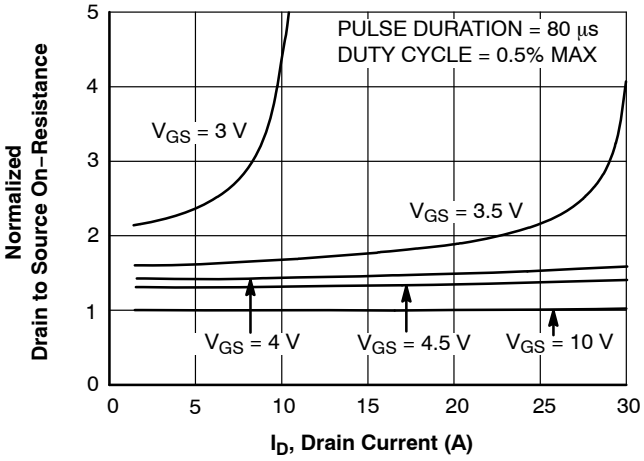


Figure 2. Normalized On−Resistance vs. Drain Current and Gate Voltage

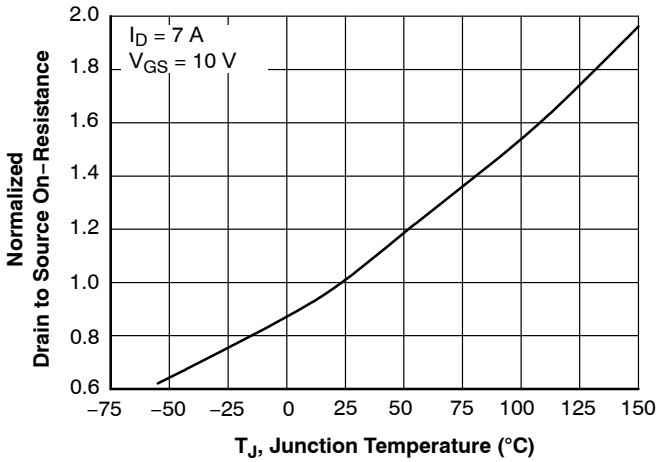


Figure 3. Normalized On−Resistance vs. Junction Temperature

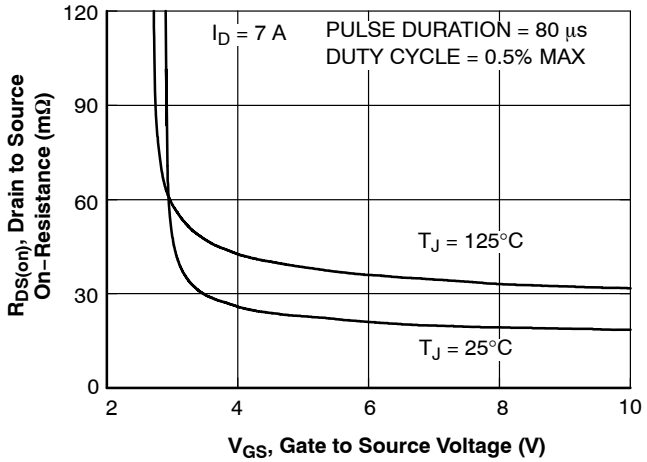


Figure 4. On−Resistance vs. Gate to Source Voltage

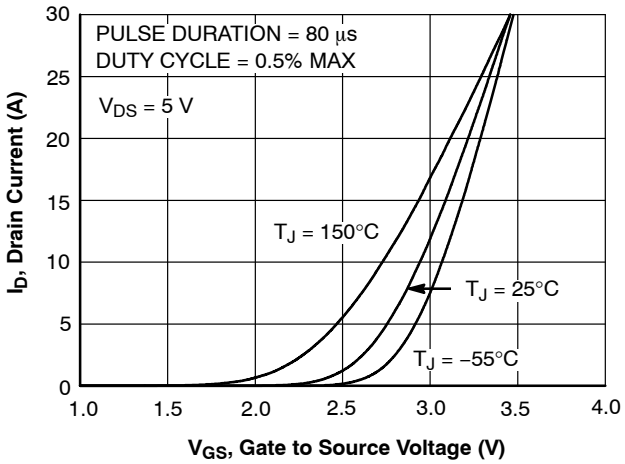


Figure 5. Transfer Characteristics

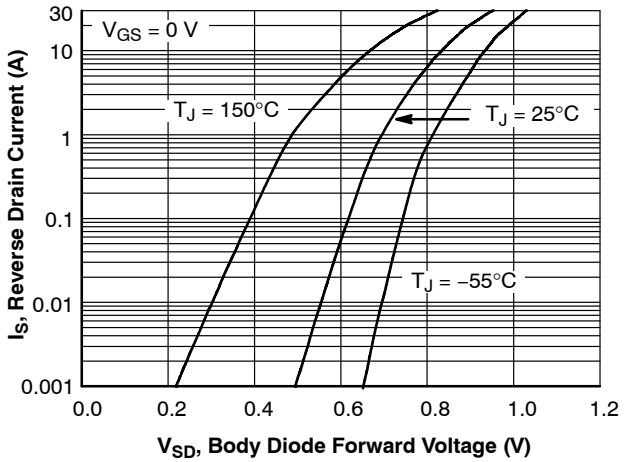


Figure 6. Source to Drain Diode Forward Voltage vs. Source Current

TYPICAL CHARACTERISTICS (continued)

(T_J = 25°C unless otherwise noted)

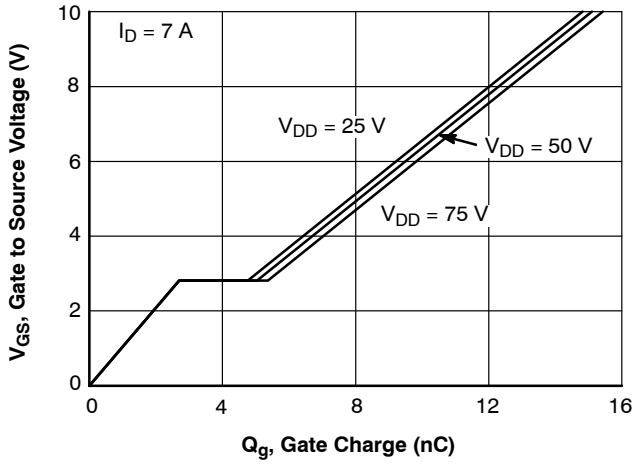


Figure 7. Gate Charge Characteristics

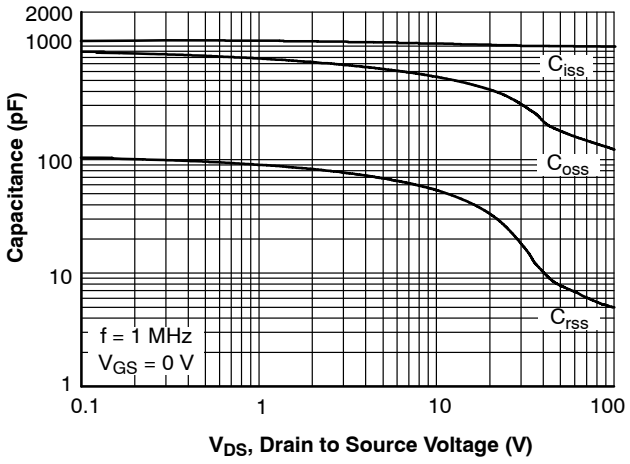


Figure 8. Capacitance vs. Drain to Source Voltage

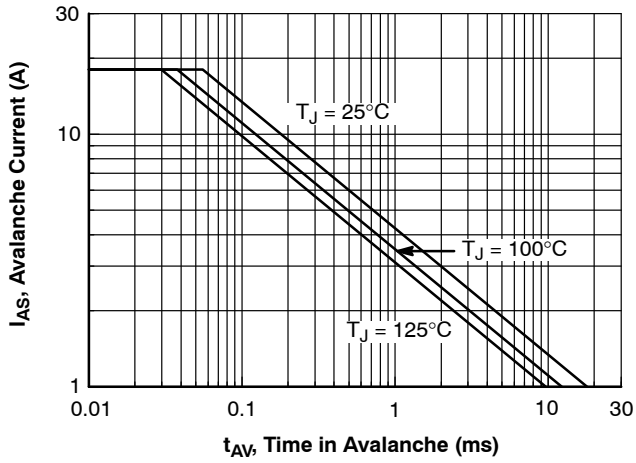


Figure 9. Unclamped Inductive Switching Capability

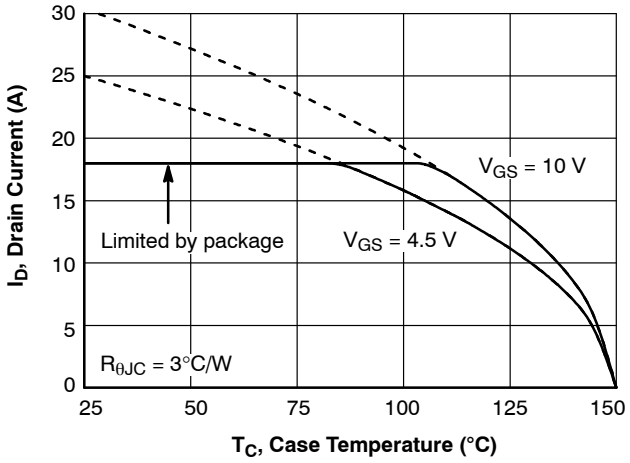


Figure 10. Maximum Continuous Drain Current vs. Case Temperature

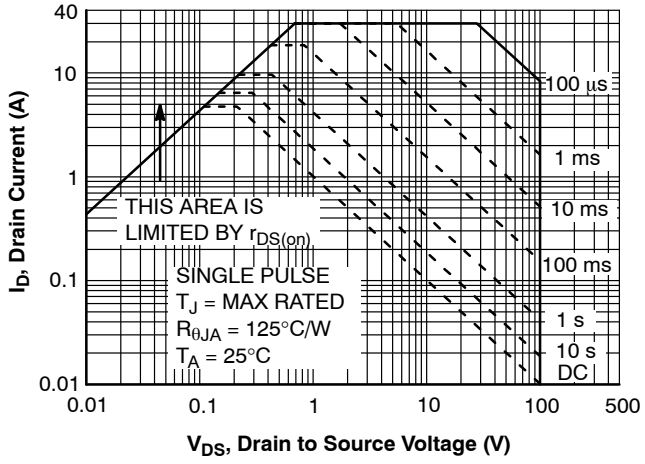


Figure 11. Forward Bias Safe Operating Area

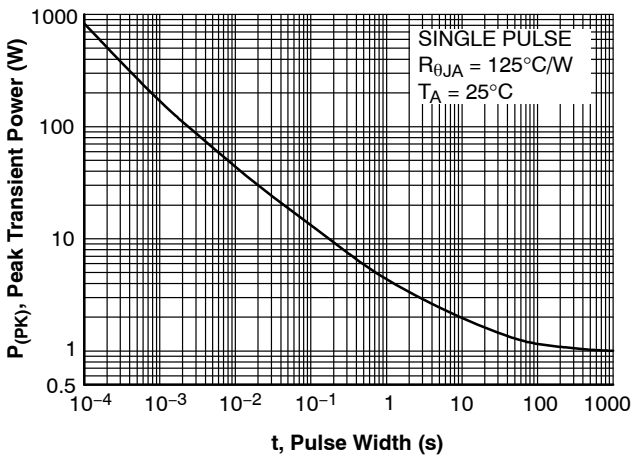


Figure 12. Single Pulse Maximum Power Dissipation

TYPICAL CHARACTERISTICS (continued)

(T_J = 25°C unless otherwise noted)

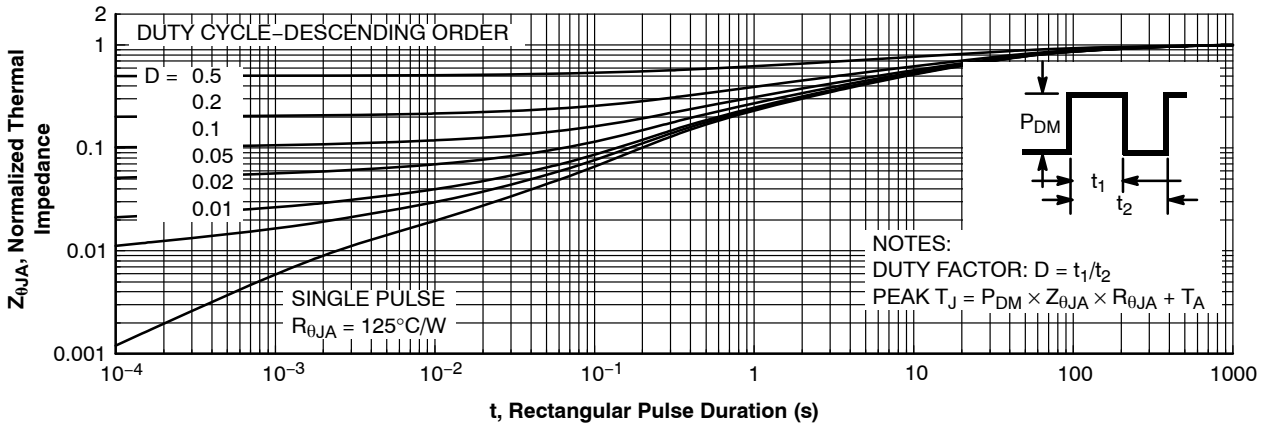
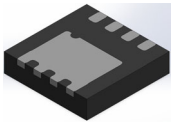
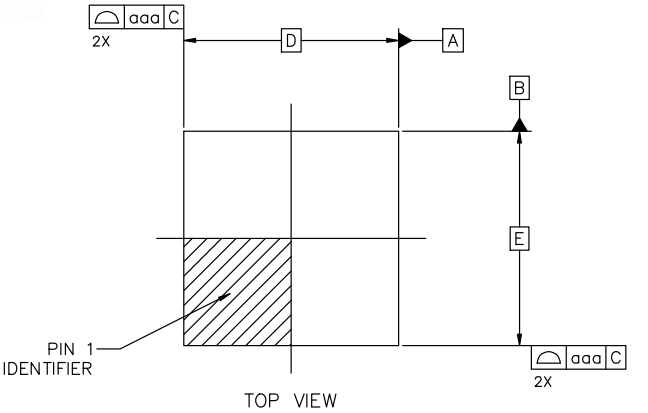


Figure 13. Junction−to−Ambient Transient Thermal Response Curve



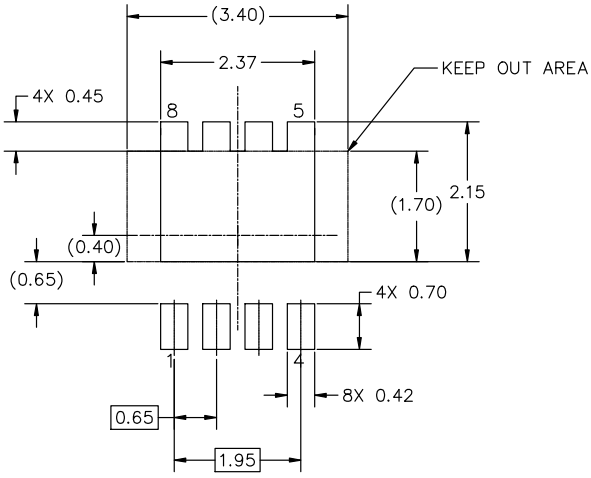
WDFN−8 3.30x3.30x0.75, 0.65P
CASE 511DH
ISSUE A

DATE 04 DEC 2025



NOTES:
1. DIMENSIONING AND TOLERANCING AS PER ASME Y14.5M, 2018.
2. CONTROLLING DIMENSION: MILLIMETERS.

MILLIMETERS			
DIM	MIN	NOM	MAX
A	0.70	0.75	0.80
A1	0.00	0.025	0.05
A3		0.20 REF	
b	0.30	0.35	0.40
D		3.30 BSC	
D2	2.22	2.27	2.32
E		3.30 BSC	
E2	1.95	2.00	2.05
e		0.65 BSC	
k		0.80 REF	
k1		0.50 REF	
L	0.45	0.50	0.55
L1	0.25	0.30	0.35
TOLERANCE FORM & POSITION			
aaa		0.05	
bbb		0.10	
ccc		0.10	
ddd		0.05	
eee		0.08	



RECOMMENDED MOUNTING FOOTPRINT

* For additional information on our Pb−Free strategy and soldering details, please download the onsemi Soldering and Mounting Techniques reference manual, SOLDERRM/D.

GENERIC MARKING DIAGRAM*

XXXX = Specific Device Code
A = Assembly Location
Y = Year
WW = Work Week

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, "G" or microdot "▪", may or may not be present. Some products may not follow the Generic Marking.

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