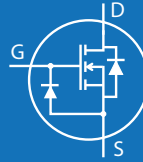


EPC2038 – Enhancement Mode Power Transistor with Integrated Reverse Gate Clamp Diode

 $V_{DS}, 100\text{ V}$
 $R_{DS(on)}, 3300\text{ m}\Omega$
 $I_D, 0.5\text{ A}$


Revised July 3, 2023

Gallium Nitride's exceptionally high electron mobility and low temperature coefficient allows very low $R_{DS(on)}$, while its lateral device structure and majority carrier diode provide exceptionally low Q_G and zero Q_{RR} . The end result is a device that can handle tasks where very high switching frequency, and low on-time are beneficial as well as those where on-state losses dominate.

Questions:
Ask a GaN
Expert



Maximum Ratings			
PARAMETER		VALUE	UNIT
V_{DS}	Drain-to-Source Voltage (Continuous)	100	V
	Drain-to-Source Voltage (up to 10,000 5 ms pulses at 150°C)	120	
I_D	Continuous ($T_A = 25^\circ\text{C}$, $R_{\theta JA} = 100^\circ\text{C/W}$)	0.5	A
	Pulsed (25°C , $T_{PULSE} = 300\ \mu\text{s}$)	0.5	
V_{GS}	Gate-to-Source Voltage	6	V
T_J	Operating Temperature	-40 to 150	°C
T_{STG}	Storage Temperature	-55 to 150	

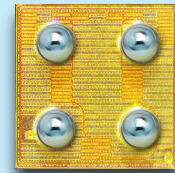
Thermal Characteristics			
PARAMETER		TYP	UNIT
$R_{\theta JC}$	Thermal Resistance, Junction-to-Case	27	°C/W
$R_{\theta JB}$	Thermal Resistance, Junction-to-Board	91	
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient (Note 1)	100	

Note 1: $R_{\theta JA}$ is determined with the device mounted on one square inch of copper pad, single layer 2 oz copper on FR4 board. See https://epc-co.com/epc/documents/product-training/Appnote_Thermal_Performance_of_eGaN_FETs.pdf for details.

Static Characteristics ($T_J = 25^\circ\text{C}$ unless otherwise stated)						
PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
BV_{DSS}	Drain-to-Source Voltage	$V_{GS} = 0\text{ V}$, $I_D = 125\ \mu\text{A}$	100			V
I_{DSS}	Drain-Source Leakage	$V_{GS} = 0\text{ V}$, $V_{DS} = 80\text{ V}$		20	100	μA
I_{GSS}	Gate-to-Source Forward Leakage	$V_{GS} = 5\text{ V}$, $T_J = 25^\circ\text{C}$		0.0001	0.5	mA
	Gate-to-Source Forward Leakage [#]	$V_{GS} = 5\text{ V}$, $T_J = 125^\circ\text{C}$		0.002	1	
V_F	Source-Gate Forward Voltage	$I_F = 0.2\text{ mA}$, $V_{DS} = 0\text{ V}$			2.7	V
$V_{GS(TH)}$	Gate Threshold Voltage	$V_{DS} = V_{GS}$, $I_D = 0.1\text{ mA}$	0.8	1.7	2.5	V
$R_{DS(on)}$	Drain-Source On Resistance	$V_{GS} = 5\text{ V}$, $I_D = 0.05\text{ A}$		2100	3300	m Ω
V_{SD}	Source-Drain Forward Voltage [#]	$V_{GS} = 0\text{ V}$, $I_S = 0.1\text{ A}$		2.9		V

[#] Defined by design. Not subject to production test.

All measurements were done with substrate connected to source.



Die size: 0.9 x 0.9 mm

EPC2038 eGaN® FETs are supplied only in passivated die form with solder bumps.

Applications

Synchronous Bootstrap for:

- High speed DC-DC conversion
- Wireless power transfer
- High frequency hard-switching and soft-switching circuits
- Lidar/pulsed power applications
- Class-D audio

Benefits

- Ultra high efficiency
- Ultra low $R_{DS(on)}$
- Ultra low Q_G
- Ultra small footprint

Scan QR code or click link below for more information including reliability reports, device models, demo boards!



<https://l.ead.me/EPC2038>

Dynamic Characteristics# (T_j = 25°C unless otherwise stated)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
C _{ISS}	Input Capacitance	V _{GS} = 0 V, V _{DS} = 50 V		7	8.4	pF
C _{RSS}	Reverse Transfer Capacitance			0.02		
C _{OSS}	Output Capacitance			1.6	2.4	
C _{OSS(ER)}	Effective Output Capacitance, Energy Related (Note 2)	V _{GS} = 0 V, V _{DS} = 0 to 50 V		2.2		
C _{OSS(TR)}	Effective Output Capacitance, Time Related (Note 3)			2.7		
R _G	Gate Resistance			4.8		Ω
Q _G	Total Gate Charge	V _{GS} = 5 V, V _{DS} = 50 V, I _D = 0.05 A		44		pC
Q _{GS}	Gate-to-Source Charge	V _{DS} = 50 V, I _D = 0.05 A		20		
Q _{GD}	Gate-to-Drain Charge			4		
Q _{G(TH)}	Gate Charge at Threshold			18		
Q _{OSS}	Output Charge	V _{GS} = 0 V, V _{DS} = 50 V		134		
Q _{RR}	Source-Drain Recovery Charge			0		

Defined by design. Not subject to production test.

All measurements were done with substrate connected to source.

Note 2: C_{OSS(ER)} is a fixed capacitance that gives the same stored energy as C_{OSS} while V_{DS} is rising from 0 to 50% BV_{DSS}.

Note 3: C_{OSS(TR)} is a fixed capacitance that gives the same charging time as C_{OSS} while V_{DS} is rising from 0 to 50% BV_{DSS}.

Figure 1: Typical Output Characteristics at 25°C

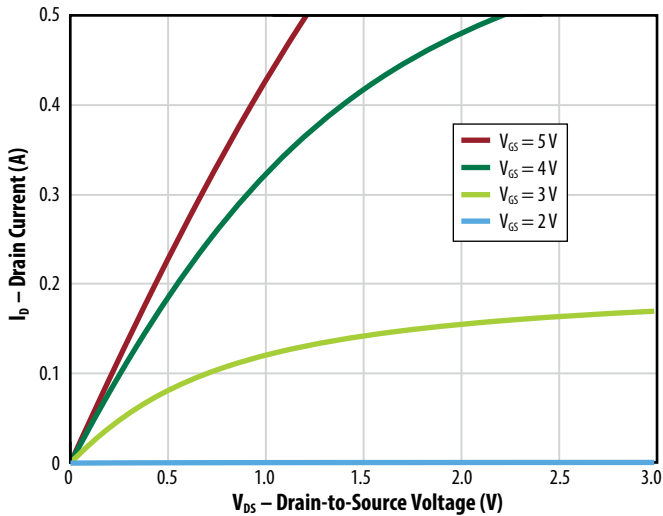


Figure 2: Typical Transfer Characteristics

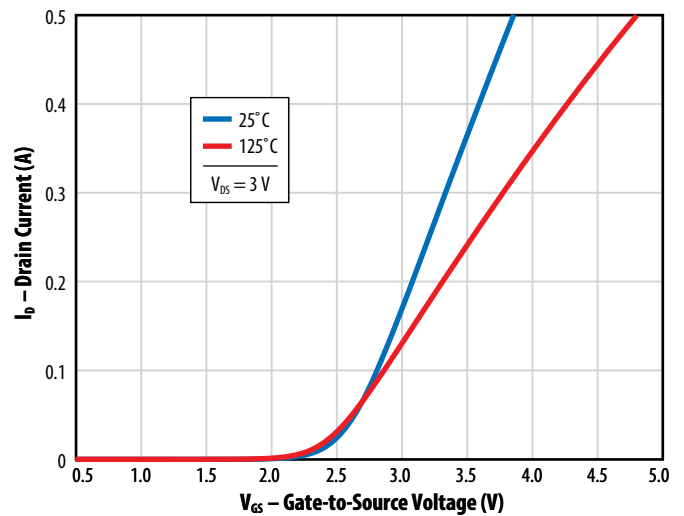


Figure 3: Typical R_{DS(on)} vs. V_{GS} for Various Drain Currents

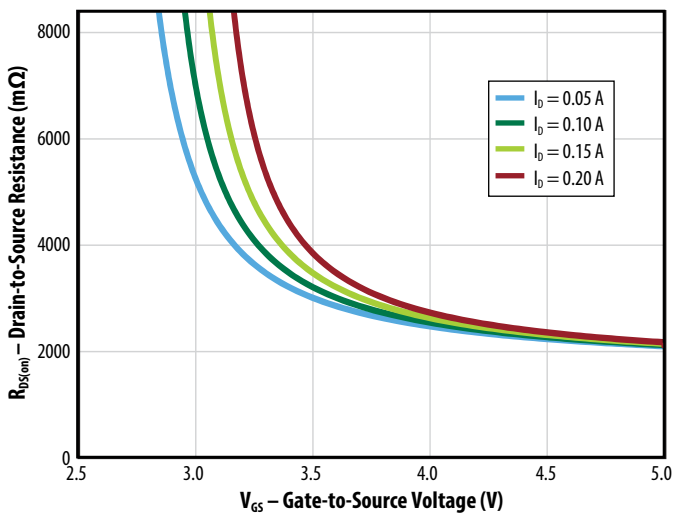


Figure 4: Typical R_{DS(on)} vs. V_{GS} for Various Temperatures

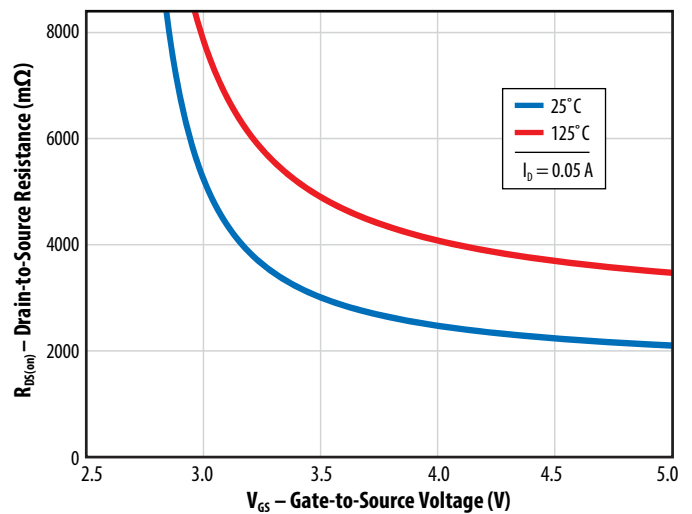


Figure 5a: Typical Capacitance (Linear Scale)

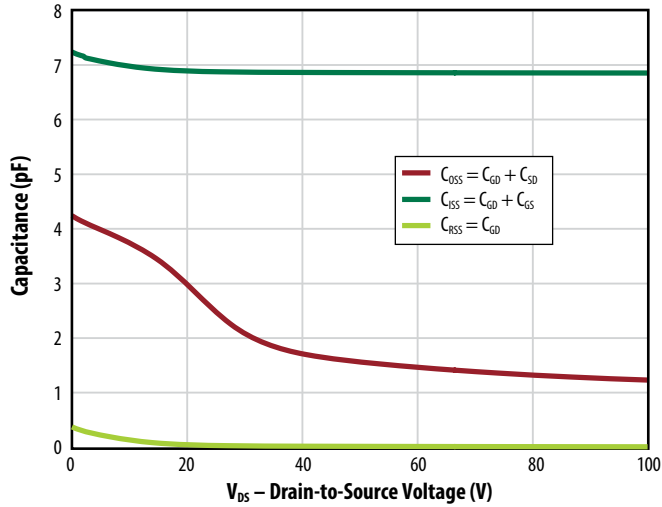


Figure 5b: Typical Capacitance (Log Scale)

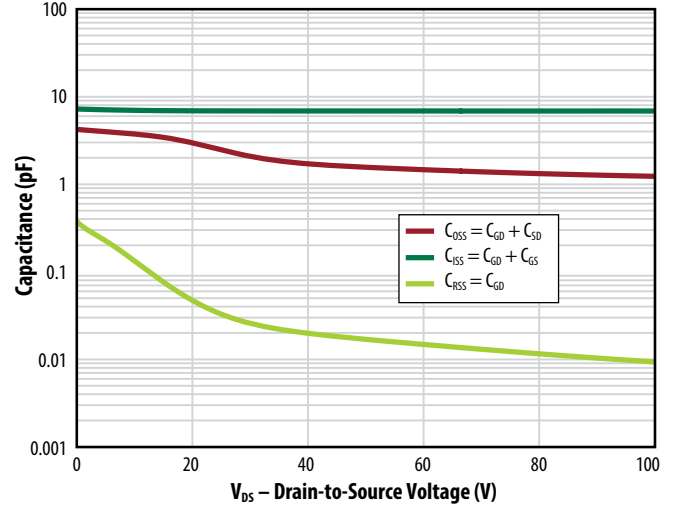


Figure 6: Typical Gate Charge

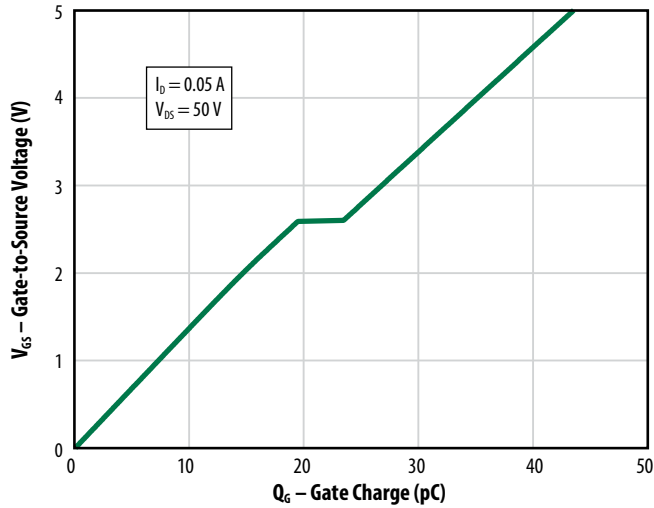
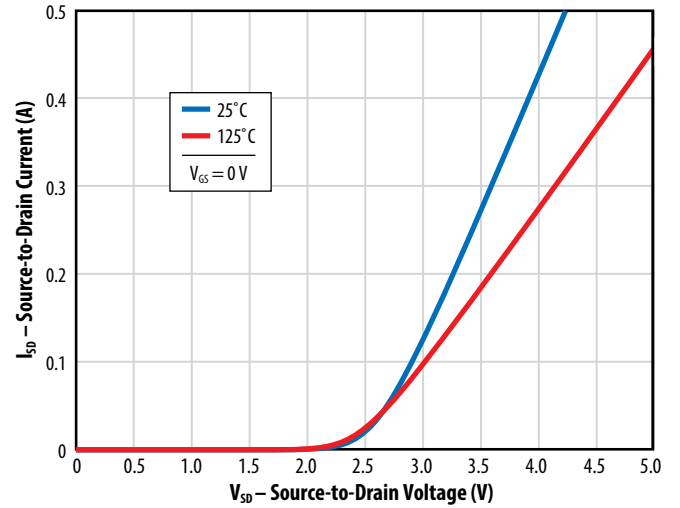


Figure 7: Typical Reverse Drain-Source Characteristics



Note: Negative gate drive voltage increases the reverse drain-source voltage. EPC recommends 0V for OFF.

Figure 8: Typical Normalized On-State Resistance vs. Temp.

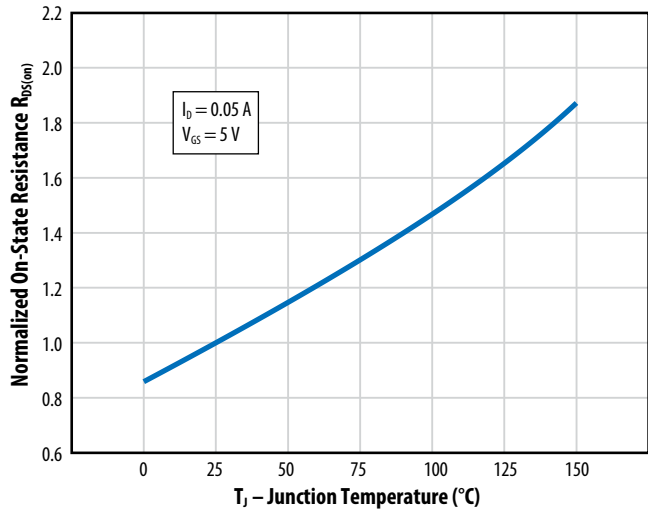


Figure 9: Typical Normalized Threshold Voltage vs. Temp.

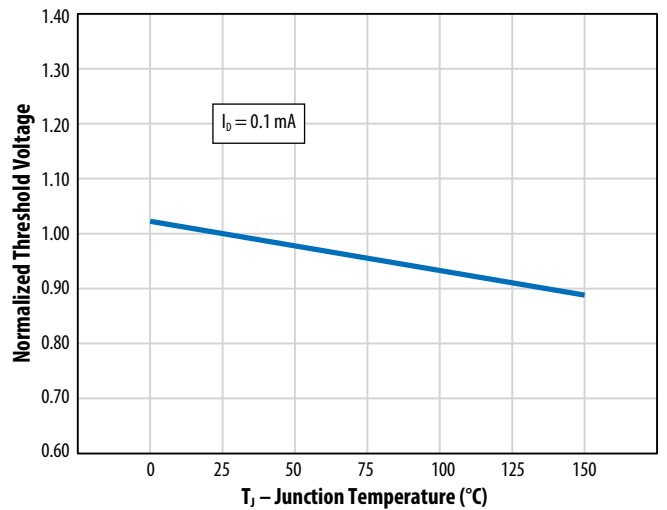


Figure 10: Typical Transient Thermal Response Curves

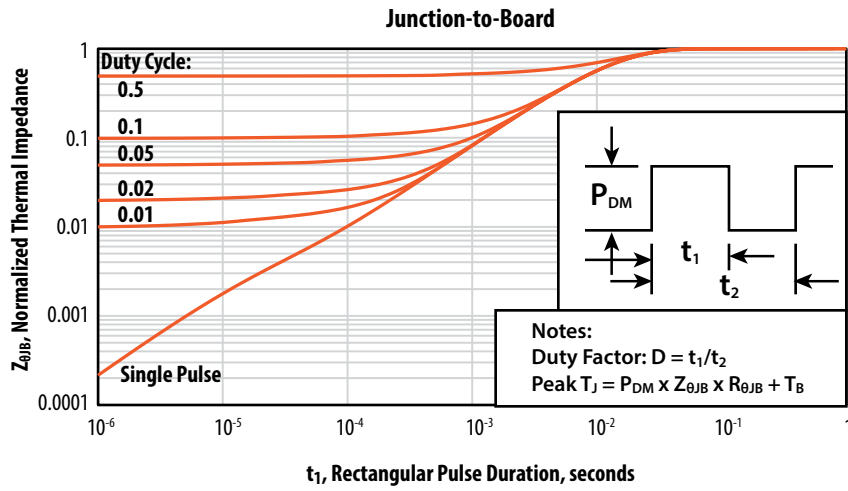
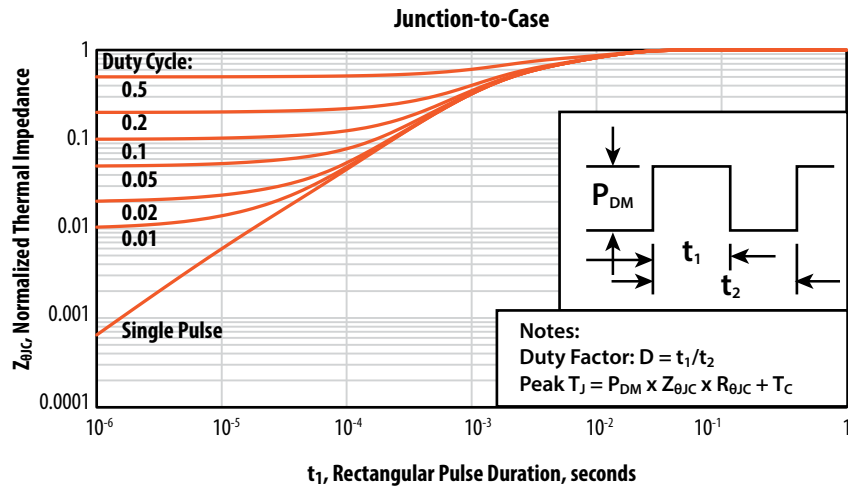
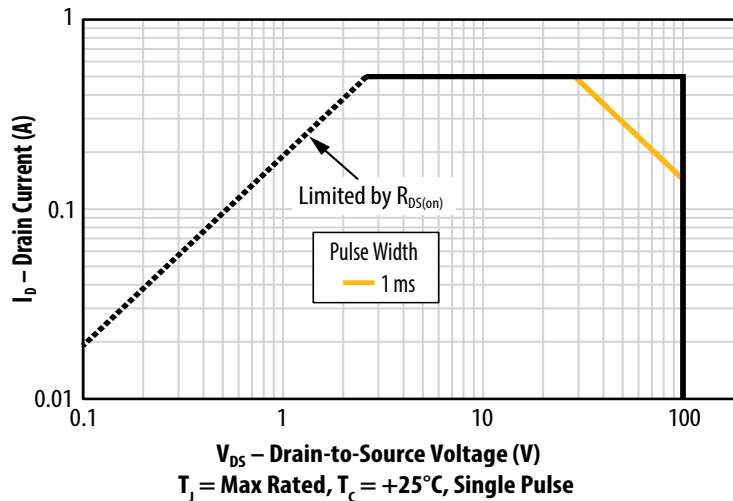
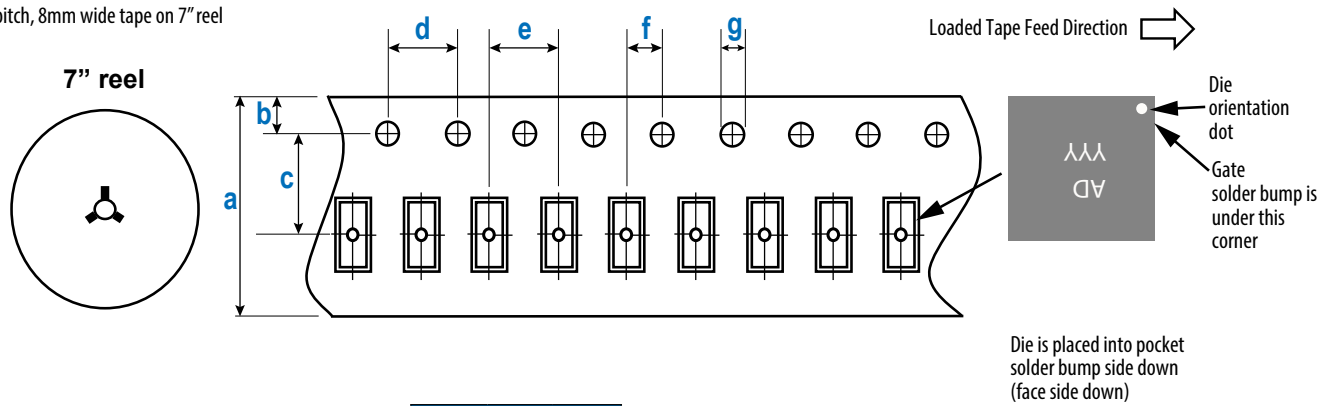


Figure 11: Safe Operating Area



TAPE AND REEL CONFIGURATION

4mm pitch, 8mm wide tape on 7" reel

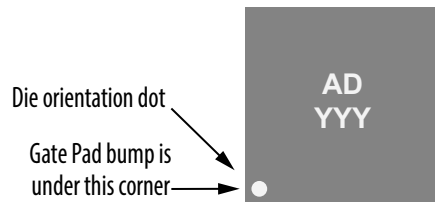


Dimension (mm)			
EPC2038 (Note 1)	Target	MIN	MAX
a	8.00	7.90	8.30
b	1.75	1.65	1.85
c (Note 2)	3.50	3.45	3.55
d	4.00	3.90	4.10
e	4.00	3.90	4.10
f (Note 2)	2.00	1.95	2.05
g	1.50	1.50	1.60

Note 1: MSL 1 (moisture sensitivity level 1) classified according to IPC/ JEDEC industry standard.

Note 2: Pocket position is relative to the sprocket hole measured as true position of the pocket, not the pocket hole.

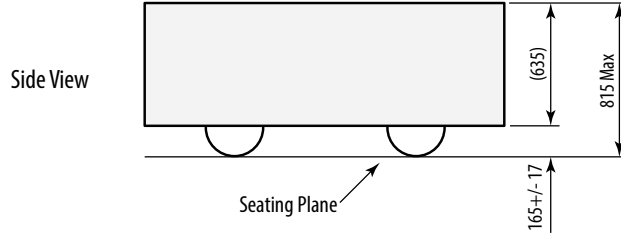
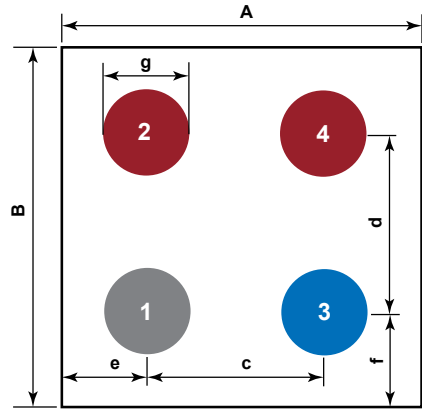
DIE MARKINGS



Part Number	Laser Markings	
	Part # Marking Line 1	Lot_Date Code Marking Line 2
EPC2038	AD	YYY

DIE OUTLINE

Solder Bump View



DIM	MIN	Nominal	MAX
A	870	900	930
B	870	900	930
c	450	450	450
d	450	450	450
e	210	225	240
f	210	225	240
g	187	208	229

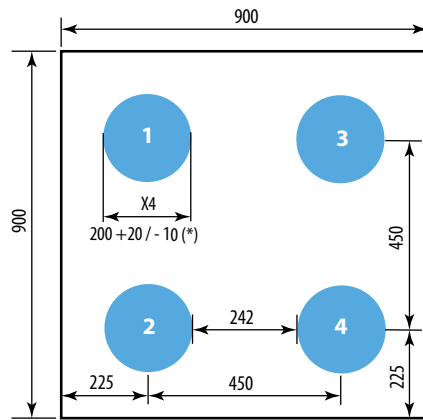
Pad 1 is Gate;

Pad 3 is Drain;

Pads 2, 4 are Source

RECOMMENDED LAND PATTERN

(measurements in μm)



* minimum 190

The land pattern is solder mask defined.

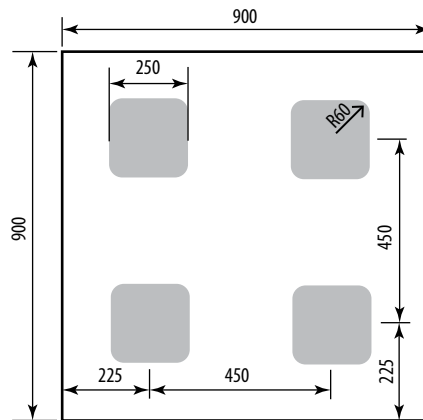
Pads 1 is Gate;

Pad 3 is Drain;

Pads 2, 4 are Source

RECOMMENDED STENCIL DRAWING

(measurements in μm)



Recommended stencil should be 4 mil (100 μm) thick, must be laser cut, openings per drawing.

Intended for use with SAC305 Type 4 solder, reference 88.5% metals content.

Additional assembly resources available at

<https://epc-co.com/epc/design-support/assemblybasics>

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