

P-Channel Power MOSFET

FEATURES

- Advance trench process technology
- High density cell design for ultra-low on-resistance
- RoHS compliant
- Halogen-free

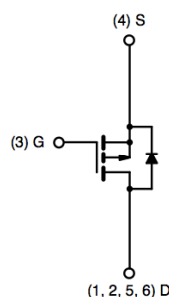
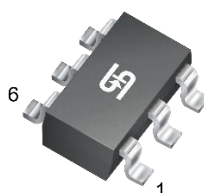
APPLICATIONS

- Power management
- Load switch

KEY PERFORMANCE PARAMETERS		
PARAMETER	VALUE	UNIT
V_{DS}	-30	V
$R_{DS(on)}$ (max)	$V_{GS} = -10V$	48
	$V_{GS} = -4.5V$	79
Q_g	24	nC



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Note: MSL 1 (Moisture Sensitivity Level) per J-STD-020

ABSOLUTE MAXIMUM RATINGS ($T_A = 25^\circ\text{C}$ unless otherwise noted)			
PARAMETER	SYMBOL	LIMIT	UNIT
Drain-Source Voltage	V_{DS}	-30	V
Gate-Source Voltage	V_{GS}	± 20	V
Continuous Drain Current	I_D	-4.6	A
Pulsed Drain Current (Note 1)	I_{DM}	-18.4	A
Total Power Dissipation	P_D	1.56	W
		1	
Operating Junction and Storage Temperature Range	T_J, T_{STG}	- 55 to +150	$^\circ\text{C}$

THERMAL PERFORMANCE			
PARAMETER	SYMBOL	LIMIT	UNIT
Junction to Ambient Thermal Resistance (Note 2)	$R_{\theta JA}$	80	$^\circ\text{C/W}$

Notes:

1. Pulse Width $\leq 100\mu\text{s}$.
2. Device on a PCB FR4 with 1 in² (single layer, 2 oz thickness) copper area for drain connection.

ELECTRICAL SPECIFICATIONS (T _A = 25°C unless otherwise noted)						
PARAMETER	CONDITIONS	SYMBOL	MIN	TYP	MAX	UNIT
Static (Note 3)						
Drain-Source Breakdown Voltage	V _{GS} = 0V, I _D = -250μA	BV _{DSS}	-30	--	--	V
Gate Threshold Voltage	V _{DS} = V _{GS} , I _D = -250μA	V _{GS(TH)}	-1	-1.5	-3	V
Gate Body Leakage	V _{GS} = ±20V, V _{DS} = 0V	I _{GSS}	--	--	±100	nA
Zero Gate Voltage Drain Current	V _{DS} = -24V, V _{GS} = 0V	I _{DSS}	--	--	-1	μA
Drain-Source On-State Resistance	V _{GS} = -10V, I _D = -4.6A	R _{DS(on)}	--	15	48	mΩ
	V _{GS} = -4.5V, I _D = -3.6A		--	21	79	
Forward Transconductance	V _{DS} = -10V, I _D = -1.2A	g _{fs}	--	7	--	S
Dynamic (Note 4)						
Total Gate Charge	V _{DS} = -15V, I _D = -4.6A, V _{GS} = -10V	Q _g	--	24	--	nC
Gate-Source Charge		Q _{gs}	--	3.3	--	
Gate-Drain Charge		Q _{gd}	--	5.2	--	
Input Capacitance	V _{DS} = -15V, V _{GS} = 0V, f = 1.0MHz	C _{iss}	--	1077	--	pF
Output Capacitance		C _{oss}	--	188	--	
Reverse Transfer Capacitance		C _{rss}	--	29	--	
Switching (Note 5)						
Turn-On Delay Time	V _{DD} = -15V, R _G = 6Ω, I _D = -4.6A, V _{GS} = -10V	t _{d(on)}	--	5.6	--	ns
Turn-On Rise Time		t _r	--	2.3	--	
Turn-Off Delay Time		t _{d(off)}	--	95	--	
Turn-Off Fall Time		t _f	--	48	--	
Source-Drain Diode						
Forward Voltage (Note 3)	I _S = -4.6A, V _{GS} = 0V	V _{SD}	--	-0.8	-1.2	V

Notes:

- Pulse test: Pulse Width $\leq 300\mu s$, duty cycle $\leq 2\%$.
- Defined by design. Not subject to production test.
- Switching time is essentially independent of operating temperature.

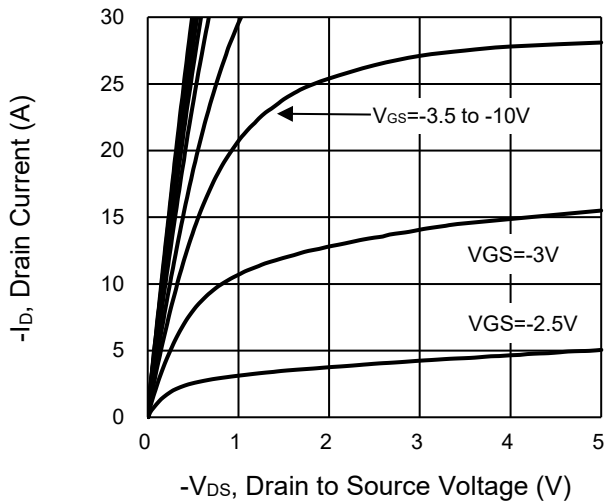
ORDERING INFORMATION

ORDERING CODE	PACKAGE	PACKING
TSM3481CX6 RFG	SOT-26	3kpcs / 7" Reel

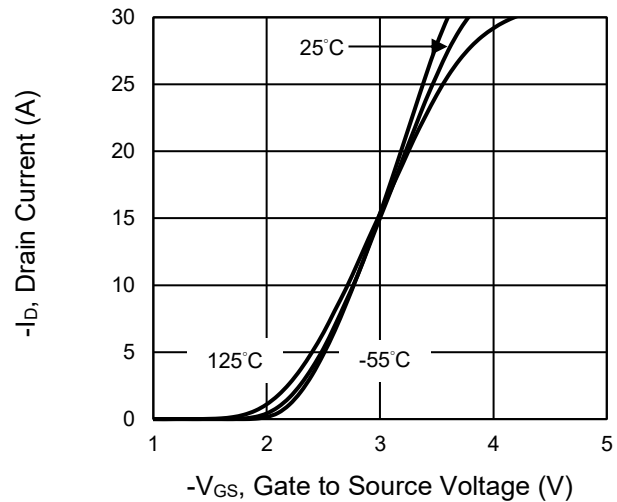
CHARACTERISTICS CURVES

($T_A = 25^\circ\text{C}$ unless otherwise noted)

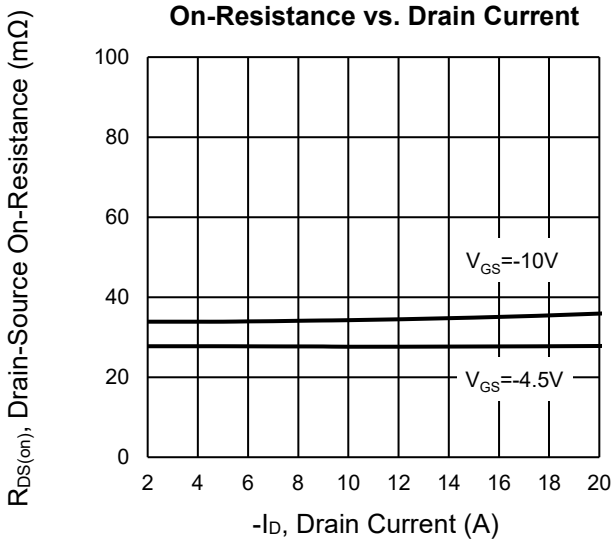
Output Characteristics



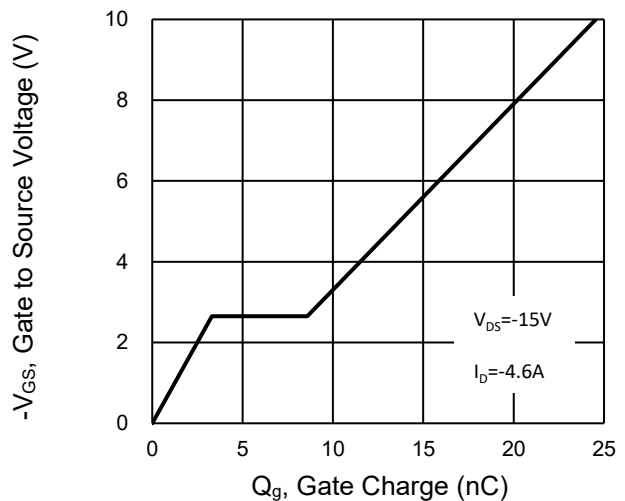
Transfer Characteristics



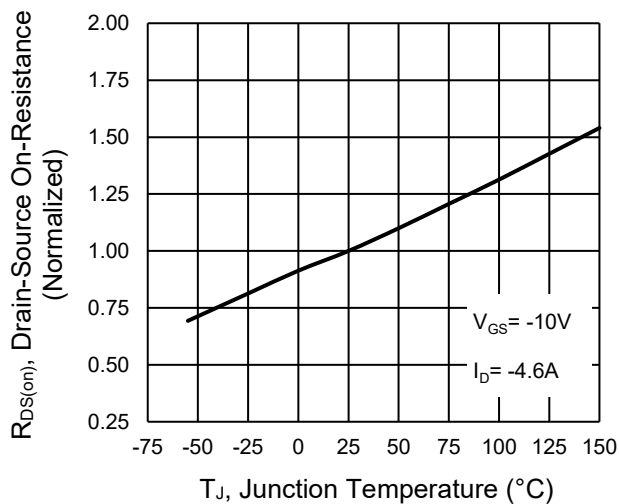
On-Resistance vs. Drain Current



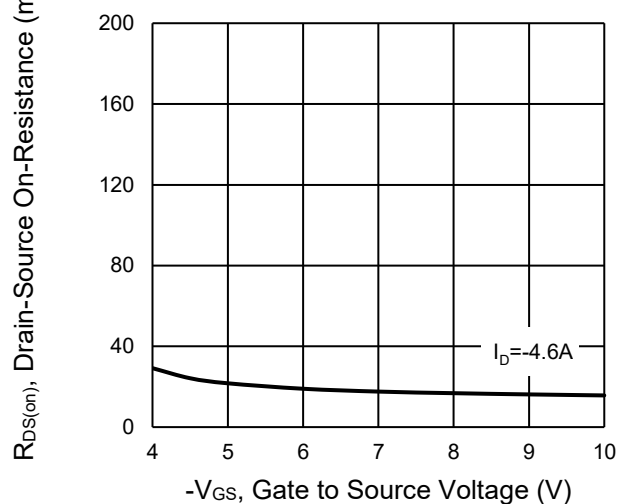
Gate-Source Voltage vs. Gate Charge



On-Resistance vs. Junction Temperature



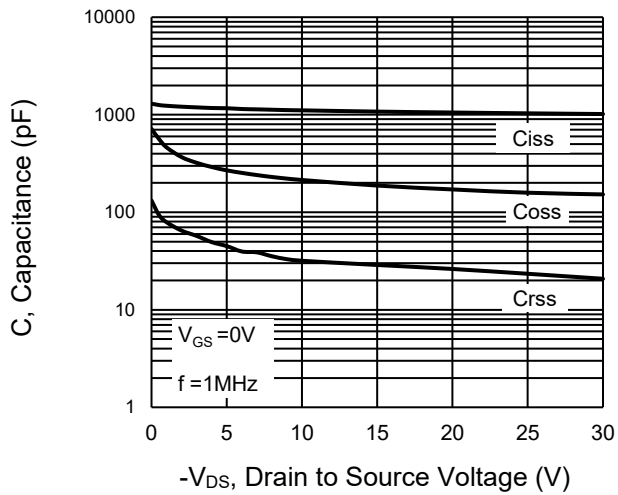
On-Resistance vs. Gate-Source Voltage



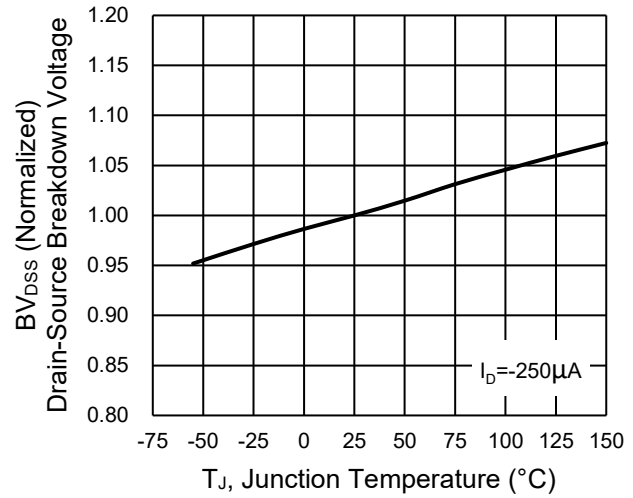
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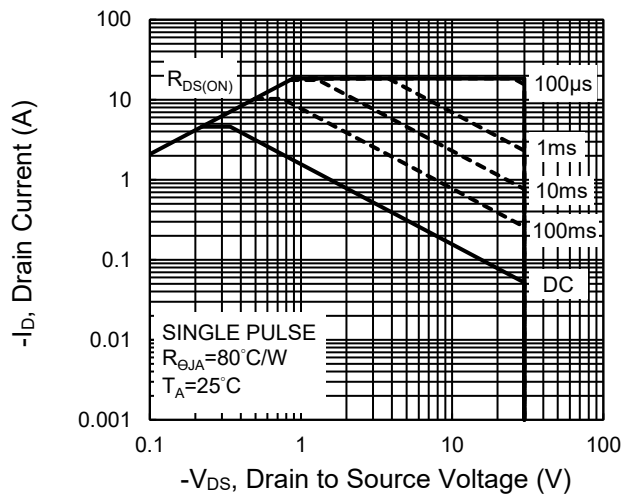
Capacitance vs. Drain-Source Voltage



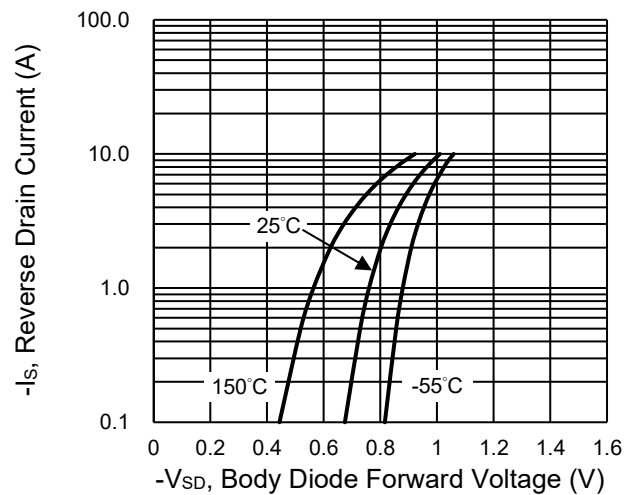
BV_{DSS} vs. Junction Temperature



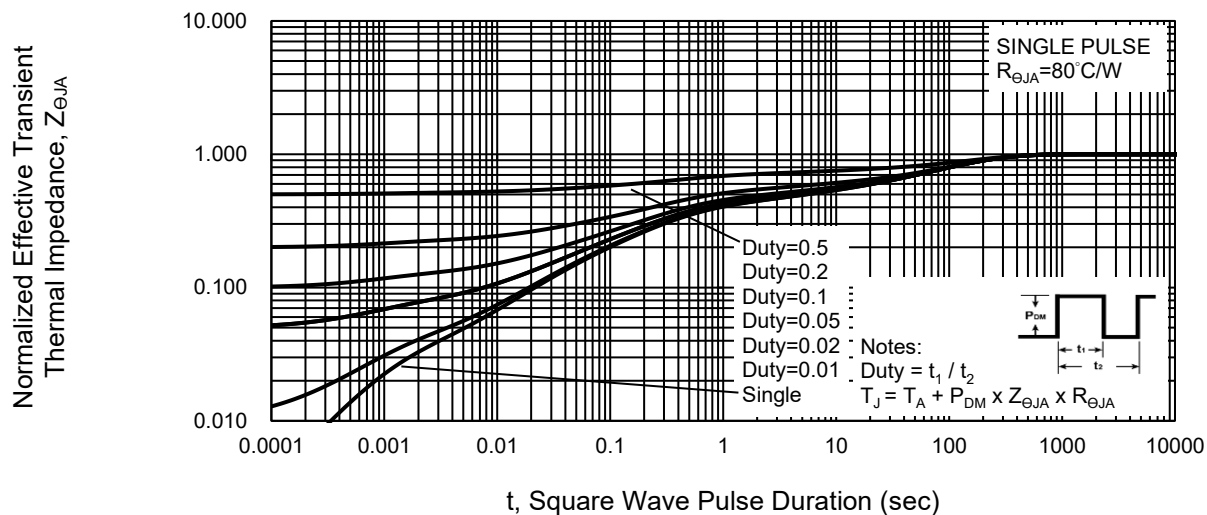
Maximum Safe Operating Area, Junction-to-Ambient



Source-Drain Diode Forward Current vs. Voltage

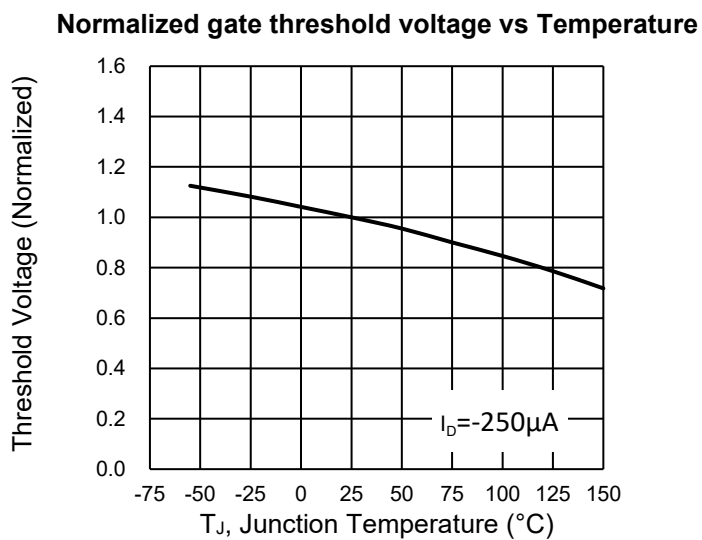
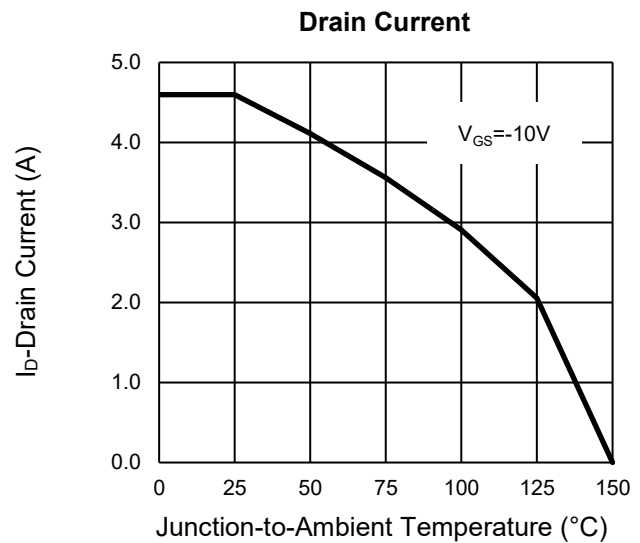
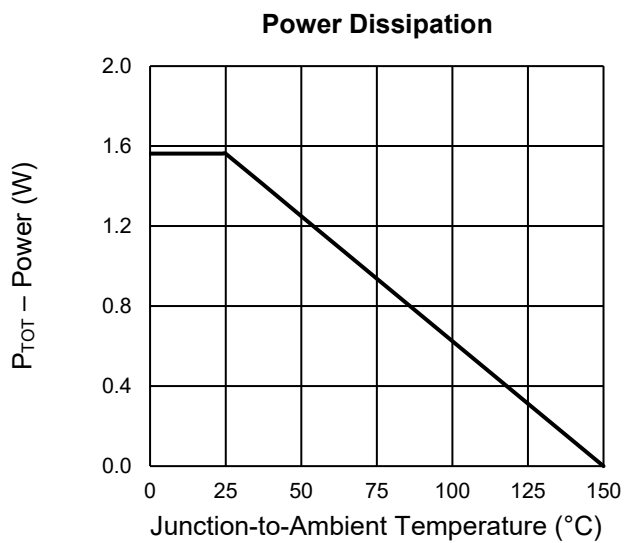


Normalized Thermal Transient Impedance, Junction-to-Ambient



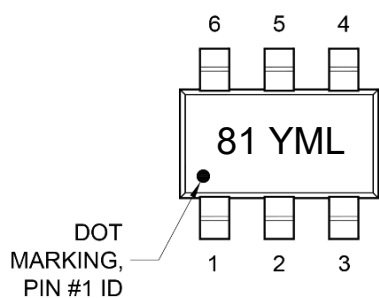
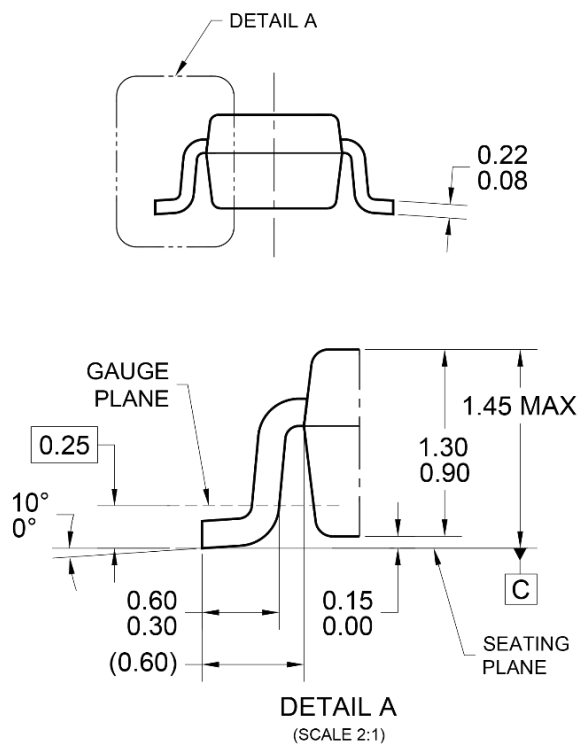
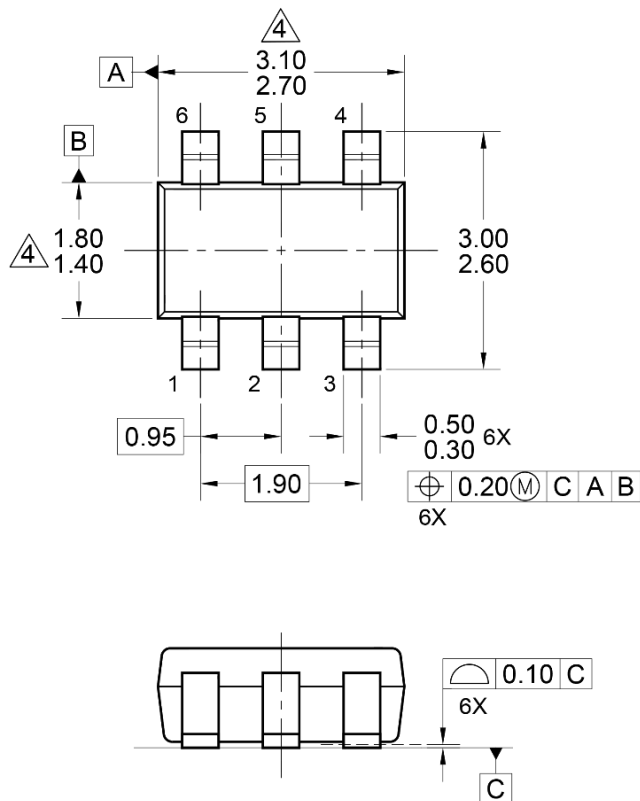
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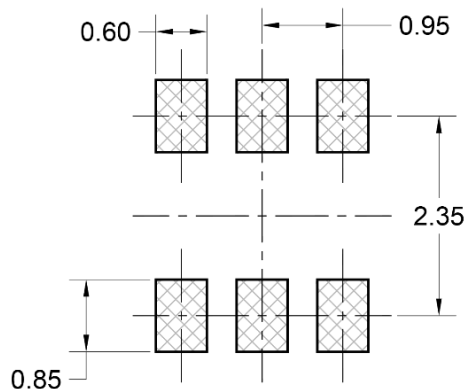
PACKAGE OUTLINE DIMENSIONS (Unit: Millimeters)

SOT-26



MARKING DIAGRAM

- 81 = Device marking
 Y = Year Code
 M = Month Code for Halogen Free Product
 (O=Jan, P=Feb, Q=Mar, R=Apr, S=May, T=Jun, U=Jul, V=Aug, W=Sep, X=Oct, Y=Nov, Z=Dec)
 L = Lot Code



SUGGESTED PAD LAYOUT

NOTES: UNLESS OTHERWISE SPECIFIED

- ALL DIMENSIONS ARE IN MILLIMETERS.
- DIMENSIONING AND TOLERANCING PER ASME Y14.5M-1994.
- PACKAGE OUTLINE REFERENCE: JEDEC MO-178, VARIATION AB.
- MOLDED PLASTIC BODY DIMENSIONS DO NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS.
- DWG NO. REF: HQ2SD07-SOT26-027 REV A.

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