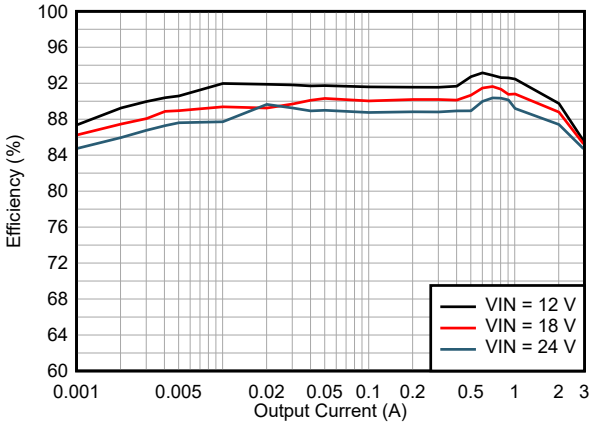
# LMQ664x0-Q1 36V, 1A, 2A, and 3A, Ultra-Small, Synchronous Automotive ZEN 2 Step-Down Converter With Integrated $V_{IN}$ Bypass and $C_{BOOT}$ Capacitors

## 1 Features

- Functional Safety-Capable
  - Documentation available to aid functional safety system design
- AEC-Q100-qualified for automotive applications:
  - Temperature grade 1: –40°C to +125°C, $T_A$
- ZEN 2 switcher
  - Facilitates CISPR 25 class 5 compliance
  - Integrated bypass and boot capacitors reduce EMI
  - Dual random spread spectrum reduces peak emissions
  - Enhanced HotRod™ QFN package minimizes switch node ringing
- Greater than 85% efficiency at 1mA
- Designed for automotive applications:
  - Junction temperature range: –40°C to +150°C
  - NC pin between critical pins for better reliability
  - Best in-class pin FMEA
  - Supports 42V automotive load dump transients
  - Supports 3$V_{IN}$ for automotive cold crank
- Miniature design size and low component cost:
  - Integrated input bypass capacitors and bootstrap capacitor reducing EMI
  - 2.6mm × 2.6mm enhanced HotRod QFN package with wettable flanks
  - Internal control loop compensation

## 2 Applications

- Advanced driver assistance systems: radar ECU
- Infotainment and cluster: head unit, eCall
- Body electronics and lighting




**Efficiency: $V_{OUT}$ = 3.3V (Fixed), 2.2MHz**

## 3 Description

The LMQ664x0-Q1 is the industry smallest 36V, 3A (available in 2A and 1A variants) synchronous step-down DC/DC converter with an integrated bypass and bootstrap capacitor in an enhanced HotRod QFN package. This easy-to-use converter supports a wide input voltage range of 2.7V to 36V (after start-up or after operating) with transients up to 42V.

The LMQ664x0-Q1 is specifically designed to meet low standby power requirements for always-on, automotive applications. Auto mode enables frequency foldback when operating at light loads, allowing an unloaded typical current consumption of 1.5µA at 13.5$V_{IN}$ and high light load efficiency. A seamless transition between PWM and PFM modes along with very low MOSFET ON resistances makes sure there is exceptional efficiency across the entire load range. The control architecture (peak current mode) and feature set are optimized for an ultra-small design size with minimal output capacitance. The device minimizes input filter size by using dual-random spread spectrum (DRSS), a low-EMI enhanced HotRod QFN package, and an optimized pinout. The MODE/SYNC pin can be used to set or synchronize the frequency to avoid noise sensitive frequency bands. There are NC pins between critical high voltage pins, reducing potential failures (excellent choice pin FMEA). ZEN 2 switcher features enable the device to support ultra low-EMI applications. The rich feature set of the LMQ664x0-Q1 is designed to simplify implementation for a wide range of automotive end equipment.

**Package Information**

| PART NUMBER | PACKAGE (1) | PACKAGE SIZE(2) |
|---|---|---|
| LMQ66430-Q1 | RXB (VQFN-FCRLF, 14) | 2.60mm × 2.60mm |
| LMQ66420-Q1 | | |
| LMQ66410-Q1 | | |

(1) For more information, see Section 11.
(2) The package size (length × width) is a nominal value and includes pins, where applicable.

**Device Information**

| PART NUMBER | RATED OUTPUT CURRENT (1) |
|---|---|
| LMQ66430-Q1 | 3A |
| LMQ66420-Q1 | 2A |
| LMQ66410-Q1 | 1A |

(1) See the *Device Comparison Table*.

An IMPORTANT NOTICE at the end of this data sheet addresses availability, warranty, changes, use in safety-critical applications, intellectual property matters and other important disclaimers. PRODUCTION DATA.

# Table of Contents

**1 Features**....1
**2 Applications**....1
**3 Description**....1
**4 Device Comparison Table**....3
**5 Pin Configuration and Functions**....4
**6 Specifications**....5
6.1 Absolute Maximum Ratings....5
6.2 ESD Ratings....5
6.3 Recommended Operating Conditions....5
6.4 Thermal Information....6
6.5 Electrical Characteristics....6
6.6 System Characteristics....8
6.7 Typical Characteristics....9
**7 Detailed Description**....10
7.1 Overview....10
7.2 Functional Block Diagram....11
7.3 Feature Description....12
7.4 Device Functional Modes....20
**8 Application and Implementation**....27
8.1 Application Information....27
8.2 Typical Application....28
8.3 Best Design Practices....41
8.4 Power Supply Recommendations....41
8.5 Layout....41
**9 Device and Documentation Support**....43
9.1 Device Support....43
9.2 Documentation Support....44
9.3 Receiving Notification of Documentation Updates....44
9.4 Support Resources....44
9.5 Trademarks....44
9.6 Electrostatic Discharge Caution....44
9.7 Glossary....44
**10 Revision History**....45
**11 Mechanical, Packaging, and Orderable Information**....46


Copyright © 2025 Texas Instruments Incorporated

# 4 Device Comparison Table

| Orderable Part Number (1) (2) | Output Current | Output Voltage | External Sync | $F_{SW}$ | Internal Capacitors | Spread Spectrum |
|---|---|---|---|---|---|---|
| LMQ66430MC3RXBRQ1 | 3 A | 3.3 V fixed / adjustable | Yes (PFM / FPWM Selectable) | Fixed 2.2 MHz | Yes | Yes |
| LMQ66430MC5RXBRQ1 | 3 A | 5 V fixed / adjustable | Yes (PFM / FPWM selectable) | Fixed 2.2 MHz | Yes | Yes |
| LMQ66430MA3RXBRQ1 | 3 A | 3.3 V fixed / adjustable | Yes (PFM / FPWM selectable) | Fixed 400 kHz | Yes | Yes |
| LMQ66430MA5RXBRQ1 | 3 A | 5 V fixed / adjustable | Yes (PFM / FPWM selectable) | Fixed 400 kHz | Yes | Yes |
| LMQ66420MC3RXBRQ1 | 2 A | 3.3 V fixed / adjustable | Yes (PFM / FPWM selectable) | Fixed 2.2 MHz | Yes | Yes |
| LMQ66420MC5RXBRQ1 | 2 A | 5 V fixed / adjustable | Yes (PFM / FPWM selectable) | Fixed 2.2 MHz | Yes | Yes |
| LMQ66420MA3RXBRQ1 | 2 A | 3.3 V fixed / adjustable | Yes (PFM / FPWM selectable) | Fixed 400 kHz | Yes | Yes |
| LMQ66420MA5RXBRQ1 | 2 A | 5 V fixed / adjustable | Yes (PFM / FPWM selectable) | Fixed 400 kHz | Yes | Yes |
| LMQ66410MC3RXBRQ1 | 1 A | 3.3 V fixed / adjustable | Yes (PFM / FPWM selectable) | Fixed 2.2 MHz | Yes | Yes |
| LMQ66410MC5RXBRQ1 | 1 A | 5 V fixed / adjustable | Yes (PFM / FPWM selectable) | Fixed 2.2 MHz | Yes | Yes |
| LMQ66410MA3RXBRQ1 | 1 A | 3.3 V fixed / adjustable | Yes (PFM / FPWM selectable) | Fixed 400 kHz | Yes | Yes |
| LMQ66410MA5RXBRQ1 | 1 A | 5 V fixed / adjustable | Yes (PFM / FPWM selectable) | Fixed 400 kHz | Yes | Yes |

(1) For more information on device orderable part numbers, see *Device Nomenclature*.
(2) For other variant options, please contact TI.

Copyright © 2025 Texas Instruments Incorporated

# 5 Pin Configuration and Functions

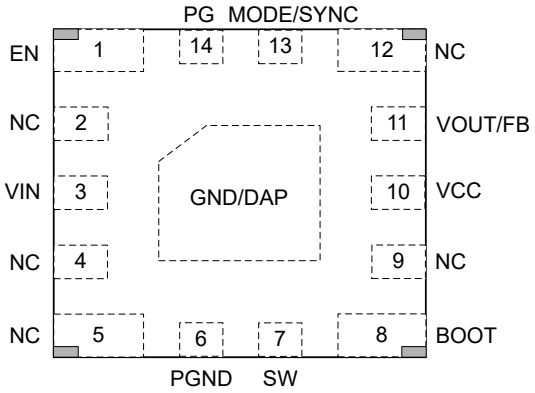



**Figure 5-1. RXB 14-Pin (2.6mm × 2.6mm) Enhanced HotRod™ VQFN-FCRLF Package (Top View)**

**Table 5-1. Pin Functions**

| PIN | | TYPE | DESCRIPTION |
|---|---|---|---|
| NAME | NO. | | |
| EN/UVLO | 1 | A | Enable input to regulator. High = ON, low = OFF. Can be connected directly to VIN. *Do not float this pin.* |
| NC | 2 | — | No internal connection to device |
| VIN | 3 | P | Input supply to regulator. Two 22-nF capacitors are connected in series internally from this pin to the PGND pin. Additional high-quality bypass capacitor or capacitors can be added directly to this pin and PGND. |
| NC | 4 | — | Middle point of the two internal series bypass capacitors. *Leave this pin floating.* |
| NC | 5 | — | Middle point of the two internal series bypass capacitors. *Leave this pin floating.* |
| PGND | 6 | G | Power ground terminal. Connect to system ground. Connect to $C_{IN}$ with short, wide traces. |
| SW | 7 | P | Regulator switch node. Connect to the power inductor. |
| BOOT | 8 | P | Bootstrap supply voltage for internal high-side driver. A 0.1-µF capacitor is internally connected from this pin to the SW pin. |
| NC | 9 | — | No internal connection to device |
| VCC | 10 | A | Internal LDO output. Used as supply to internal control circuits. Do not connect to external loads. Can be used as logic supply for power-good flag. Connect a high-quality 1-µF capacitor from this pin to GND. |
| VOUT/FB | 11 | A | Fixed output options and adjustable output options are available with the VOUT/FB pin variant. Connect to the output voltage node for fixed $V_{OUT}$. See *$V_{OUT}$ / FB for Adjustable Output* for how to select feedback resistor divider values. See *Device Comparison Table* for more details. The FB function can be used to adjust the output voltage. Connect to tap point of feedback voltage divider. *Do not float this pin.* |
| NC | 12 | — | No internal connection to device |
| MODE/SYNC | 13 | A | This pin allows the user to select between PFM/FPWM mode or to synchronize to an external clock. See *MODE/SYNC variant* for more details. *Do not float this pin.* |
| PG | 14 | A | Open-drain power-good flag output. Connect to suitable voltage supply through a current limiting resistor. High = power OK, low = power bad. This pin goes low when EN = low. This pin can be open or grounded when not used. |
| GND/DAP | — | G | Thermal pad of the package. Must be soldered to achieve appropriate dissipation. Must be connected to GND. |
| A = Analog, P = Power, G = Ground | | | |


Copyright © 2025 Texas Instruments Incorporated

# 6 Specifications

## 6.1 Absolute Maximum Ratings

Over the recommended operating junction temperature range (1)

| PARAMETER | | MIN | MAX | UNIT |
|---|---|---|---|---|
| Voltages | VIN to GND | –0.3 | 42 | V |
| Voltages | SW to GND | –0.3 | $V_{IN}$ + 0.3 | V |
| Voltages | BOOT to SW | –0.3 | 5.5 | V |
| Voltages | VCC to GND | –0.3 | 5.5 | V |
| Voltages | VOUT/FB to GND | –0.3 | 16 | V |
| Voltages | SYNC/MODE or RT to GND | –0.3 | 5.5 | V |
| Voltages | PG to GND | –0.3 | 20 | V |
| Voltages | EN to GND | –0.3 | 42 | V |
| Temperature | $T_J$, Junction temperature | –40 | 150 | °C |
| Temperature | $T_{stg}$, Storage temperature | –65 | 150 | °C |

(1) Operation outside the Absolute Maximum Ratings may cause permanent device damage. Absolute Maximum Ratings do not imply functional operation of the device at these or any other conditions beyond those listed under Recommended Operating Conditions. If used outside the Recommended Operating Conditions but within the Absolute Maximum Ratings, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.

## 6.2 ESD Ratings

| | | | VALUE | UNIT |
|---|---|---|---|---|
| $V_{(ESD)}$ | Electrostatic discharge | Human-body model (HBM), per AEC Q100-002, HBD ESD Classification Level 2 (1) | ±2000 | V |
| | | Charged-device model (CDM), per AEC Q100-011 CDM ESD clasiffication Level C4B | ±750 | V |

(1) AEC Q100-002 indicates that HBM stressing must be in accordance with the ANSI/ESDA/JEDEC JS-001 specification

## 6.3 Recommended Operating Conditions

Over the recommended operating junction temperature range of –40°C to 150°C (unless otherwise noted)

| | | MIN | MAX | UNIT |
|---|---|---|---|---|
| $V_{IN}$ | Input voltage range for start-up | 3.6 | 36 | V |
| | Input voltage range after start-up | 3.0 | 36 | V |
| $V_{OUT}$ | Output voltage range with adjustable output voltage setup | 1 | 18 | V |
| $I_{OUT}$ | LMQ66430-Q1 continuous DC output current range | 0 | 3 | A |
| $I_{OUT}$ | LMQ66420-Q1 continuous DC output current range | 0 | 2 | A |
| $I_{OUT}$ | LMQ66410-Q1 continuous DC output current range | 0 | 1 | A |
| $T_J$ | Operating junction temperature | –40 | 150 | °C |

Copyright © 2025 Texas Instruments Incorporated

## 6.4 Thermal Information

The value of $R_{\theta JA}$ in this table is only valid for comparison with other packages. These values were calculated in accordance with JESD 51-7, and simulated on a 4-layer JEDEC board. They do not represent the performance obtained in an actual application. For example, a 4-layer PCB can achieve a $R_{\theta JA}$= 50°C/W.

| THERMAL METRIC (1) | | LMQ664x0-Q1 VQFN 14 PINS | UNIT |
|---|---|---|---|
| $R_{\theta JA}$ | Junction-to-ambient thermal resistance for LMQ66430-2EVM | 45 | °C/W |
| $R_{\theta JA}$ | Junction-to-ambient thermal resistance | 66.1 | °C/W |
| $R_{\theta JC(top)}$ | Junction-to-case (top) thermal resistance | 53.6 | °C/W |
| $R_{\theta JB}$ | Junction-to-board thermal resistance | 26.2 | °C/W |
| $\psi_{JT}$ | Junction-to-top characterization parameter | 3.3 | °C/W |
| $\psi_{JB}$ | Junction-to-board characterization parameter | 25.9 | °C/W |

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application note.

## 6.5 Electrical Characteristics

Limits apply over the recommended operating junction temperature range of –40°C to +150°C, unless otherwise noted. Minimum and Maximum limits are specified through test, design or statistical correlation. Typical values represent the most likely parametric norm at $T_J$ = 25°C, and are provided for reference purposes only. Unless otherwise stated the following conditions apply: VIN = 13.5V, VOUT = 3.3V.

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| **SUPPLY VOLTAGE (VIN PIN)** | | | | | | |
| $V_{INMIN}$ | Input voltage rising threshold for start-up | Before start-up | 3.2 | 3.35 | 3.5 | V |
| | Input voltage falling threshold | Once operating | 2.45 | 2.7 | 3 | V |
| $I_{SD(VIN)}$ | Shutdown quiescent current at VIN pin | EN = 0V | | 0.25 | 1 | µA |
| $I_{BIAS}$ | Non-switching input current at VOUT/FB | Fixed 5.0V Vout, $V_{VOUT/FB}$ = 5.25V | | 4.2 | 6.5 | µA |
| $I_{BIAS}$ | Non-switching input current at VOUT/FB | Fixed 3.3Vout, $V_{VOUT/FB}$ = 3.47V | | 4.2 | 6.5 | µA |
| $I_{QVIN(nonsw)}$ | Non-switching input current; measured at VIN pin (1) | Fixed 5-V $V_{OUT}$, $V_{VOUT/FB}$ = 5.25 V | | 1.6 | 3 | µA |
| $I_{QVIN(nonsw)}$ | Non-switching input current; measured at VIN pin (1) | Fixed 3.3V $V_{OUT}$, $V_{VOUT/FB}$ = 3.47V | | 1.2 | 2.2 | µA |
| **ENABLE (EN PIN)** | | | | | | |
| $V_{EN-WAKE}$ | EN wakeup threshold | | 0.5 | 0.7 | 1 | V |
| $V_{EN-VOUT}$ | Precision enable rising threshold for $V_{OUT}$ | | 1.16 | 1.23 | 1.3 | V |
| $V_{EN-HYST}$ | Enable hysteresis below $V_{EN-VOUT}$ | | 0.3 | 0.35 | 0.4 | V |
| $I_{LKG-EN}$ | Enable pin input leakage current | $V_{EN}$ = $V_{IN}$ = 13.5V | | 10 | | nA |
| **INTERNAL LDO (VCC PIN)** | | | | | | |
| $V_{CC}$ | VCC pin output voltage | $V_{FB}$ = 0V, $I_{VCC}$ = 1mA | 3.1 | 3.3 | 3.45 | V |
| **VOLTAGE FEEDBACK (VOUT/FB PIN)** | | | | | | |
| $V_{OUT}$ | Output voltage accuracy for fixed $V_{OUT}$ | 3.3V $V_{OUT}$, $V_{IN}$ = 3.6V to 36V, FPWM mode | 3.27 | 3.3 | 3.32 | V |
| | | 5V $V_{OUT}$, $V_{IN}$ = 5.5V to 36V, FPWM mode | 4.94 | 5.00 | 5.06 | V |
| $V_{FB}$ | Internal reference voltage accuracy | $V_{OUT}$ = 1V, $V_{IN}$ = 3.0V to 36V, FPWM mode | 0.99 | 1.00 | 1.01 | V |
| $I_{FB(LKG)}$ | FB input current | Adjustable configuration, FB = 1V | | 10 | | nA |
| **CURRENT LIMITS** | | | | | | |
| $I_{PEAKMAX}$ | High-side peak current limit | LMQ66430-Q1 | 3.9 | 4.4 | 5 | A |
| $I_{VALMAX}$ | Low-side valley current limit | LMQ66430-Q1 | 2.9 | 3.5 | 4 | A |
| $I_{PEAKMIN}$ | Minimum peak current limit | LMQ66430-Q1, Auto mode | 0.55 | 0.69 | 0.86 | A |
| $I_{NEGMIN}$ | Low-side valley current negative limit | LMQ66430-Q1, FPWM mode | -1.5 | -1.3 | -1 | A |


Copyright © 2025 Texas Instruments Incorporated

## 6.5 Electrical Characteristics (continued)

Limits apply over the recommended operating junction temperature range of –40°C to +150°C, unless otherwise noted. Minimum and Maximum limits are specified through test, design or statistical correlation. Typical values represent the most likely parametric norm at $T_J$ = 25°C, and are provided for reference purposes only. Unless otherwise stated the following conditions apply: VIN = 13.5V, VOUT = 3.3V.

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| $I_{PEAKMAX}$ | High-side peak current limit | LMQ66420-Q1 | 2.8 | 3.4 | 3.9 | A |
| $I_{VALMAX}$ | Low-side valley current limit | LMQ66420-Q1 | 1.9 | 2.2 | 2.53 | A |
| $I_{PEAKMIN}$ | Minimum peak current limit | LMQ66420-Q1, Auto mode | 0.37 | 0.5 | 0.65 | A |
| $I_{NEGMIN}$ | Negative current limit | LMQ66420-Q1, FPWM mode | -1 | -0.8 | -0.6 | A |
| $I_{PEAKMAX}$ | High-side peak current limit | LMQ66410-Q1 | 1.4 | 1.8 | 2.1 | A |
| $I_{VALMAX}$ | Low-side valley current limit | LMQ66410-Q1 | 0.9 | 1.1 | 1.4 | A |
| $I_{PEAKMIN}$ | Minimum peak current limit | LMQ66410-Q1, Auto mode | 0.17 | 0.27 | 0.35 | A |
| $I_{NEGMIN}$ | Low-side valley current negative limit | LMQ66410-Q1, FPWM mode | -1 | -0.8 | -0.6 | A |
| $I_{ZC}$ | Zero-cross current limit | Auto mode | 30 | 80 | 135 | mA |
| **POWER GOOD (PG PIN)** | | | | | | |
| $PG_{OV}$ | PG upper threshold - rising | % of VOUT/FB (Fixed or Adj. output) | 104 | 108 | 111 | % |
| $PG_{UV}$ | PG upper threshold - falling | % of VOUT/FB (Fixed or Adj. output) | 89 | 91 | 94.2 | % |
| $PG_{HYST}$ | PG recovery hysteresis for OV | % of VOUT/FB target regulation voltage | 2 | 2.4 | 2.8 | % |
| | PG recovery hysteresis for UV | % of VOUT/FB target regulation voltage | 2 | 3.3 | 4.6 | % |
| $V_{PG-VAL}$ | Minimum $V_{IN}$ for PG function | $V_{EN}$ = 0V, $R_{PG_PU}$ = 10kΩ | | | 1.5 | V |
| $R_{PG}$ | PG ON resistance | $V_{EN}$ = 3.3V, 200µA pullup current | | | 100 | Ω |
| $R_{PG}$ | PG ON resistance | $V_{EN}$ = 0V, 200µA pullup current | | | 100 | Ω |
| $t_{RESET_FILTER}$ | PG deglitch delay at falling edge | | 25 | 40 | 75 | µs |
| $t_{PG_ACT}$ | Delay time to PG high signal | | 1.35 | 2.5 | 4 | ms |
| **SOFT START** | | | | | | |
| $t_{SS}$ | Time from first SW pulse to VOUT/FB at 90% of set point | | 2 | 3.5 | 4.6 | ms |
| $t_{HICCUP}$ | Time in hiccup before retry soft start | | 30 | 50 | 75 | ms |
| **OSCILLATOR (SYNC/MODE PIN)** | | | | | | |
| $t_{PULSE_H}$ | High duration needed to be recognized as a pulse | | 100 | | | ns |
| $t_{PULSE_L}$ | Low duration needed to be recognized as a pulse | | 100 | | | ns |
| $t_{SYNC}$ | High/Low level pulse maximum duration to be recognized as a valid clock signal | | | | 6 | µs |
| $t_{MODE}$ | Time at one level needed to indicate FPWM or Auto Mode | | 12.5 | | | µs |
| $F_{SW(400kHz)}$ | Switching Frequency with fixed 400kHz | | 340 | 400 | 460 | kHz |
| $F_{SW(2.2MHz)}$ | Switching Frequency with fixed 2.2MHz | | 2100 | 2200 | 2300 | kHz |
| $f_{SYNC}$ | Frequency SYNC range | | 0.2 | | 2.5 | MHz |
| $V_{MODE_L}$ | SYNC/MODE input voltage low level threshold | | | | 1 | V |
| $V_{MODE_H}$ | SYNC/MODE input voltage high level threshold | | 1.6 | | | V |
| **SWITCH NODE** | | | | | | |
| $t_{ON-MIN}$ | Minimum HS switch on-time | FPWM mode $I_{OUT}$ = 1A, 2.2MHz fixed | | 65 | 75 | ns |
| $t_{OFF-MIN}$ | Minimum HS switch off-time | | | 60 | 85 | ns |
| $t_{ON-MAX}$ | Maximum HS switch on-time | HS timeout in dropout | 6 | 9 | 13 | µs |
| **POWER STAGE** | | | | | | |

Copyright © 2025 Texas Instruments Incorporated

## 6.5 Electrical Characteristics (continued)

Limits apply over the recommended operating junction temperature range of –40°C to +150°C, unless otherwise noted. Minimum and Maximum limits are specified through test, design or statistical correlation. Typical values represent the most likely parametric norm at $T_J$ = 25°C, and are provided for reference purposes only. Unless otherwise stated the following conditions apply: VIN = 13.5V, VOUT = 3.3V.

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| $V_{BOOT_UVLO}$ | Voltage on BOOT pin compared to SW which will turnoff high-side switch | | | 2.1 | | V |
| $R_{DSON-HS}$ | High-side MOSFET on-resistance | Load = 1A | | 132 | 260 | mΩ |
| $R_{DSON-LS}$ | Low-side MOSFET on-resistance | Load = 1A | | 75 | 140 | mΩ |

(1) This is the current used by the device open loop. It does not represent the total input current of the system when in regulation.

## 6.6 System Characteristics

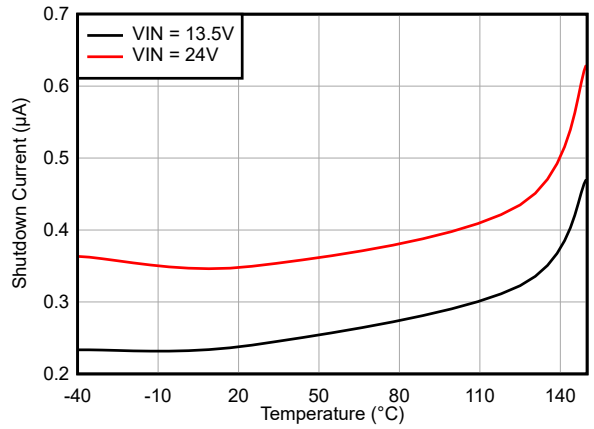
The following specifications apply only to the typical applications circuit, with nominal component values. Specifications in the typical (TYP) column apply to $T_J$ = 25°C only. Specifications in the minimum (MIN) and maximum (MAX) columns apply to the case of typical components over the temperature range of $T_J$ = –40°C to 150°C. These specifications are not ensured by production testing.

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| **SUPPLY CURRENT** | | | | | | |
| $I_{QVIN}$ | Input current to $V_{IN}$ | $V_{IN}$ = 13.5V, Fixed 3.3V $V_{OUT}$, $I_{OUT}$ = 0A, Auto mode | | 1.5 | | µA |
| | | $V_{IN}$ = 13.5V, Fixed 5V $V_{OUT}$, $I_{OUT}$ = 0A, Auto mode | | 2 | | µA |
| **POWER STAGE** | | | | | | |
| $V_{DROP1}$ | Input to output voltage differential to maintain $V_{OUT}$ regulation ≥ 95%, with frequency foldback | $V_{OUT}$ = 3.3V, fixed 2.2MHz, $I_{OUT}$ = 1A | | 0.2 | | V |
| | | $V_{OUT}$ = 5V, fixed 2.2MHz, $I_{OUT}$ = 1A | | 0.2 | | V |
| $V_{DROP2}$ | Input to output voltage differential to maintain $V_{OUT}$ regulation ≥ 95% and $F_{SW}$ ≥1.85MHz | $V_{OUT}$ = 3.3V, fixed 2.2MHz, $I_{OUT}$ = 1A | | 0.7 | | V |
| | Input to output voltage differential to maintain $V_{OUT}$ regulation ≥ 95% and $F_{SW}$ ≥ 1.85MHz | $V_{OUT}$ = 5V, fixed 2.2MHz trim, $I_{OUT}$ = 1A | | 0.9 | | V |
| $D_{MAX}$ | Maximum switch duty cycle | While in frequency fold-back | | 98 | | % |
| | | $F_{SW}$ = 1.85MHz, $V_{OUT}$ = 5.0V, $I_{OUT}$ = 1A | | 87 | | % |
| $R_{FBPARA(min)}$ | Minimum value of parallel FB resistor : RFBT parallel RFBB | | | 5 | | KΩ |
| **PROTECTION** | | | | | | |
| $T_{SD(trip)}$ | Thermal shutdown threshold | Temperature rising | 158 | 168 | 186 | °C |
| $T_{SD(hyst)}$ | Thermal shutdown hysteresis | | | 15 | 20 | °C |


Copyright © 2025 Texas Instruments Incorporated

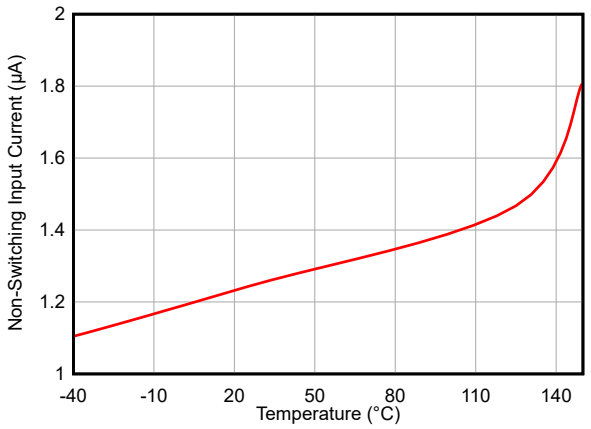
## 6.7 Typical Characteristics

Unless otherwise specified, the following conditions apply: $T_A$ = 25°C, $V_{IN}$ = 13.5 V



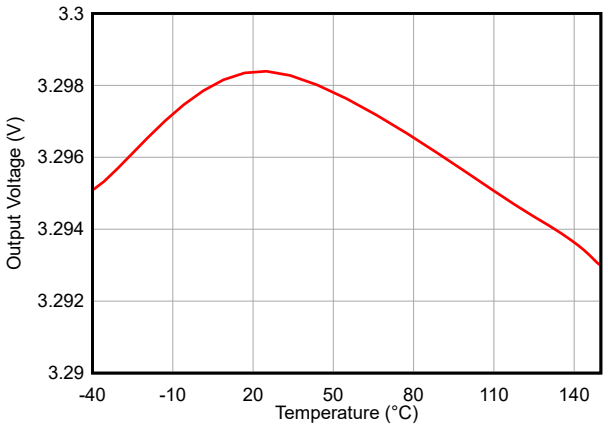

$V_{OUT}$ = 3.3-V fixed

**Figure 6-1. Shutdown Current Versus Temperature**



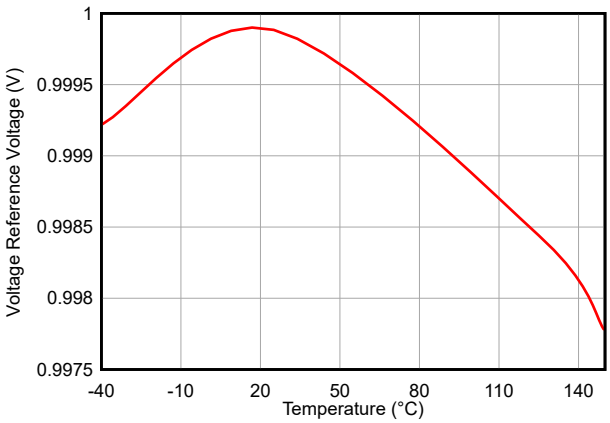

$V_{OUT}$ = 3.3-V fixed

**Figure 6-2. Non-Switching Input Current ($I_{QVIN(nonsw)}$) Versus Temperature**




$V_{OUT}$ = 3.3-V fixed

**Figure 6-3. Output Voltage Accuracy Versus Temperature**




$V_{OUT}$ = adjustable

**Figure 6-4. Feedback Voltage Accuracy Versus Temperature**

# 7 Detailed Description

## 7.1 Overview

The LMQ664x0-Q1 is a wide input, low-quiescent current, high-performance regulator that can operate over a wide range of duty ratio and the switching frequencies, including sub-AM band at 400 kHz and above AM band at 2.2 MHz. During wide input transients, if the minimum on time or the minimum off time cannot support the desired duty ratio at the higher switching frequency settings, the switching frequency is reduced automatically, allowing the device to maintain the output voltage regulation. With an internally compensated design optimized for minimal output capacitors, the system design process with the device is simplified significantly compared to other buck regulators available in the market.

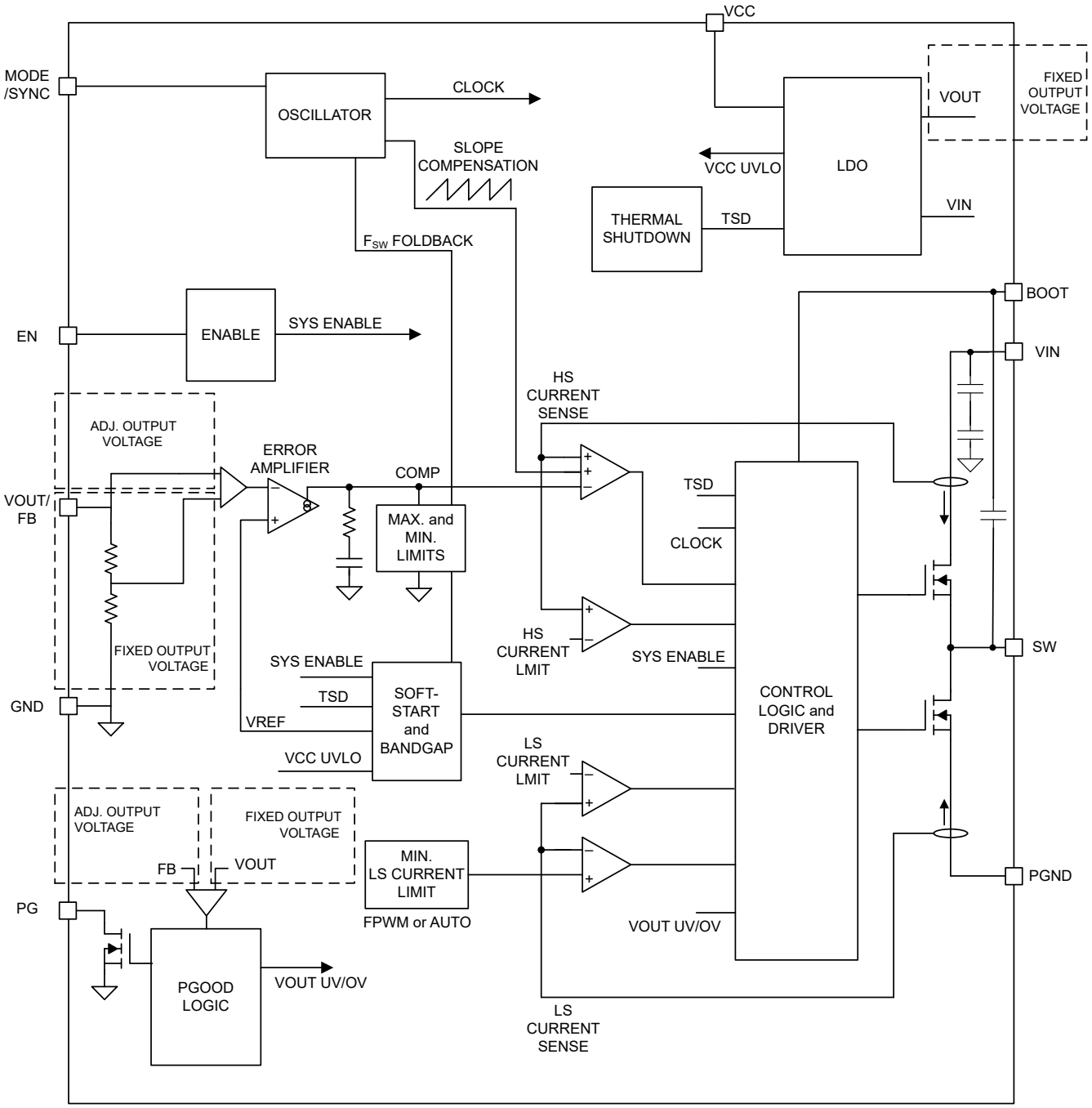
The device is designed to minimize external component cost and design size while operating in all demanding automotive environments. To further reduce system cost, the PG output feature with built-in delayed release allows the elimination of the reset supervisor in many applications.

The LMQ664x0-Q1 family is designed to reduce EMI/EMC emissions by introducing a dual random spread spectrum (DRSS) switching frequency dithering scheme, using the enhanced HotRod QFN package where no bond wires are used. and integrates the high-frequency VIN bypass capacitors including, a CBOOT capacitor, inside the package. Also, available is the MODE/SYNC feature that allows synchronization to an external clock. Together, these features reduce the need for any common-mode choke or shielding or any elaborate input filter design scheme, greatly reducing the complexity and cost of the EMI/EMC mitigation measures.

The device comes in an ultra-small, 2.6-mm × 2.6-mm, enhanced, HotRod QFN package with wettable flanks, allowing for quick optical inspection along with specially designed corner anchor pins for reliable board level solder connections.


Copyright © 2025 Texas Instruments Incorporated

## 7.2 Functional Block Diagram



## 7.3 Feature Description

### 7.3.1 Enable, Start-Up, and Shutdown

Voltage at the EN pin controls the start-up or remote shutdown of the LMQ664x0-Q1 family of devices. The part stays shut down as long as the EN pin voltage is less than $V_{EN-WAKE}$ = 0.7 V (typical). During the shutdown, the input current drawn by the device typically drops down to 0.25 µA ($V_{IN}$ = 13.5 V). With the voltage at the EN pin greater than $V_{EN-WAKE}$, the device enters device standby mode and the internal LDO powers up to generate VCC. As the EN voltage increases further, approaching $V_{EN-VOUT}$, the device finally starts to switch, entering start-up mode with a soft start. During the device shutdown process, when the EN input voltage measures less than ($V_{EN-VOUT}$–$V_{EN-HYST}$), the regulator stops switching and re-enters device standby mode. Any further decrease in the EN pin voltage, below $V_{EN-WAKE}$, and the device is then firmly shut down. The high-voltage compliant EN input pin can be connected directly to the $V_{IN}$ input pin if remote precision control is not needed. The EN input pin must not be allowed to float. The various EN threshold parameters and the values are listed in the *Electrical Characteristics*. Figure 7-2 shows the precision enable behavior and Figure 7-3 shows a typical remote EN start-up waveform in an application. After EN goes high, after a delay of about 2.5 ms, the output voltage begins to rise with a soft start and reaches close to the final value in about 3.5 ms ($t_{ss}$). After a delay of about 2.5 ms ($t_{PG_ACT}$), the PG flag goes high. During start-up, the device is not allowed to enter FPWM mode until the soft-start time has elapsed. This time is measured from the rising edge of EN. Check *External UVLO* for component selection.

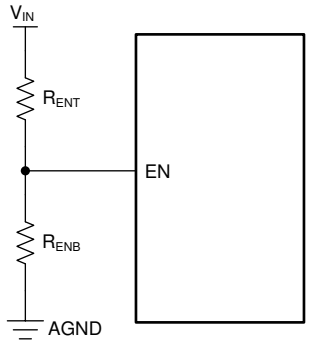



**Figure 7-1. VIN UVLO Using the EN Pin**


Copyright © 2025 Texas Instruments Incorporated

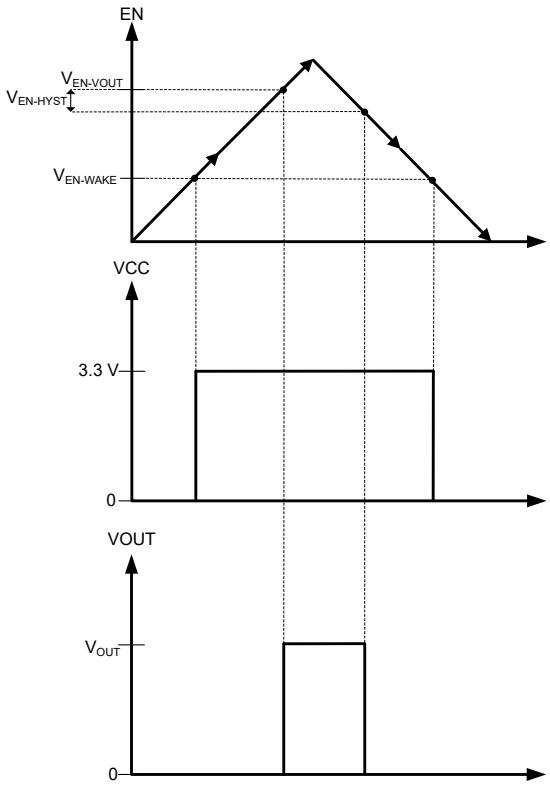



**Figure 7-2. Precision Enable Behavior**

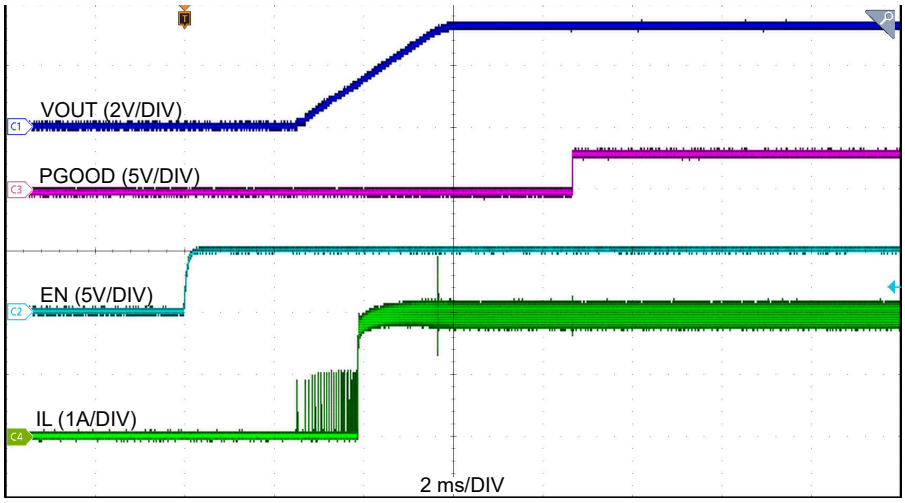



**Figure 7-3. Enable Start-Up $V_{IN}$ = 24 V, $V_{OUT}$ = 3.3 V, $I_{OUT}$ = 2 A**

### *7.3.2 External CLK SYNC (With MODE/SYNC)*

Synchronized operation of multiple regulators in a single system is often desirable for a well-defined system level performance. The select variants in the device with the MODE/SYNC pin allow the power designer to synchronize the device to a common external clock. The device implements an in-phase locking scheme, where the rising edge of the clock signal, provided to the MODE/SYNC pin of the device, corresponds to the turning on of the high-side device. The external clock synchronization is implemented using a phase locked loop (PLL), eliminating any large glitches. The external clock fed into the device replaces the internal free-running clock, but does not affect any frequency foldback operation. Output voltage continues to be well regulated. The device

Copyright © 2025 Texas Instruments Incorporated

remains in FPWM mode and operates in CCM for light loads when synchronization input is provided. The range of frequencies permitted by the device is given by $f_{SYNC}$ and is provided in the *Electrical Characteristics*.

The MODE/SYNC input pin in the device can operate in one of three selectable modes:

- Auto mode: Pulse frequency modulation (PFM) operation is enabled during light load and diode emulation prevents reverse current through the inductor. See Section 7.4.3.2 for more details.
- FPWM mode: In FPWM mode, diode emulation is disabled, allowing current to flow backwards through the inductor. This action allows operation at full frequency even without load current. See Section 7.4.3.3 for more details.
- SYNC mode: The internal clock locks to an external signal applied to the MODE/SYNC pin. As long as output voltage can be regulated at full frequency and is not limited by minimum off time or minimum on time, clock frequency is matched to the frequency of the signal applied to the MODE/SYNC pin. While the device is in SYNC mode, the device operates as though in FPWM mode: diode emulation is disabled, allowing the frequency applied to the MODE/SYNC pin to be matched without a load.

#### 7.3.2.1 Pulse-Dependent MODE/SYNC Pin Control

Most systems that require more than a single mode of operation from the device are controlled by digital circuitry such as a microprocessor. These systems can generate dynamic signals easily but have difficulty generating multi-level signals. Pulse-dependent MODE/SYNC pin control is useful with these systems. To initiate pulse-dependent MODE/SYNC pin control, apply a valid sync signal. Table 7-1 shows a summary of the pulse dependent mode selection settings.

**Table 7-1. Pulse-Dependent Mode Selection Settings**

| Mode/Sync Input | Mode |
|---|---|
| > $V_{MODE_H}$ | FPWM with spread spectrum factory setting |
| < $V_{MODE_L}$ | Auto mode with spread spectrum factory setting |
| Synchronization Clock | SYNC mode |

Figure 7-4 shows the transition between auto mode and FPWM mode while in pulse-dependent MODE/SYNC control. The device transitions to a new mode of operation after the time, $t_{MODE}$. Figure 7-4 and Figure 7-5 show the details.

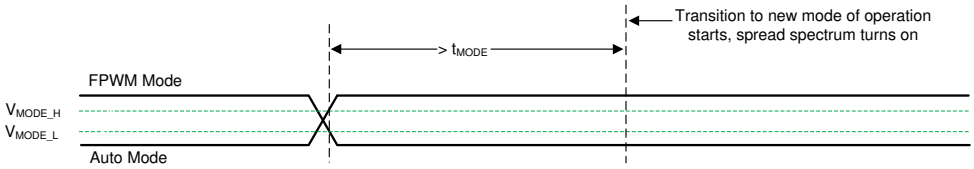



**Figure 7-4. Transition from Auto Mode and FPWM Mode**

If MODE/SYNC voltage remains constant longer than $t_{MODE}$, the device enters either auto mode or FPWM mode with spread spectrum turned on (if factory setting is enabled) and MODE/SYNC continues to operate in pulse-dependent scheme.

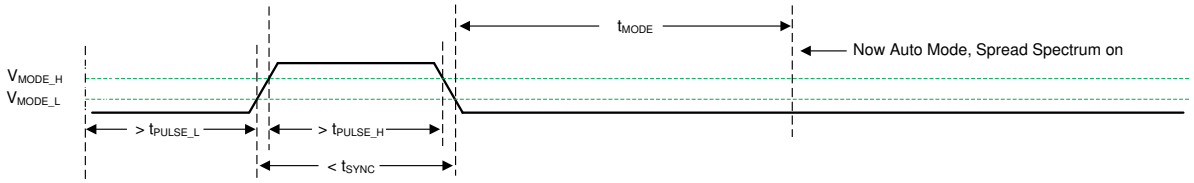



**Figure 7-5. Transition from SYNC Mode to Auto Mode**


Copyright © 2025 Texas Instruments Incorporated

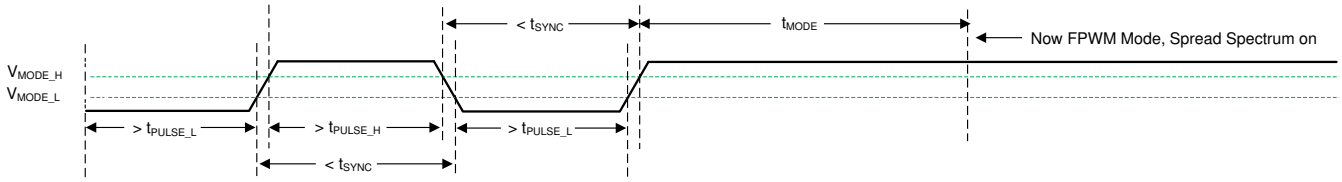



**Figure 7-6. Transition from SYNC Mode to FPWM Mode**

### *7.3.3 Power-Good Output Operation*

Use the power-good feature using the PG pin of the device to reset a system microprocessor whenever the output voltage is out of regulation. This open-drain output remains low under device fault conditions, such as current limit and thermal shutdown, as well as during normal start-up. A glitch filter prevents false flag operation for any short duration excursions in the output voltage, such as during line and load transients. Output voltage excursions lasting less than $t_{RESET_FILTER}$ do not trip the power-good flag. Power-good operation can best be understood in reference to Figure 7-7. Table 7-2 gives a more detailed breakdown of the PG operation. Here, $V_{PG_{UV}}$ is defined as the $PG_{UV}$ scaled version of $V_{OUT}$ (target regulated output voltage) and $V_{PG_{HYST}}$ as the $PG_{HYST}$ scaled version of $V_{OUT}$, where both $PG_{UV}$ and $PG_{HYST}$ are listed in the *Electrical Characteristics*. During the initial power up, a total delay of 8.5 ms (typical) is encountered from the time $V_{EN-VOUT}$ is triggered to the time that the power good is flagged high. This delay only occurs during the device start-up and is not encountered during any other normal operation of the power-good function. When EN is pulled low, the power-good flag output is also forced low. With EN low, power good remains valid as long as the input voltage, $V_{PG-VAL}$, is greater 1.5 V (maximum).

The power-good output scheme consists of an open-drain n-channel MOSFET, which requires an external pullup resistor connected to a suitable logic supply. The power-good output scheme can also be pulled up to either $V_{CC}$ or $V_{OUT}$ through an appropriate resistor, as desired. If this function is not needed, the PG pin can be open or grounded. Limit the current into this pin to ≤ 4 mA.

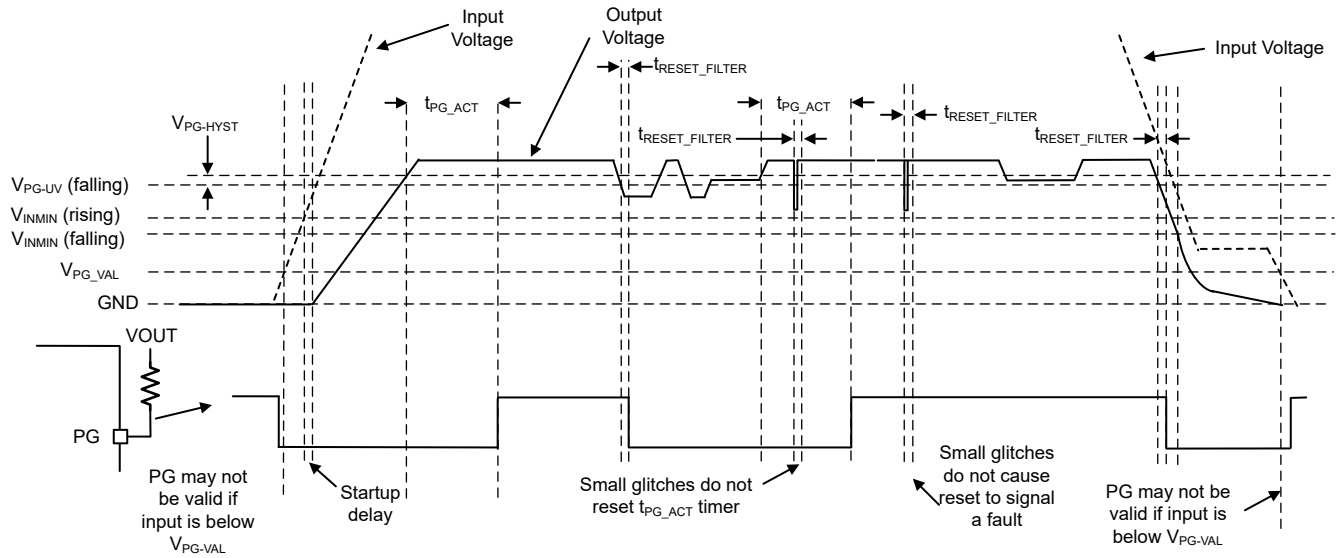



**Figure 7-7. Power-Good Operation (OV Events Not Included)**

**Table 7-2. Fault Conditions for PG (Pull Low)**

| Fault Condition Initiated | Fault Condition Ends (After Which $t_{PG_ACT}$ Must Pass Before PG Output is Released) |
|---|---|
| $V_{OUT} < V_{PG_{UV}}$ AND $t > t_{RESET_FILTER}$ | Output voltage in regulation: $V_{PG_{UV}} + V_{PG_{HYST}} < V_{OUT} < V_{PG_{OV}} - V_{PG_{HYST}}$ |
| $V_{OUT} > V_{PG_{OV}}$ AND $t > t_{RESET_FILTER}$ | Output voltage in regulation |
| $T_J > T_{SD(trip)}$ | $T_J < T_{SD(trip)} - T_{SD(hyst)}$ AND output voltage in regulation |
| $EN < V_{EN-VOUT} - V_{EN-HYST}$ | $EN > V_{EN-VOUT}$ AND output voltage in regulation |

### 7.3.4 Internal LDO, VCC, and VOUT/FB Input

The device uses the internal LDO output and the VCC pin for all internal power supply. The VCC pin draws power either from the VIN (in adjustable output variants) or VOUT/FB (in fixed-output variants). In the fixed-output variants, after the device is active but has yet to regulate, the VCC rail continues to draw power from the input voltage, $V_{IN}$, until the VOUT/FB voltage reaches > 3.15 V (or when the device has reached steady-state regulation post the soft start). The VCC rail typically measures 3.3 V in both adjustable and fixed output variants. During start-up, VCC momentarily exceeds the normal operating voltage and then drops to the normal operating voltage.

### 7.3.5 Bootstrap Voltage and $V_{BOOT-UVLO}$ (BOOT Terminal)

The high-side switch driver circuit requires a bias voltage higher than VIN to make sure the HS switch is turned on. The internal 0.1-µF capacitor that is connected between BOOT and SW works as a charge pump to boost voltage on the BOOT terminal to (SW + VCC). The boot diode is integrated on the device die to minimize physical design size. The CBOOT rail has a UVLO setting. This UVLO has a threshold of $V_{BOOT-UVLO}$ and is typically set at 2.1 V. If the BOOT capacitor is not charged above this voltage with respect to the SW pin, then the part initiates a charging sequence, turning on the low-side switch before attempting to turn on the high-side device.

### 7.3.6 Output Voltage Selection

In the device family, an adjustable output or fixed output voltage option is configurable for every device variant (see Section 4). For an adjustable output, the user needs an external resistor divider connection between the output voltage node, the device FB pin, and the system GND, as shown in Figure 7-8. The adjustable output voltage operation uses a 1-V internal reference voltage. Refer to Section 8.2.1.2.2.1 for more details on how to adjust the output voltage.

When using the fixed-output configuration from the device family, simply connect the FB pin (identified as VOUT/FB pin for fixed-output variants in the rest of the data sheet) to the system output voltage node. See Section 4 for more details.

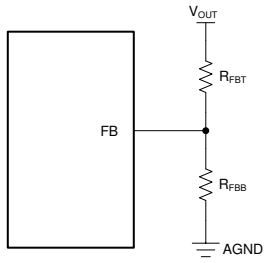



**Figure 7-8. Setting Output Voltage for Adjustable Output Variant**

In adjustable output voltage variants, an additional feedforward capacitor, $C_{FF}$, in parallel with the $R_{FBT}$, can be used to optimize the phase margin and transient response. See Section 8.2.1.2.8 for more details. No additional resistor divider or feedforward capacitor is needed in fixed-output variants.


Copyright © 2025 Texas Instruments Incorporated

### 7.3.7 Spread Spectrum

In the LMQ664x0-Q1 family of devices, spread spectrum is a factory option. To find which parts have spread spectrum enabled, see Section 4.

Spread spectrum reduces peak emissions at specific frequencies by spreading these peaks across a wider range of frequencies than a part with fixed-frequency operation. The LMQ664x0-Q1 implements a modulation pattern designed to reduce low frequency-conducted emissions from the first few harmonics of the switching frequency. The pattern can also help reduce the higher harmonics that are more difficult to filter, which can fall in the FM band. These harmonics often couple to the environment through electric fields around the switch node and inductor. The LMQ664x0-Q1 uses a spread of frequencies, which can spread energy smoothly across the FM and TV bands. The device implements dual random spread spectrum (DRSS). DRSS is a combination of a triangular frequency spreading pattern and pseudorandom frequency hopping. The combination allows the spread spectrum to be very effective at spreading the energy at the following:

- Fundamental switching harmonic with slow triangular pattern
- High frequency harmonics with additional pseudo-random jumps at the switching frequency

The advantage of DRSS is the equivalent harmonic attenuation in the upper frequencies with a smaller fundamental frequency deviation. This reduces the amount of input current and output voltage ripple that is introduced at the modulating frequency. Additionally, the LMQ664x0-Q1 also allows the user to further reduce the output voltage ripple caused by the spread spectrum modulating pattern.

The spread spectrum is only available while the clock of the device is free running at the natural frequency. Any of the following conditions overrides spread spectrum, turning spread spectrum off:

- The clock is slowed due to operation at low-input voltage – this is operation in dropout.
- The clock is slowed under light load in auto mode. Note that if you are operating in FPWM mode, spread spectrum can be active, even if there is no load.
- The clock is slowed due to high input to output voltage ratio. This mode of operation is expected if on time reaches minimum on time. See the *Electrical Characteristics*.
- The clock is synchronized with an external clock.

### 7.3.8 Soft Start and Recovery from Dropout

When designing with the LMQ664x0-Q1, consider slow rise in output voltage due to recovery from dropout and soft start as two separate operating conditions, as shown in Figure 7-9 and Figure 7-10. Soft start is triggered by any of the following conditions:

- Power is applied to the VIN pin of the device, releasing undervoltage lockout.
- EN is used to turn on the device.
- Recovery from shutdown due to overtemperature protection

After soft start is triggered, the IC takes the following actions:

- The reference used by the IC to regulate output voltage is slowly ramped up. The net result is that output voltage, if previously 0 V, takes $t_{SS}$ to reach 90% of the desired value.
- Operating mode is set to auto mode of operation, activating the diode emulation mode for the low-side MOSFET. This action allows start-up without pulling the output low. This is true even when there is a voltage already present at the output during a prebias start-up.

Copyright © 2025 Texas Instruments Incorporated

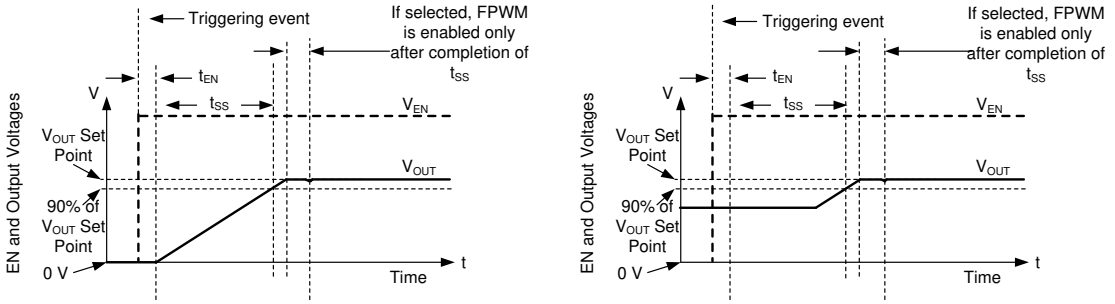



**Figure 7-9. Soft Start With and Without Prebias Voltage**

#### 7.3.8.1 Recovery from Dropout

Any time the output voltage falls more than a few percent, output voltage ramps up slowly. This condition, called graceful recovery from dropout in this document, differs from soft start in two important ways:

- The reference voltage is set to approximately 1% above what is needed to achieve the existing output voltage.
- If the device is set to FPWM, the device continues to operate in that mode during the recovery from dropout. If output voltage were to suddenly be pulled up by an external supply, the LMQ664x0-Q1 can pull down on the output. Note that all protections that are present during normal operation are in place, preventing any catastrophic failure if output is shorted to a high voltage or ground.

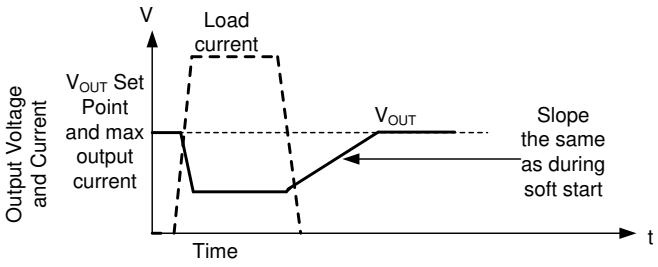



**Figure 7-10. Recovery from Dropout**

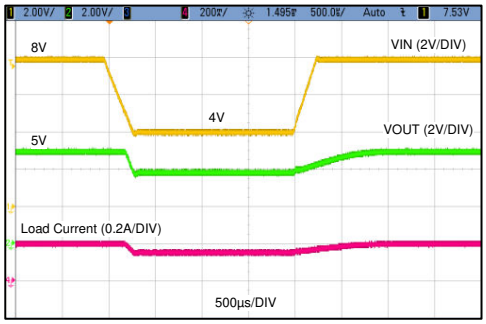



**Figure 7-11. Typical Output Recovery from Dropout from 8 V to 4 V**

Whether output voltage falls due to high load or low input voltage, after the condition that causes output to fall below the set point is removed, the output climbs at the same speed as during start-up. Figure 7-11 shows an example of this behavior.

### *7.3.9 Current Limit and Short Circuit*

The device is protected from over current conditions by cycle-by-cycle current limiting on both high-side and low-side MOSFETs. High-side (HS) MOSFET over current protection is implemented by the typical peak-current mode control scheme. The HS switch current is sensed when the HS is turned on after a short blanking time. The HS switch current is compared to either the minimum of a fixed current set point or the output of the internal error amplifier loop minus the slope compensation every switching cycle. When the HS switch current hits the current limit threshold, the HS switch is turned off. Because the output of the internal error amplifier loop has a maximum value and slope compensation increases with duty cycle, HS current limit decreases with increased duty factor if duty factor is typically above 35%.

When the low-side (LS) switch is turned on, the current going through the switch is also sensed and monitored. Like the high-side device, the low-side device has a turn-off commanded by the internal error amplifier loop. In the case of the low-side device, turn-off is prevented if the current exceeds this value, even if the oscillator normally starts a new switching cycle. Also like the high-side device, there is a limit on how high the turn-off


Copyright © 2025 Texas Instruments Incorporated

current is allowed to be. This limit is called the low-side current limit, $I_{VALMAX}$ in Figure 7-12. If the LS current limit is exceeded, the LS MOSFET stays on and the HS switch is not to be turned on. The LS switch is turned off after the LS current falls below this limit and the HS switch is turned on again as long as at least one clock period has passed since the last time the HS device has turned on.

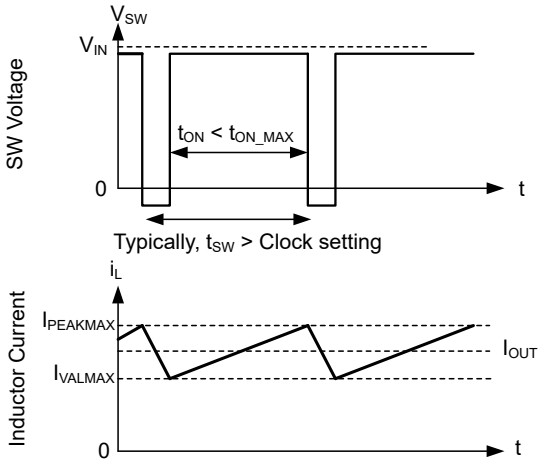



**Figure 7-12. Current Limit Waveforms**

Because the current waveform assumes values between $I_{PEAKMAX}$ and $I_{VALMAX}$, the maximum output current is very close to the average of these two values unless duty factor is very high. After operating in current limit, hysteretic control is used and current does not increase as output voltage approaches zero.

The LMQ664x0-Q1 employs hiccup over current protection if there is an extreme overload, and the following conditions are met:

- Output voltage is below approximately 0.4 times the output voltage set point.
- Greater than $t_{SS}$ has passed since soft start has started.
- The part is not operating in dropout, which is defined as having a minimum off time controlled duty cycle.

In hiccup mode, the device shuts down and attempts to soft start after $t_{HICCUP}$. Hiccup mode helps reduce the device power dissipation under severe over current conditions and short circuits. See Figure 7-13.

After the overload is removed, the device recovers as though in soft start; see Figure 7-14.

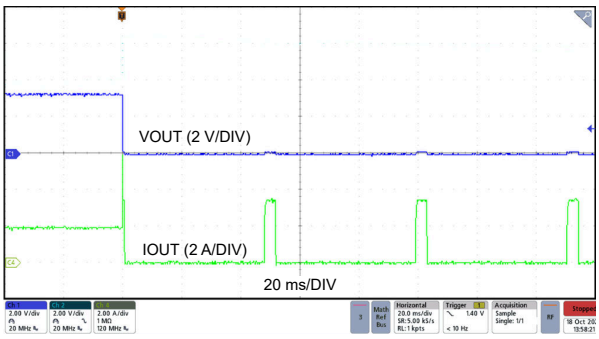



**Figure 7-13. Hiccup Entry**

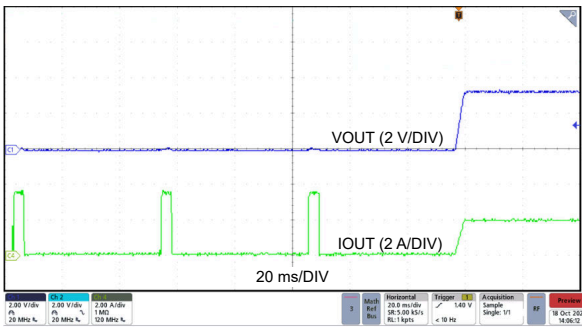



**Figure 7-14. Hiccup Exit**

### *7.3.10 Thermal Shutdown*

Thermal shutdown limits total power dissipation by turning off the internal switches when the device junction temperature exceeds 168°C (typical). Thermal shutdown does not trigger below 158°C (minimum). After thermal shutdown occurs, hysteresis prevents the part from switching until the junction temperature drops to

Copyright © 2025 Texas Instruments Incorporated

approximately 153°C (typical). When the junction temperature falls below 153°C (typical), the device attempts another soft start.

While the device is shut down due to high junction temperature, power continues to be provided to VCC. To prevent overheating due to a short circuit applied to VCC, the LDO that provides power for VCC has reduced current limit while the part is disabled due to high junction temperature. The LDO only provides a few milliamperes during thermal shutdown.

#### 7.3.11 Input Supply Current

The device is designed to have very low input supply current when regulating light loads. This is achieved by powering much of the internal circuitry from the output. The VOUT/FB pin in the fixed-output voltage variants is the input to the LDO that powers the majority of the control circuits. By connecting the VOUT/FB input pin to the output node of the regulator, a small amount of current is drawn from the output. This current is reduced at the input by the ratio of $V_{OUT}$ / $V_{IN}$.

$$I_{QVIN} = I_Q + I_{EN} + I_{BIAS} \times \frac{V_{OUT}}{\eta_{eff} \times V_{IN}} \quad (1)$$

where

- $I_{QVIN}$ is the total standby (switching) current consumed by the operating (switching) buck converter when unloaded.
- $I_Q$ is the current drawn from the $V_{IN}$ terminal.
- $I_{EN}$ is current drawn by the EN terminal. Include this current if EN is connected to VIN. Check $I_{LKG-EN}$ in the *Electrical Characteristics* for $I_{EN}$.
- $I_{BIAS}$ is bias current drawn by the BIAS LDO.
- $\eta_{eff}$ is the light-load efficiency of the buck converter with $I_{Q_VIN}$ removed from the input current of the buck converter. $\eta_{eff}$ = 0.8 is a conservative value that can be used under normal operating conditions. This can be traced back as the $I_{SUPPLY}$ in the *System Characteristics*.

### 7.4 Device Functional Modes

#### 7.4.1 Shutdown Mode

The EN pin provides electrical ON and OFF control of the device. When the EN pin voltage is below 0.4 V, both the converter and the internal LDO have no output voltage and the part is in shutdown mode. In shutdown mode, the quiescent current drops to typically 250 nA.

#### 7.4.2 Standby Mode

The internal LDO has a lower EN threshold than the output of the converter. When the EN pin voltage is above 1 V (maximum) and below the precision enable threshold for the output voltage, the internal LDO regulates the VCC voltage at 3.3 V typical. The precision enable circuitry is ON after VCC is above the UVLO. The internal power MOSFETs of the SW node remain off unless the voltage on EN pin goes above the precision enable threshold. The device also employs UVLO protection. If the VCC voltage is below the UVLO level, the output of the converter turns off.

#### 7.4.3 Active Mode

The device is in active mode whenever the EN pin is above $V_{EN-VOUT}$, $V_{IN}$ is high enough to satisfy $V_{INMIN}$, and no other fault conditions are present. The simplest way to enable the operation is to connect the EN pin to $V_{IN}$, which allows the device to start up when the applied input voltage exceeds the minimum $V_{INMIN}$.

In active mode, depending on the load current, input voltage, and output voltage, the device is in one of five modes:

- *Continuous conduction mode (CCM)* with fixed switching frequency when load current is above half of the inductor current ripple
- *Auto mode* – light load operation: PFM when switching frequency is decreased at very light load
- *FPWM mode* – light load operation: Discontinuous conduction mode (DCM) when the load current is lower than half of the inductor current ripple


Copyright © 2025 Texas Instruments Incorporated

- *Minimum on time*: At high input voltage and low output voltages, the switching frequency is reduced to maintain regulation.
- *Dropout mode*: When switching frequency is reduced to minimize voltage dropout

#### 7.4.3.1 CCM Mode

The following operating description of the device refers to Section 7.2 and to the waveforms in Figure 7-15. In CCM, the device supplies a regulated output voltage by turning on the internal high-side (HS) and low-side (LS) switches with varying duty cycle (D). During the HS switch on time, the SW pin voltage, $V_{SW}$, swings up to approximately $V_{IN}$, and the inductor current, $i_L$, increases with a linear slope. The HS switch is turned off by the control logic. During the HS switch off time, $t_{OFF}$, the LS switch is turned on. Inductor current discharges through the LS switch, which forces the $V_{SW}$ to swing below ground by the voltage drop across the LS switch. The converter loop adjusts the duty cycle to maintain a constant output voltage. D is defined by the on time of the HS switch over the switching period:

$$D = \frac{T_{ON}}{T_{SW}} \tag{2}$$

In an ideal buck converter where losses are ignored, D is proportional to the output voltage and inversely proportional to the input voltage:

$$D = \frac{V_{OUT}}{V_{IN}} \tag{3}$$

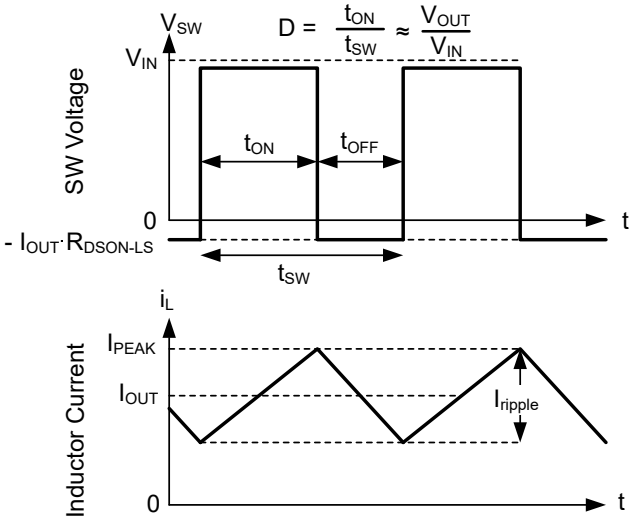



**Figure 7-15. SW Voltage and Inductor Current Waveforms in Continuous Conduction Mode (CCM)**

#### 7.4.3.2 Auto Mode – Light Load Operation

The LMQ664x0-Q1 can have two behaviors while lightly loaded. One behavior, called auto mode operation, allows for seamless transition between normal current mode operation while heavily loaded and highly efficient light load operation. Note that for output voltages between 1-V and 2-V multi-pulsing behavior can be observed on the switch node waveform when the device transitions from PFM to PWM mode. The other behavior, called FPWM mode, maintains full frequency even when unloaded. Which mode the device operates in depends on which variant from this family is selected. Note that all parts operate in FPWM mode when synchronizing frequency to an external signal.

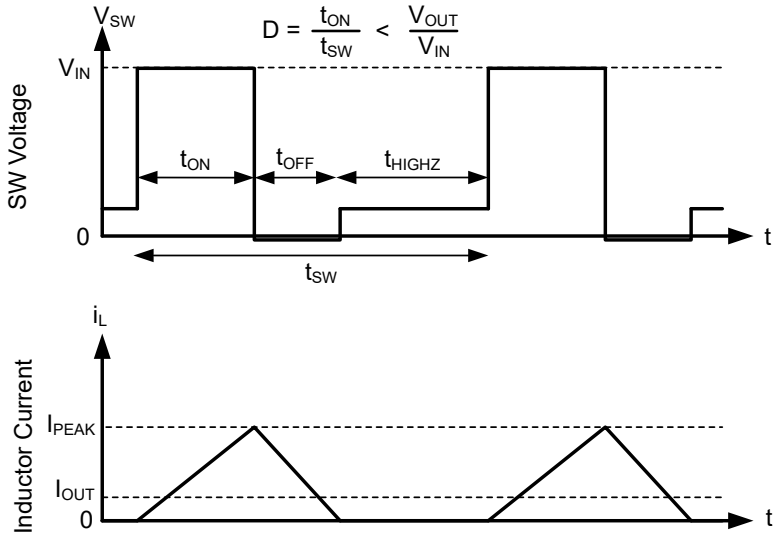
The light load operation is employed in the device only in auto mode. The light load operation employs two techniques to improve efficiency:

- Diode emulation, which allows DCM operation. See Figure 7-16.
- Frequency reduction. See Figure 7-16.

Note that while these two features operate together to improve light load efficiency, these features operate independently.

##### *7.4.3.2.1 Diode Emulation*

Diode emulation prevents reverse current through the inductor, which requires a lower frequency needed to regulate given a fixed peak inductor current. Diode emulation also limits ripple current as frequency is reduced. With a fixed peak current, as output current is reduced to zero, frequency must be reduced to near zero to maintain regulation.




In auto mode, the low-side device is turned off after SW node current is near zero. As a result, after output current is less than half of what inductor ripple can be in CCM, the part operates in DCM, which is equivalent to the statement that diode emulation is active.

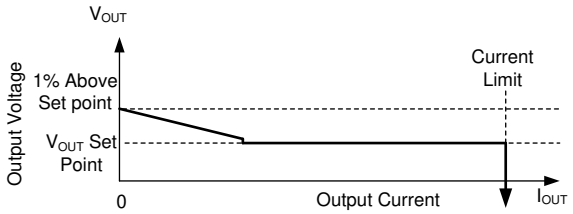
**Figure 7-16. PFM Operation**

The device has a minimum peak inductor current setting (see $I_{PEAKMIN}$ in the *Electrical Characteristics*) while in auto mode. After current is reduced to a low value with fixed input voltage, on time is constant. Regulation is then achieved by adjusting frequency. This mode of operation is called PFM mode regulation.


Copyright © 2025 Texas Instruments Incorporated

#### *7.4.3.2.2 Frequency Reduction*

The device reduces frequency whenever output voltage is high. This function is enabled whenever the internal error amplifier compensation output, COMP, an internal signal, is low and there is an offset between the regulation set point of FB and the voltage applied to FB. The net effect is that there is larger output impedance while lightly loaded in auto mode than in normal operation. Output voltage must be approximately 1% high when the part is completely unloaded.



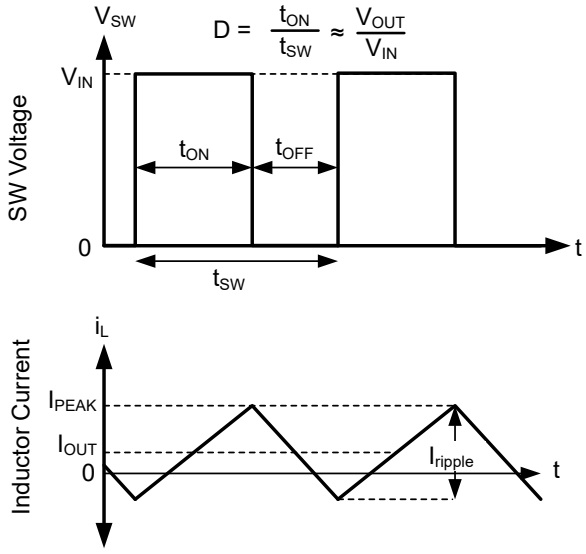

In auto mode, after output current drops below approximately 1/10th the rated current of the part, output resistance increases so that output voltage is 1% high while the buck is completely unloaded.

**Figure 7-17. Steady State Output Voltage Versus Output Current in Auto Mode**

In PFM operation, a small DC positive offset is required on the output voltage to activate the PFM detector. The lower the frequency in PFM, the more DC offset is needed on $V_{OUT}$. If the DC offset on $V_{OUT}$ is not acceptable, a dummy load at $V_{OUT}$ or FPWM mode can be used to reduce or eliminate this offset.

#### 7.4.3.3 FPWM Mode – Light Load Operation

In FPWM mode, frequency is maintained while lightly loaded. To maintain frequency, a limited reverse current is allowed to flow through the inductor. Reverse current is limited by reverse current limit circuitry, see the *Electrical Characteristics* for reverse current limit values.




In FPWM mode, continuous conduction (CCM) is possible even if $I_{OUT}$ is less than half of $I_{ripple}$.

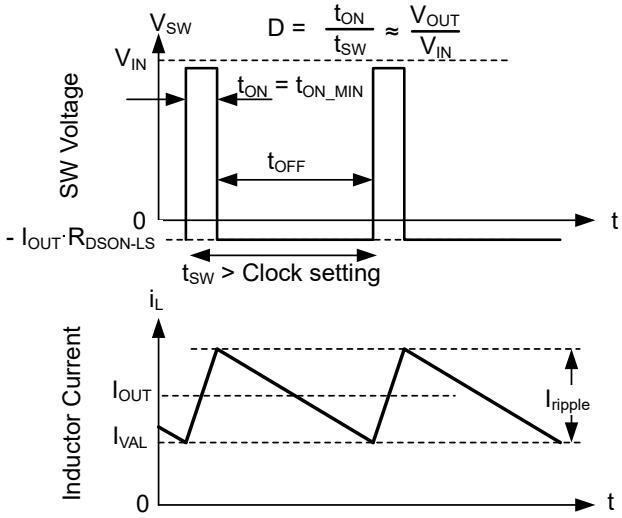
**Figure 7-18. FPWM Mode Operation**

For all devices, in FPWM mode, frequency reduction is still available if output voltage is high enough to command minimum on time even while lightly loaded, allowing good behavior during faults that involve output being pulled up.

Copyright © 2025 Texas Instruments Incorporated

#### 7.4.3.4 Minimum On-Time (High Input Voltage) Operation

The device continues to regulate output voltage even if the input-to-output voltage ratio requires an on time less than the minimum on time of the chip with a given clock setting. This regulation is accomplished by using valley current control. At all times, the compensation circuit dictates both a maximum peak inductor current and a maximum valley inductor current. If for any reason, valley current is exceeded, the clock cycle is extended until valley current falls below that determined by the compensation circuit. If the converter is not operating in current limit, the maximum valley current is set above the peak inductor current, preventing valley control from being used unless there is a failure to regulate using peak current only. If the input-to-output voltage ratio is too high, such that the inductor current peak value exceeds the peak command dictated by compensation, the high-side device cannot be turned off quickly enough to regulate output voltage. As a result, the compensation circuit reduces both peak and valley current. After a low enough current is selected by the compensation circuit, valley current matches that being commanded by the compensation circuit. Under these conditions, the low-side device is kept on and the next clock cycle is prevented from starting until inductor current drops below the desired valley current. Because the on time is fixed at the minimum value, this type of operation resembles that of a device using a constant on-time (COT) control scheme; see Figure 7-19.



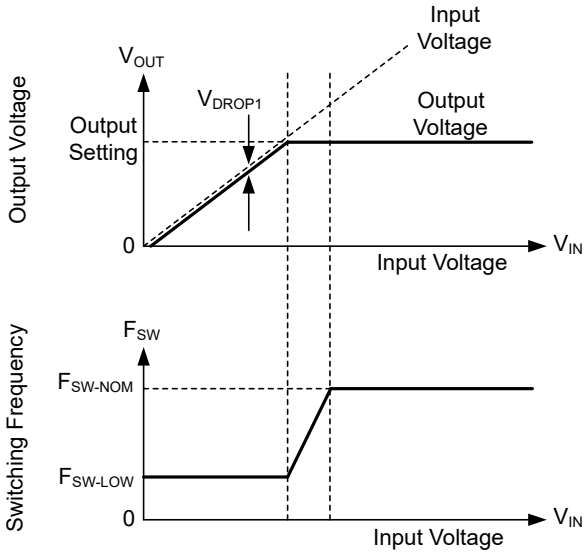

In valley control mode, minimum inductor current is regulated, not peak inductor current.

**Figure 7-19. Valley Current Mode Operation**


Copyright © 2025 Texas Instruments Incorporated

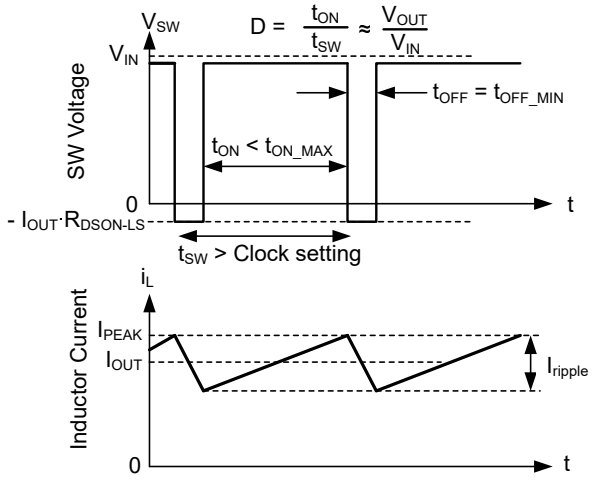
#### 7.4.3.5 Dropout

Dropout operation is defined as any input-to-output voltage ratio that requires frequency to drop to achieve the required duty cycle. At a given clock frequency the duty cycle is limited by minimum off time. After this limit is reached, as shown in Figure 7-21, and the clock frequency was to be maintained, the output voltage can fall. Instead of allowing the output voltage to drop, the device extends the high-side switch on time past the end of the clock cycle until the needed peak inductor current is achieved. The clock is allowed to start a new cycle after peak inductor current is achieved or after a pre-determined maximum on time, $t_{ON-MAX}$, of approximately 9 µs passes. As a result, after the needed duty cycle cannot be achieved at the selected clock frequency due to the existence of a minimum off time, frequency drops to maintain regulation. As shown in Figure 7-20, if input voltage is low enough so that output voltage cannot be regulated even with an on time of $t_{ON-MAX}$, output voltage drops to slightly below the input voltage by $V_{DROP1}$. For additional information on recovery from dropout, refer to Figure 7-10.




Output voltage and frequency versus input voltage: If there is little difference between input voltage and output voltage setting, the IC reduces frequency to maintain regulation. If input voltage is too low to provide the desired output voltage at $F_{SW-LOW}$ which is approximately 110-kHz, input voltage tracks output voltage.

**Figure 7-20. Frequency and Output Voltage in Dropout**




Switching waveforms while in dropout. Inductor current takes longer than a normal clock to reach the desired peak value. As a result, frequency drops. This frequency drop is limited by $t_{ON-MAX}$.

**Figure 7-21. Dropout Waveforms**


Copyright © 2025 Texas Instruments Incorporated

# 8 Application and Implementation

**Note**

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

## 8.1 Application Information

The LMQ664x0-Q1 step-down DC-to-DC converters are typically used to convert a higher DC voltage to a lower DC voltage. The LMQ66430-Q1 supports a maximum output current of 3 A while the LMQ66420-Q1 and LMQ66410-Q1 support a maximum output current of 2 A and 1 A, respectively. The following design procedure can be used to select components for the LMQ66430-Q1. The design procedure can also be used to select components for the LMQ66420-Q1 or LMQ66410-Q1 by limiting the maximum output current to 2 A or 1 A, respectively.

**Note**

All of the capacitance values given in the following application information refer to *effective* values unless otherwise stated. The *effective* value is defined as the actual capacitance under DC bias and temperature, not the rated or nameplate values. Use high-quality, low-ESR, ceramic capacitors with an X7R or better dielectric throughout. All high value ceramic capacitors have a large voltage coefficient in addition to normal tolerances and temperature effects. Under DC bias the capacitance drops considerably. Large case sizes and higher voltage ratings are better in this regard. To help mitigate these effects, multiple capacitors can be used in parallel to bring the minimum *effective* capacitance up to the required value. This action can also ease the RMS current requirements on a single capacitor. A careful study of bias and temperature variation of any capacitor bank must be made to make sure that the minimum value of *effective* capacitance is provided.

Copyright © 2025 Texas Instruments Incorporated

## 8.2 Typical Application

For the circuit schematic, bill of materials, PCB layout files, and test results of an LMQ664x0-Q1 implementation see the LMQ66430-Q1 EVM. As a quick-start guide, Table 8-1 and Table 8-4 provide typical component values for a range of the most common output voltages.

**Table 8-1. Typical External Component Values for Adjustable Output LMQ66430-Q1**

| $f_{SW}$ (kHz) (1) | $V_{OUT}$ (V) | L (µH) | Nominal $C_{OUT}$ (Rated Capacitance) | Minimum $C_{OUT}$(Effective Capacitance)(2) | $R_{FBT}$ (kΩ)(3) | $R_{FBB}$ (kΩ) | $C_{IN}$ | $C_{BOOT}$ | $C_{VCC}$ | $C_{FF}$ (4) |
|---|---|---|---|---|---|---|---|---|---|---|
| 400 | 3.3 | 10 | 3 × 22µF | 60µF | 33.2 | 14.3 | 4.7µF | DNP | 1µF | 100pF |
| 2200 | 3.3 | 2.2 | 3 × 22µF | 60µF | 33.2 | 14.3 | 4.7µF | DNP | 1µF | DNP |
| 400 | 5 | 10 | 3 × 22µF | 60µF | 49.9 | 12.4 | 4.7µF | DNP | 1µF | 100pF |
| 2200 | 5 | 2.2 | 3 × 22µF | 60µF | 49.9 | 12.4 | 4.7µF | DNP | 1µF | DNP |

(1) Inductor values are calculated based on typical $V_{IN}$ = 12V.
(2) Minimum $C_{OUT}$ values take into account the effects of DC bias voltage and temperature on the actual capacitance value.
(3) For $R_{FBT}$ and $R_{FBB}$ values outside the range stated above, see Section 8.2.1.2.2.1.
(4) See Section 8.2.1.2.8 for more information.

**Table 8-2. Typical External Component Values for Adjustable Output LMQ66420-Q1**

| $f_{SW}$ (kHz) (1) | $V_{OUT}$ (V) | L (µH) | Nominal $C_{OUT}$ (Rated Capacitance) | Minimum $C_{OUT}$(Effective Capacitance)(2) | $R_{FBT}$ (kΩ)(3) | $R_{FBB}$ (kΩ) | $C_{IN}$ | $C_{BOOT}$ | $C_{VCC}$ | $C_{FF}$ (4) |
|---|---|---|---|---|---|---|---|---|---|---|
| 400 | 3.3 | 6.8 | 3 × 22µF | 60µF | 33.2 | 14.3 | 4.7µF | DNP | 1µF | 100pF |
| 2200 | 3.3 | 2.2 | 2 × 22µF | 40µF | 33.2 | 14.3 | 4.7µF | DNP | 1µF | DNP |
| 400 | 5 | 6.8 | 3 × 22µF | 60µF | 49.9 | 12.4 | 4.7µF | DNP | 1µF | 100pF |
| 2200 | 5 | 2.2 | 2 × 22µF | 40µF | 49.9 | 12.4 | 4.7µF | DNP | 1µF | DNP |

(1) Inductor values are calculated based on typical $V_{IN}$ = 12V.
(2) Minimum $C_{OUT}$ values take into account the effects of DC bias voltage and temperature on the actual capacitance value.
(3) For $R_{FBT}$ and $R_{FBB}$ values outside the range stated above, see Section 8.2.1.2.2.1.
(4) See Section 8.2.1.2.8 for more information.

**Table 8-3. Typical External Component Values for Adjustable Output LMQ66410-Q1**

| $f_{SW}$ (kHz) (1) | $V_{OUT}$ (V) | L (µH) | Nominal $C_{OUT}$ (Rated Capacitance) | Minimum $C_{OUT}$(Effective Capacitance)(2) | $R_{FBT}$ (kΩ)(3) | $R_{FBB}$ (kΩ) | $C_{IN}$ | $C_{BOOT}$ | $C_{VCC}$ | $C_{FF}$ (4) |
|---|---|---|---|---|---|---|---|---|---|---|
| 400 | 3.3 | 22 | 2 × 22µF | 40µF | 33.2 | 14.3 | 4.7µF | DNP | 1µF | 100pF |
| 2200 | 3.3 | 4.7 | 1 × 22µF | 20µF | 33.2 | 14.3 | 4.7µF | DNP | 1µF | DNP |
| 400 | 5 | 22 | 2 × 22µF | 40µF | 49.9 | 12.4 | 4.7µF | DNP | 1µF | 100pF |
| 2200 | 5 | 4.7 | 1 × 22µF | 20µF | 49.9 | 12.4 | 4.7µF | DNP | 1µF | DNP |

(1) Inductor values are calculated based on typical $V_{IN}$ = 12V.
(2) Minimum $C_{OUT}$ values take into account the effects of DC bias voltage and temperature on the actual capacitance value.
(3) For $R_{FBT}$ and $R_{FBB}$ values outside the range stated above, see Section 8.2.1.2.2.1.
(4) See Section 8.2.1.2.8 for more information.

**Table 8-4. Typical External Component Values for Fixed Output LMQ66430-Q1**

| $f_{SW}$ (kHz) (1) | $V_{OUT}$ (V) | L (µH) | Nominal $C_{OUT}$ (Rated Capacitance) | Minimum $C_{OUT}$(Effective Capacitance)(2) | $R_{FBT}$ (Ω) | $R_{FBB}$ (Ω)(3) | $C_{IN}$ | $C_{BOOT}$ | $C_{VCC}$ | $C_{FF}$ |
|---|---|---|---|---|---|---|---|---|---|---|
| 400 | 3.3 | 10 | 3 × 22µF | 60µF | 0 | DNP | 4.7µF | DNP | 1µF | DNP |
| 2200 | 3.3 | 2.2 | 2 × 22µF | 40µF | 0 | DNP | 4.7µF | DNP | 1µF | DNP |
| 400 | 5 | 10 | 3 × 22µF | 60µF | 0 | DNP | 4.7µF | DNP | 1µF | DNP |
| 2200 | 5 | 2.2 | 2 × 22µF | 40µF | 0 | DNP | 4.7µF | DNP | 1µF | DNP |

(1) Inductor values are calculated based on typical $V_{IN}$ = 12V.
(2) Minimum $C_{OUT}$ values take into account the effects of DC bias voltage and temperature on the actual capacitance value.


Copyright © 2025 Texas Instruments Incorporated

(3) DNP = Do Not Populate.

**Table 8-5. Typical External Component Values for Fixed Output LMQ66420-Q1**

| $f_{SW}$ (kHz) (1) | $V_{OUT}$ (V) | L (µH) | Nominal $C_{OUT}$ (Rated Capacitance) | Minimum $C_{OUT}$(Effective Capacitance)(2) | $R_{FBT}$ (kΩ) | $R_{FBB}$ (kΩ)(3) | $C_{IN}$ | $C_{BOOT}$ | $C_{VCC}$ | $C_{FF}$ |
|---|---|---|---|---|---|---|---|---|---|---|
| 400 | 3.3 | 6.8 | 3 × 22µF | 60µF | 0 | DNP | 4.7µF | DNP | 1µF | DNP |
| 2200 | 3.3 | 2.2 | 2 × 22µF | 40µF | 0 | DNP | 4.7µF | DNP | 1µF | DNP |
| 400 | 5 | 6.8 | 3 × 22µF | 60µF | 0 | DNP | 4.7µF | DNP | 1µF | DNP |
| 2200 | 5 | 2.2 | 2 × 22µF | 40µF | 0 | DNP | 4.7µF | DNP | 1µF | DNP |

(1) Inductor values are calculated based on typical $V_{IN}$ = 12V.
(2) Minimum $C_{OUT}$ values take into account the effects of DC bias voltage and temperature on the actual capacitance value.
(3) DNP = Do Not Populate.

**Table 8-6. Typical External Component Values for Fixed Output LMQ66410-Q1**

| $f_{SW}$ (kHz) (1) | $V_{OUT}$ (V) | L (µH) | Nominal $C_{OUT}$ (Rated Capacitance) | Minimum $C_{OUT}$(Effective Capacitance)(2) | $R_{FBT}$ (kΩ) | $R_{FBB}$ (kΩ)(3) | $C_{IN}$ | $C_{BOOT}$ | $C_{VCC}$ | $C_{FF}$ |
|---|---|---|---|---|---|---|---|---|---|---|
| 400 | 3.3 | 22 | 2 × 22µF | 40µF | 0 | DNP | 4.7µF | DNP | 1µF | DNP |
| 2200 | 3.3 | 4.7 | 1 × 22µF | 20µF | 0 | DNP | 4.7µF | DNP | 1µF | DNP |
| 400 | 5 | 22 | 2 × 22µF | 40µF | 0 | DNP | 4.7µF | DNP | 1µF | DNP |
| 2200 | 5 | 4.7 | 1 × 22µF | 20µF | 0 | DNP | 4.7µF | DNP | 1µF | DNP |

(1) Inductor values are calculated based on typical $V_{IN}$ = 12V.
(2) Minimum $C_{OUT}$ values take into account the effects of DC bias voltage and temperature on the actual capacitance value.
(3) DNP = Do Not Populate.

### *8.2.1 Design 1 - Automotive Synchronous Buck Regulator at 2.2 MHz*

Figure 8-1 shows a typical application circuit of the LMQ664x0-Q1 synchronous buck regulator with output voltage set at 3.3 V and rated load current of 3 A. This device is designed to function over a wide range of external components and system parameters. However, the internal compensation is optimized for a certain range of external inductance and output capacitance. In this example the nominal input voltage is 12 V and ranges between 4 V and 36 V. The maximum switching frequency is set at 2.2 MHz by connecting the MODE/SYNC pin to GND, which allows for the device to operate in AUTO mode. The VOUT/FB pin is connected directly to the output voltage node which improves efficiency performance.

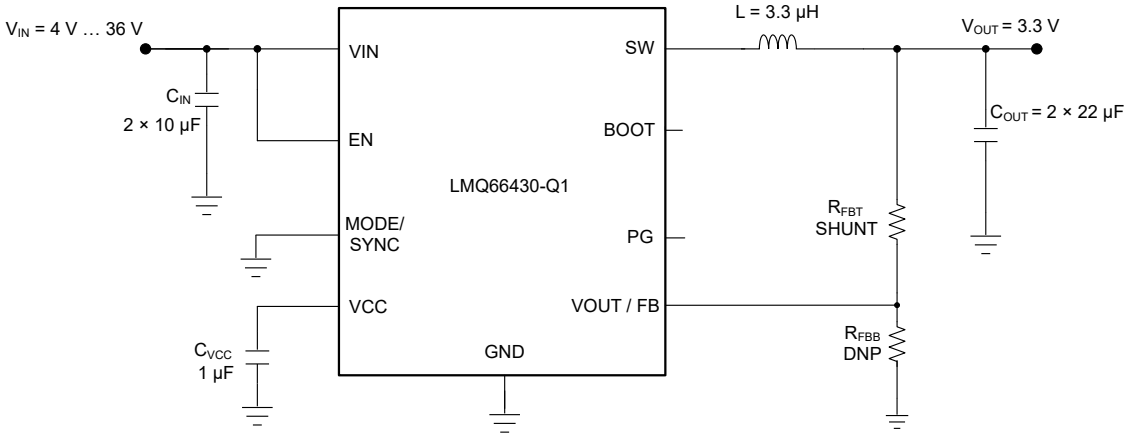



**Figure 8-1. Application Circuit 1 - 3.3 V (fixed), 3 A, 2.2 MHz**

#### 8.2.1.1 Design Requirements

Section 8.2.1.2 provides a detailed design procedure based on Table 8-7.

**Table 8-7. Detailed Design Parameters**

| DESIGN PARAMETER | EXAMPLE VALUE |
|---|---|
| Input voltage | 12 V (4 V to 36 V) |
| Output voltage | 3.3 V |
| Maximum output current | 0 A to 3 A |
| Switching frequency | 2200 kHz |

#### 8.2.1.2 Detailed Design Procedure

The following design procedure applies to Figure 8-1 and Table 8-4.

##### *8.2.1.2.1 Choosing the Switching Frequency*

The choice of switching frequency is a compromise between conversion efficiency and overall design size. Lower switching frequency implies reduced switching losses and usually results in higher system efficiency. However, higher switching frequency allows the use of smaller inductors and output capacitors, hence, a more compact design. For this example, 2200 kHz is used.

For designs that synchronize the switching frequency using the SYNC pin, this pin must not be left floating. To make sure that the SYNC pin has a known state, place either a pullup or pulldown resistor depending on the desired default switching state. If a pullup resistor is selected, make sure that the pullup source voltage does not exceed the absolute maximum rating of the pin.

##### *8.2.1.2.2 Setting the Output Voltage*

$V_{OUT}$ / FB of the device can be either connected directly to the output capacitor or a midpoint of a feedback resistor divider. When connected directly to the output capacitor, the device assumes that a fixed output voltage of either 3.3 V or 5 V is desired. The 3.3-V or 5-V fixed output options are factory trimmed and the output is unique to a specific device. See Section 4 for the selection of fixed output voltage versions.

###### *8.2.1.2.2.1 $V_{OUT}$ / FB for Adjustable Output*

If other voltages are desired, $V_{OUT}$ / FB can be connected to a feedback resistor divider network to set the output voltage. The divider network is comprised of $R_{FBT}$ and $R_{FBB}$, and closes the loop between the output voltage and the converter. The converter regulates the output voltage by holding the voltage on the $V_{OUT}$ / FB pin equal to the internal reference voltage, $V_{REF}$. The converter determines whether fixed output voltage or adjustable output voltage is required by sensing the resistance of the feedback path during start-up. To make sure that the converter regulates to the desired output voltage, the typical minimum value for the parallel combination of $R_{FBT}$ and $R_{FBB}$ is 5 kΩ while the typical maximum value is 10 kΩ as shown in Equation 4. Use Equation 5 as a starting point to determine the value of $R_{FBT}$. Reference Table 8-8 for a list of acceptable resistor values for various output voltages.

$$5\ k\Omega\ <\ R_{FBT}||R_{FBB}\ \leq 10\ k\Omega \tag{4}$$

$$R_{FBT} \leq 10\ k\Omega \times \frac{V_{OUT}}{1\ V} \tag{5}$$


Copyright © 2025 Texas Instruments Incorporated

**Table 8-8. Recommended Feedback Resistor Values for Various Output Voltages**

| $V_{OUT}$ (V) | $R_{FBT}$ (kΩ)(1) | $R_{FBB}$ (kΩ) |
|---|---|---|
| 2.5 | 24.9 | 16.5 |
| 3.3 | 33.2 | 14.3 |
| 5 | 49.9 | 12.4 |
| 6 | 60.4 | 12.1 |
| 9 | 90.9 | 11.3 |

(1) $R_{FBT}$ and $R_{FBB}$ based on 1% standard resistor values.

For this 3.3-V example, the user can choose the LMQ66430MC3RXBRQ1 and connect $V_{OUT}$ / FB directly to the output capacitor.

#### 8.2.1.2.3 Inductor Selection

The parameters for selecting the inductor are the inductance and saturation current. The inductance is based on the desired peak-to-peak ripple current and is normally chosen to be in the range of 20% to 40% of the maximum output current capability of the device (example 3-A for LMQ664x0-Q1). Note that when selecting the ripple current use the maximum device current. Use Equation 6 to determine the value of inductance. The constant K is the ratio of peak-to-peak inductor current ripple to the maximum device current. For this example, choose K = 0.2 and find an inductance of L = 1.81 µH. Select the standard value of 2.2 µH.

$$L = \frac{(V_{IN} - V_{OUT})}{f_{SW} \times K \times I_{OUTmax}} \times \frac{V_{OUT}}{V_{IN}} \quad (6)$$

Ideally, the saturation current rating of the inductor is at least as large as the high-side switch current limit, $I_{PEAKMAX}$ (see the *Electrical Characteristics*). This size makes sure that the inductor does not saturate, even during a short circuit on the output. When the inductor core material saturates, the inductance falls to a very low value, causing the inductor current to rise very rapidly. Although the valley current limit, $I_{VALMAX}$, is designed to reduce the risk of current runaway, a saturated inductor can cause the current to rise to high values very rapidly. This action can lead to component damage. Do not allow the inductor to saturate. Inductors with a ferrite core material have very *hard* saturation characteristics, but usually have lower core losses than powdered iron cores. Powered iron cores exhibit a *soft* saturation, allowing some relaxation in the current rating of the inductor. However, powered iron cores have more core losses at frequencies above about 1 MHz. In any case, the inductor saturation current must not be less than the maximum peak inductor current at full load.

The maximum inductance is limited by the minimum current ripple for the current mode control to perform correctly. The minimum inductor ripple current must be no less than about 10% of the device maximum rated current under nominal conditions.

#### 8.2.1.2.4 Output Capacitor Selection

The current mode control scheme of the LMQ664x0-Q1 devices allows operation over a wide range of output capacitance. The output capacitor bank is usually limited by the load transient requirements and stability rather than the output voltage ripple. Refer to Table 8-1 and Table 8-4 for typical output capacitor values for 3.3-V and 5-V output voltages. Based on Table 8-4, for a fixed 3.3-V output design, the user can choose the recommended 2 × 22-µF ceramic output capacitor for this example. For other designs with other output voltages, WEBENCH can be used as a starting point for selecting the value of output capacitor.

In practice, the output capacitor has the most influence on the transient response and loop-phase margin. Load transient testing and bode plots are the best way to validate any given design and must always be completed before the application goes into production. In addition to the required output capacitance, a small ceramic capacitor placed on the output can help reduce high-frequency noise. Small-case size ceramic capacitors in the range of 1 nF to 100 nF can be very helpful in reducing spikes on the output caused by inductor and board parasitics.

Limit the maximum value of total output capacitance to about 10 times the design value, or 1000 µF, whichever is smaller. Large values of output capacitance can adversely affect the start-up behavior of the regulator as well

Copyright © 2025 Texas Instruments Incorporated

as the loop stability. If values larger than noted here must be used, then perform a careful study of start-up at full load and loop stability.

#### 8.2.1.2.5 Input Capacitor Selection

The ceramic input capacitors provide a low impedance source to the regulator in addition to supplying the ripple current and isolating switching noise from other circuits. A minimum ceramic capacitance of 4.7 µF is required on the input of the LMQ664x0-Q1. This must be rated for at least the maximum input voltage that the application requires, preferably twice the maximum input voltage. This capacitance can be increased to help reduce input voltage ripple and maintain the input voltage during load transients. For this example, 2 × 4.7-µF, 50-V, X7R (or better) ceramic capacitor is chosen.

Using an electrolytic capacitor on the input in parallel with the ceramic capacitor is often desirable. This is especially true if long leads or traces are used to connect the input supply to the regulator. The moderate ESR of this capacitor can help damp any ringing on the input supply caused by the long power leads. The use of this additional capacitor also helps with voltage dips caused by input supplies with unusually high impedance.

Most of the input switching current passes through the ceramic input capacitor or capacitors. The approximate RMS value of this current can be calculated from Equation 7 and must be checked against the manufacturers' maximum ratings.

$$I_{RMS} \cong \frac{I_{OUT}}{2} \tag{7}$$

#### 8.2.1.2.6 $C_{BOOT}$

The LMQ664x0-Q1 has an integrated bootstrap 0.1-µF capacitor connected internally between the BOOT pin and the SW pin. This capacitor stores energy that is used to supply the gate drivers for the power MOSFETs. If needed, an additional high-quality ceramic capacitor can be added externally.

#### 8.2.1.2.7 VCC

The VCC pin is the output of the internal LDO used to supply the control circuits of the regulator. This output requires a 1-µF, 16-V ceramic capacitor connected from VCC to GND for proper operation. In general, this output must not be loaded with any external circuitry. However, this output can be used to supply the pullup for the power-good function (see Section 7.3.3). A value in the range of 10 kΩ to 100 kΩ is a good choice in this case. The nominal output voltage on VCC is 3.3 V; see the *Electrical Characteristics* for limits.

#### 8.2.1.2.8 $C_{FF}$ Selection

In some cases, a feedforward capacitor can be used across $R_{FBT}$ to improve the load transient response or improve the loop-phase margin. The *Optimizing Transient Response of Internally Compensated DC-DC Converters with Feedforward Capacitor* application report is helpful when experimenting with a feedforward capacitor.

Due to the nature of the feedback detect circuitry, the value of $C_{FF}$ must be limited to make sure that the desired output voltage is established when configuring for adjustable output voltages. Follow Equation 8 to make sure $C_{FF}$ remains below the maximum value.

$$C_{FF} < C_{OUT} \times \frac{\sqrt{V_{OUT}}}{1.2\ M\Omega} \tag{8}$$

#### 8.2.1.2.9 External UVLO

In some cases, an input UVLO level different than that provided internal to the device is needed. This can be accomplished by using the circuit shown in Figure 8-2. The input voltage at which the device turns on is designated as $V_{ON}$ while the turn-off voltage is $V_{OFF}$. First, a value for $R_{ENB}$ is chosen in the range of 10 kΩ to 100 kΩ, then Equation 9 and Equation 10 are used to calculate $R_{ENT}$ and $V_{OFF}$, respectively.


Copyright © 2025 Texas Instruments Incorporated

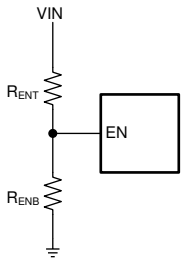



**Figure 8-2. Setup for External UVLO Application**

$$R_{ENT} = \left(\frac{V_{ON}}{V_{EN-VOUT}} - 1\right) \times R_{ENB} \quad (9)$$

$$V_{OFF} = V_{ON} \times \left(1 - \frac{V_{EN-HYS}}{V_{EN-VOUT}}\right) \quad (10)$$

where

- $V_{ON}$ is the $V_{IN}$ turn-on voltage.
- $V_{OFF}$ is the $V_{IN}$ turn-off voltage.

#### *8.2.1.2.10 Maximum Ambient Temperature*

As with any power conversion device, the LMQ664x0-Q1 dissipates internal power while operating. The effect of this power dissipation is to raise the internal temperature of the converter above ambient. The internal die temperature ($T_J$) is a function of the ambient temperature, the power loss, and the effective thermal resistance, $R_{\theta JA}$, of the device, and PCB combination. The maximum junction temperature for the LMQ664x0-Q1 must be limited to 150°C. This establishes a limit on the maximum device power dissipation and, therefore, the load current. Equation 11 shows the relationships between the important parameters. Seeing that larger ambient temperatures ($T_A$) and larger values of $R_{\theta JA}$ reduce the maximum available output current is easy. The converter efficiency can be estimated by using the curves provided in this data sheet. If the desired operating conditions cannot be found in one of the curves, interpolation can be used to estimate the efficiency. Alternatively, the EVM can be adjusted to match the desired application requirements and the efficiency can be measured directly. The correct value of $R_{\theta JA}$ is more difficult to estimate. For more information, refer to the *Semiconductor and IC Package Thermal Metrics* application report.

$$I_{OUT}\Big|_{MAX} = \frac{\left(T_J - T_A\right)}{R_{\theta JA}} \times \frac{\eta}{(1-\eta)} \times \frac{1}{V_{OUT}} \quad (11)$$

where

- η is the efficiency.

The effective $R_{\theta JA}$ is a critical parameter and depends on many factors such as the following:

- Power dissipation
- Air temperature and flow
- PCB area
- Copper heat-sink area
- Number of thermal vias under the package
- Adjacent component placement

The IC junction temperature can be estimated for a given operating condition using Equation 12.

$$T_J \cong T_A + R_{\theta JA} \times IC\ Power\ Loss \quad (12)$$

where

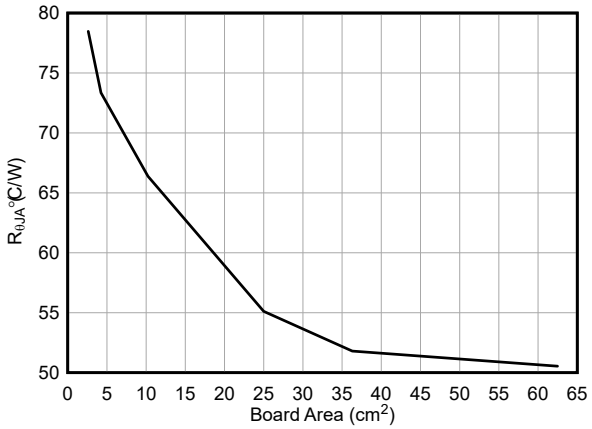
- $T_J$ is the IC junction temperature (°C).

Copyright © 2025 Texas Instruments Incorporated

- $T_A$ is the ambient temperature (°C).
- $R_{\theta JA}$ is the thermal resistance (°C/W).
- IC power loss is the power loss for the IC (W).

The IC power loss mentioned above is the overall power loss minus the loss that comes from the inductor DC resistance. The overall power loss can be approximated by using WEBENCH for a specific operating condition and temperature.

Figure 8-3 below is provided to estimate the thermal resistance of the IC for a particular board area.




The device operating conditions are as follows: 12-$V_{IN}$, 3.3-$V_{OUT}$, 3-A load, 2.2-MHz, 23ºC ambient. 4 layer board, GND plane on Mid-Layer One, 2.8-mil thick copper on each layer, see *LMQ66430-Q1 Buck Controller Evaluation Module User's Guide* for copper pattern and thermal vias.

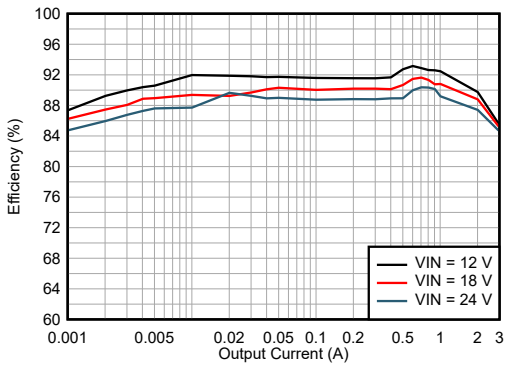
**Figure 8-3. $R_{\theta JA}$ vs Board Area**

Use the following resources as guides to excellent thermal PCB design and estimating $R_{\theta JA}$ for a given application environment:

- *Thermal Design by Insight not Hindsight* application report
- *A Guide to Board Layout for Best Thermal Resistance for Exposed Pad Packages* application report
- *Semiconductor and IC Package Thermal Metrics* application report
- *Thermal Design Made Simple with LM43603 and LM43602* application report
- *PowerPAD™ Thermally Enhanced Package* application report
- *PowerPAD™ Made Easy* application report
- *Using New Thermal Metrics* application report
- *PCB Thermal Calculator*

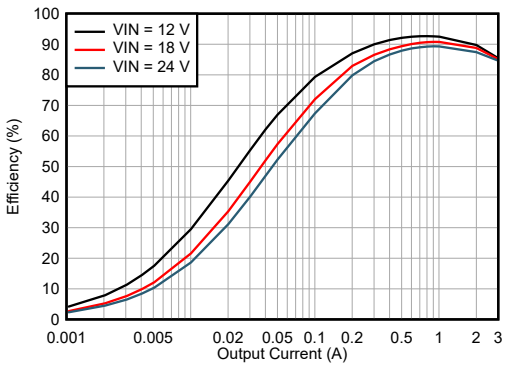

Copyright © 2025 Texas Instruments Incorporated

### 8.2.1.3 Application Curves



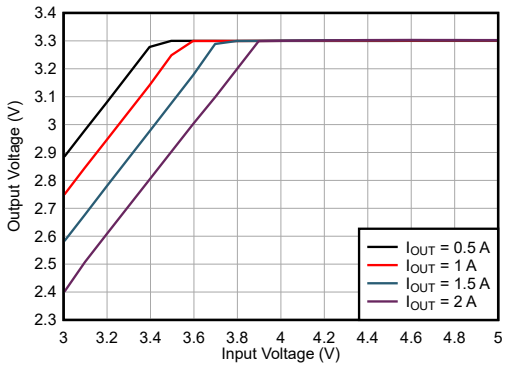

LMQ66430MC3 $V_{OUT}$ = 3.3 V 2.2 MHz (Auto) Fixed

**Figure 8-4. Efficiency**



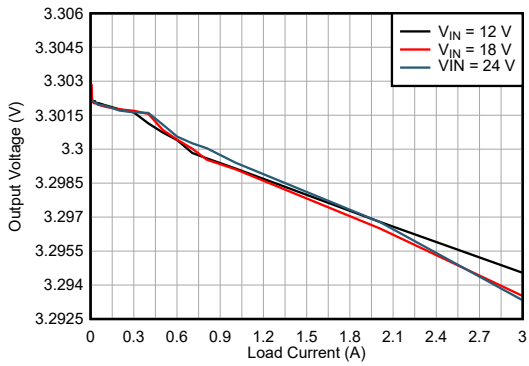

LMQ66430MC3 $V_{OUT}$ = 3.3 V 2.2 MHz (FPWM) Fixed

**Figure 8-5. Efficiency**



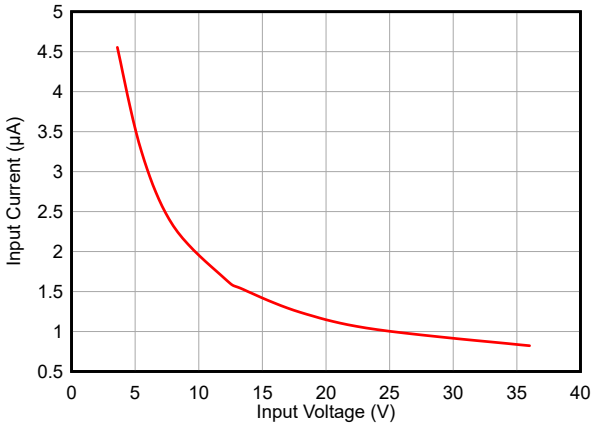

LMQ66430MC3 $V_{OUT}$ = 3.3 V 2.2 MHz (Auto) Fixed

**Figure 8-6. Dropout**



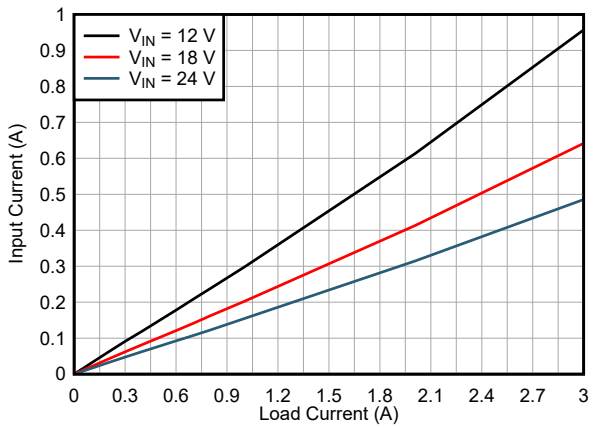

LMQ66430MC3 $V_{OUT}$ = 3.3 V 2.2 MHz (Auto) Fixed

**Figure 8-7. Line and Load Regulation**




LMQ66430MC3 $V_{OUT}$ = 3.3 V 2.2 MHz (Auto) Fixed No Load

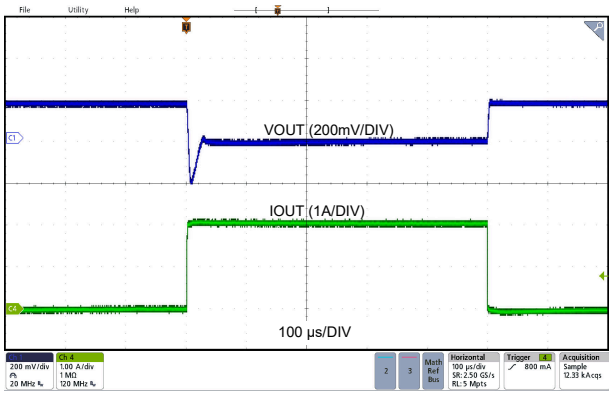
**Figure 8-8. Input Switching Current vs Input Voltage**




LMQ66430MC3 $V_{OUT}$ = 3.3 V 2.2 MHz (Auto) Fixed

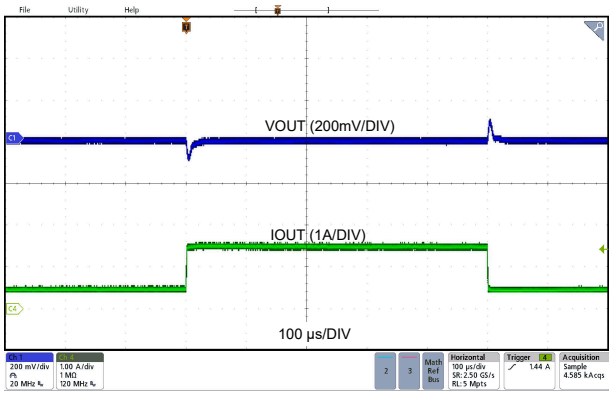
**Figure 8-9. Input Current vs Load Current**

Copyright © 2025 Texas Instruments Incorporated



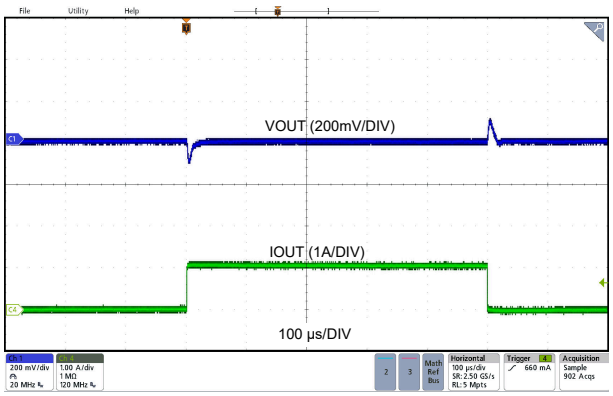

LMQ66430MC3 $V_{OUT}$ = 3.3 V 2.2 MHz (Auto)
0 A to 2 A,1 A / µs Fixed

**Figure 8-10. Load Transient**



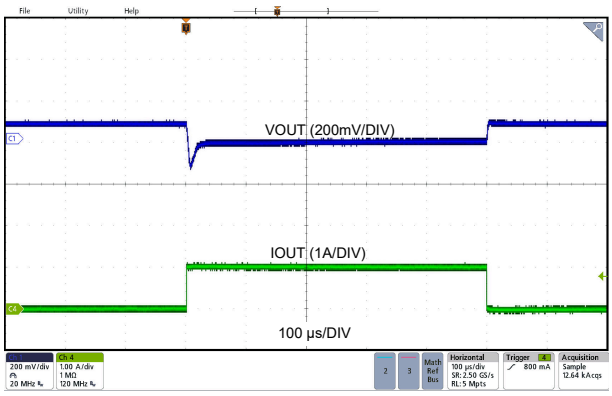

LMQ66430MC3 $V_{OUT}$ = 3.3 V 2.2 MHz (Auto)
0.5 A to 1.5 A,1 A / µs Fixed

**Figure 8-11. Load Transient**



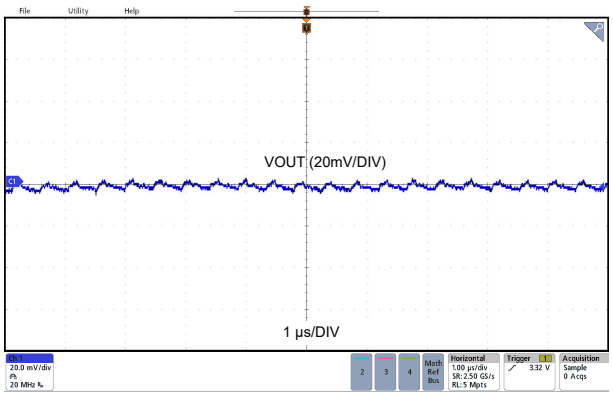

LMQ66430MC3 $V_{OUT}$ = 3.3 V 2.2 MHz (FPWM)
0 A to 1 A,1 A / µs Fixed

**Figure 8-12. Load Transient**



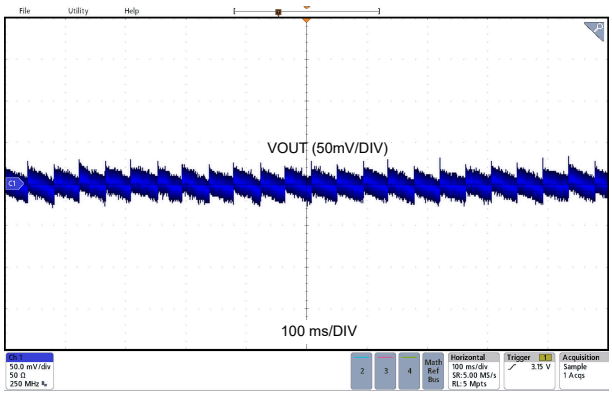

LMQ66430MC3 $V_{OUT}$ = 3.3 V 2.2 MHz (Auto)
0 A to 1 A,1 A / µs Fixed

**Figure 8-13. Load Transient**




LMQ66430MC3 $V_{OUT}$ = 3.3 V 2 A Load
Fixed

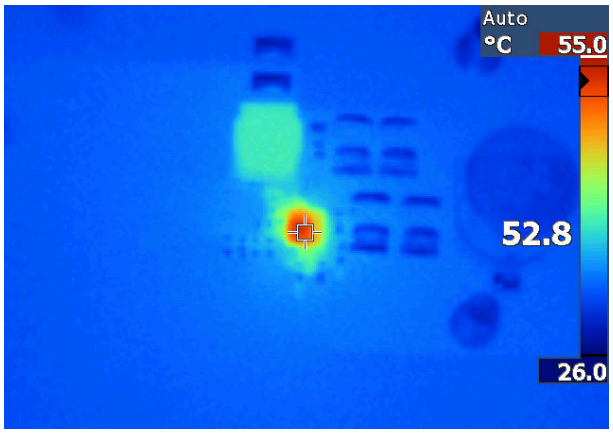
**Figure 8-14. Output Voltage Ripple**




LMQ66430MC3 $V_{OUT}$ = 3.3 V No Load
Fixed

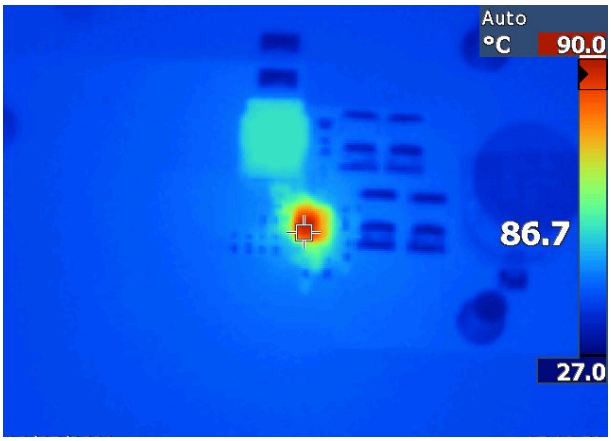
**Figure 8-15. Output Voltage Ripple**


Copyright © 2025 Texas Instruments Incorporated



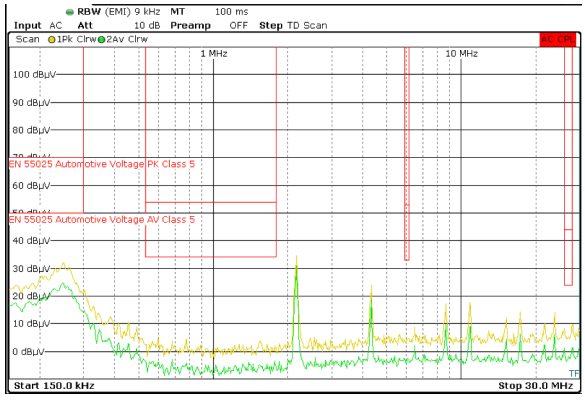

LMQ66430MC3 $V_{OUT}$ = 3.3 V Fixed 12 $V_{IN}$, 2 A, 2.2 MHz

**Figure 8-16. EVM Thermal Performance**



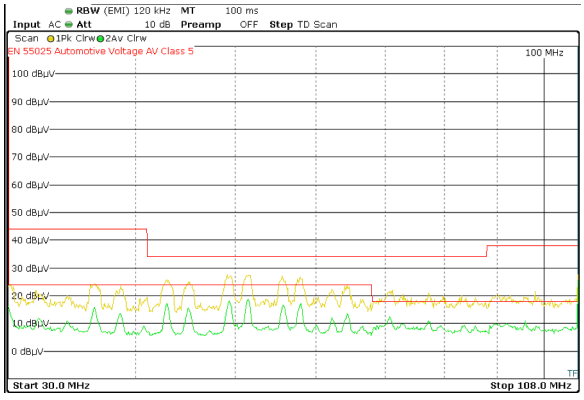

LMQ66430MC3 $V_{OUT}$ = 3.3 V Fixed 12 $V_{IN}$, 3 A, 2.2 MHz

**Figure 8-17. EVM Thermal Performance**



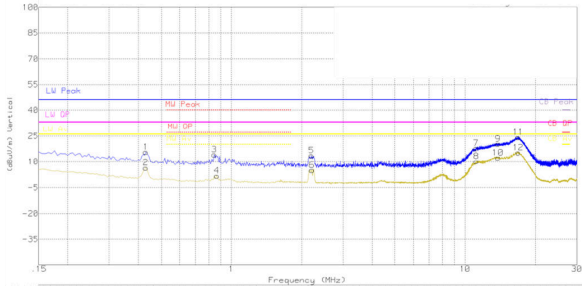

$V_{IN}$ = 12.5 V $V_{OUT}$ = 3.3 V Fsw = 2.2 MHz Load = 3 A

**Figure 8-18. CISPR 25 Class 5 Conducted EMI 150 kHz–30 MHz**
**Yellow: Peak Detect, Green: Average Detect**



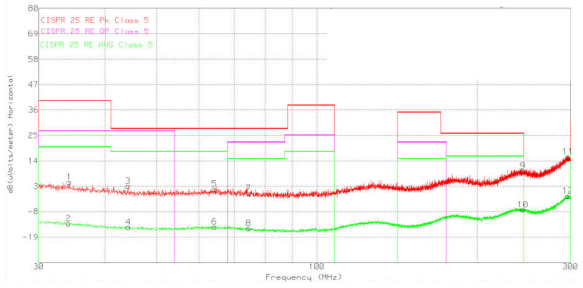

$V_{IN}$ = 12.5 V $V_{OUT}$ = 3.3 V Fsw = 2.2 MHz Load = 3 A

**Figure 8-19. CISPR 25 Class 5 Conducted EMI 30 MHz–108 MHz**
**Yellow: Peak Detect, Green: Average Detect**




$V_{IN}$ = 12.5 V $V_{OUT}$ = 3.3 V Fsw = 2.2 MHz Load = 3 A

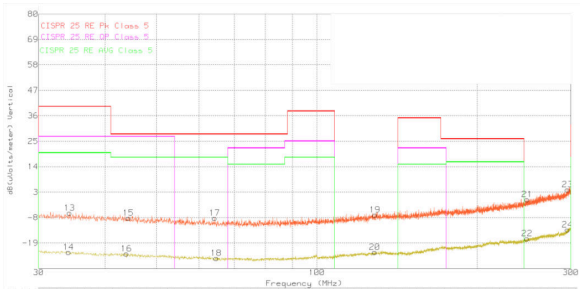
**Figure 8-20. CISPR 25 Class 5 Radiated EMI, Rod Antenna, 150 kHz–30 MHz**
**Blue: Peak Detect, Yellow: Average Detect**




$V_{IN}$ = 12.5 V $V_{OUT}$ = 3.3 V Fsw = 2.2 MHz Load = 3 A

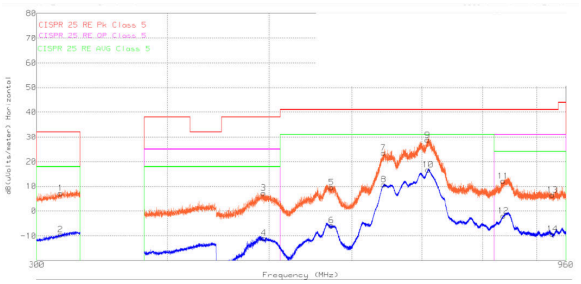
**Figure 8-21. CISPR 25 Class 5 Radiated EMI, Biconical Antenna, Horizontal Polarization, 30 MHz - 300 MHz**
**Red: Peak Detect, Green: Average Detect**

Copyright © 2025 Texas Instruments Incorporated



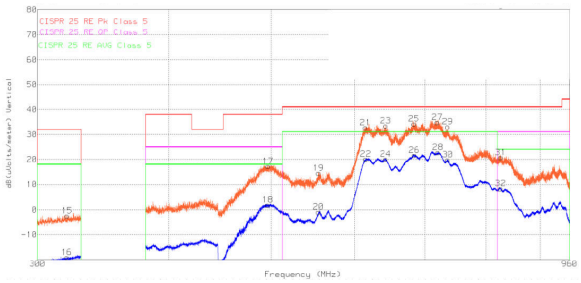
$V_{IN}$ = 12.5 V $V_{OUT}$ = 3.3 V Fsw = 2.2 MHz
Load = 3 A

**Figure 8-22. CISPR 25 Class 5 Radiated EMI, Biconical Antenna, Vertical Polarization, 30 MHz - 300 MHz**
**Orange: Peak Detect, Yellow: Average Detect**



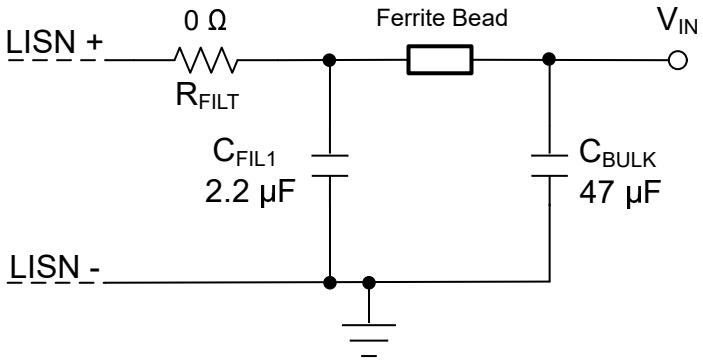
$V_{IN}$ = 12.5 V $V_{OUT}$ = 3.3 V Fsw = 2.2 MHz
Load = 3 A

**Figure 8-23. CISPR 25 Class 5 Radiated EMI, Log Antenna, Horizontal Polarization, 300 MHz - 960 MHz**
**Orange: Peak Detect, Blue: Average Detect**



$V_{IN}$ = 12.5 V $V_{OUT}$ = 3.3 V Fsw = 2.2 MHz
Load = 3 A

**Figure 8-24. CISPR 25 Class 5 Radiated EMI, Log Antenna, Vertical Polarization, 300 MHz - 960 MHz**
**Orange: Peak Detect, Blue: Average Detect**




Ferrite Bead Part Number
FBMH3225HM102NT

**Figure 8-25. Typical Input EMI Filter**


Copyright © 2025 Texas Instruments Incorporated

### 8.2.2 Design 2 - Automotive Synchronous Buck Regulator at 400 kHz

Figure 8-26 shows the schematic diagram of a synchronous buck regulator with an output voltage set at 5 V and a rated load current of 3 A. The MODE/SYNC pin is connected to a function generator to set the switching frequency to 400 kHz.

In this example, the nominal input voltage is 12 V and ranges from 7 V to 36 V.

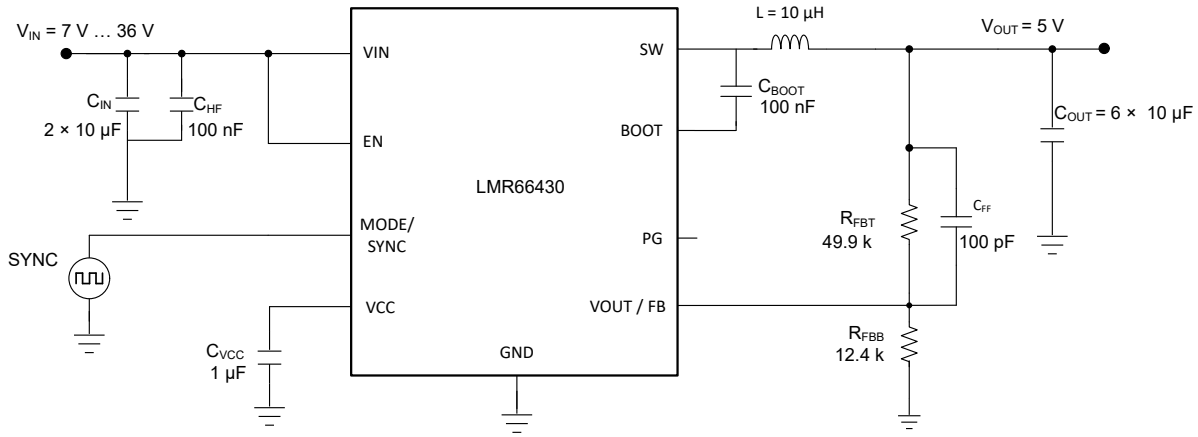



**Figure 8-26. Application Circuit 2 - 5 V (adjustable), 3 A, 400 kHz**

#### 8.2.2.1 Design Requirements

Table 8-9 describes the intended operating conditions for this design example.

**Table 8-9. Detailed Design Parameters**

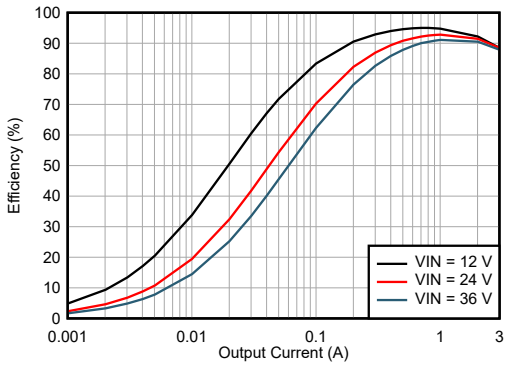
| DESIGN PARAMETER | EXAMPLE VALUE |
|---|---|
| Input voltage | 12 V (7 V to 36 V) |
| Output voltage | 5 V |
| Maximum output current | 0 A to 3 A |
| Switching frequency | 400 kHz |

#### 8.2.2.2 Detailed Design Procedure

Refer to Section 8.2.1.2 for detail related to component selection for this 400-kHz design.

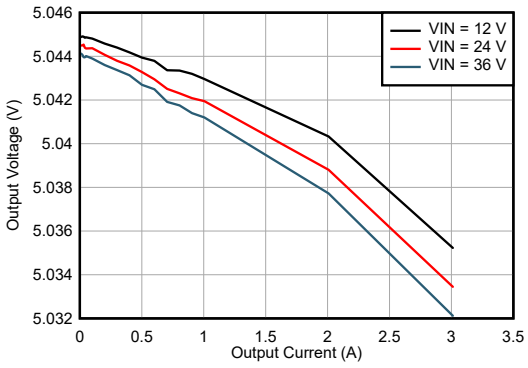
### 8.2.2.3 Application Curves

Unless otherwise specified, the following conditions apply: $V_{IN}$ = 12 V, $V_{OUT}$ = 5 V, $I_{OUT}$ = 3 A, $f_{SW}$ = 400 kHz, and $T_A$ = 25ºC. Figure 8-26 shows the circuit schematic with relevant component values.



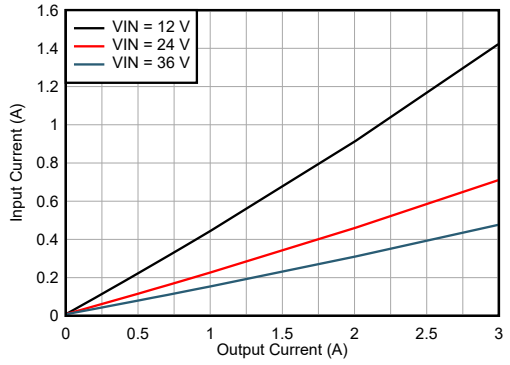

LMR66430MC3 $V_{OUT}$ = 5 V 400 kHz (FPWM) Adjustable

**Figure 8-27. Efficiency**



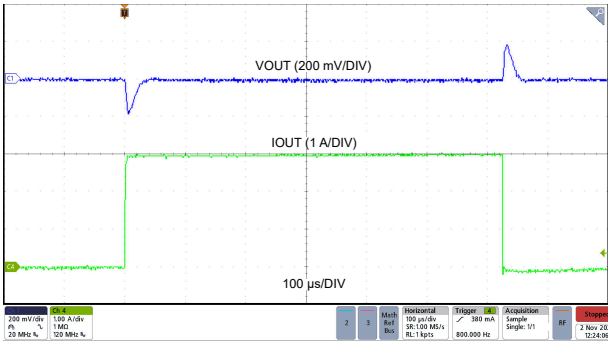

LMR66430MC3 $V_{OUT}$ = 5 V 400 kHz (FPWM) Adjustable

**Figure 8-28. Line and Load Regulation**



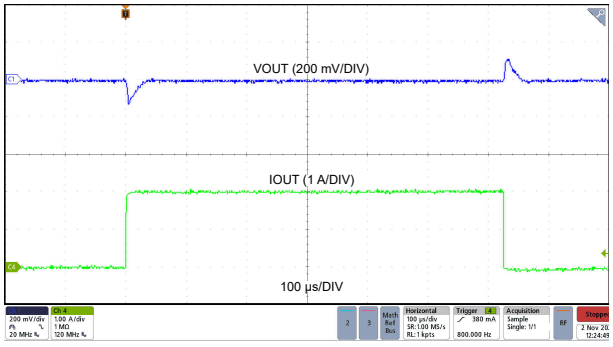

LMR66430MC3 $V_{OUT}$ = 5 V 400 kHz (FPWM) Adjustable

**Figure 8-29. Input Current vs Load Current**



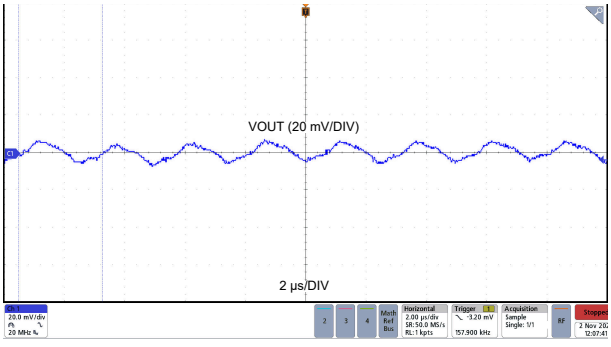

LMR66430MC3 $V_{OUT}$ = 5 V 400 kHz (FPWM)
0 A to 3 A,1 A / µs Adjustable

**Figure 8-30. Load Transient**




LMR66430MC3 $V_{OUT}$ = 5 V 400 kHz (FPWM)
0 A to 2 A,1 A / µs Adjustable

**Figure 8-31. Load Transient**




LMR66430MC3 $V_{OUT}$ = 5 V 3 A Load
Adjustable

**Figure 8-32. Output Voltage Ripple**


Copyright © 2025 Texas Instruments Incorporated

## 8.3 Best Design Practices

- Do not exceed the *Absolute Maximum Ratings*.
- Do not exceed the *Recommended Operating Conditions*.
- Do not exceed the *ESD Ratings*.
- Do not allow the EN input to float.
- Do not allow the output voltage to exceed the input voltage, nor go below ground.
- Follow all the guidelines and suggestions found in this data sheet before committing the design to production. TI application engineers are ready to help critique your design and PCB layout to help make your project a success.

## 8.4 Power Supply Recommendations

The characteristics of the input supply must be compatible with the *Specifications* found in this data sheet. In addition, the input supply must be capable of delivering the required input current to the loaded regulator. The average input current can be estimated with Equation 13.

$$I_{IN} = \frac{V_{OUT} \times I_{OUT}}{V_{IN} \times \eta} \quad (13)$$

where

- η is the efficiency.

If the regulator is connected to the input supply through long wires or PCB traces, special care is required to achieve good performance. The parasitic inductance and resistance of the input cables can have an adverse effect on the operation of the regulator. The parasitic inductance, in combination with the low-ESR, ceramic input capacitors, can form an underdamped resonant circuit, resulting in overvoltage transients at the input to the regulator. The parasitic resistance can cause the voltage at the VIN pin to dip whenever a load transient is applied to the output. If the application is operating close to the minimum input voltage, this dip can cause the regulator to momentarily shut down and reset. The best way to solve these kinds of issues is to limit the distance from the input supply to the regulator or plan to use an aluminum or tantalum input capacitor in parallel with the ceramics. The moderate ESR of these types of capacitors help dampen the input resonant circuit and reduce any overshoots. A value in the range of 20 µF to 100 µF is usually sufficient to provide input damping and help to hold the input voltage steady during large load transients.

Sometimes, for other system considerations, an input filter is used in front of the regulator. This input filter usage can lead to instability, as well as some of the effects mentioned above, unless designed carefully. The *AN-2162 Simple Success With Conducted EMI From DC/DC Converters User's Guide* provides helpful suggestions when designing an input filter for any switching regulator.

In some cases, a transient voltage suppressor (TVS) is used on the input of regulators. One class of this device has a *snap-back* characteristic (thyristor type). The use of a device with this type of characteristic is not recommended. When the TVS fires, the clamping voltage falls to a very low value. If this voltage is less than the output voltage of the regulator, the output capacitors discharge through the device back to the input. This uncontrolled current flow can damage the device.

## 8.5 Layout

### *8.5.1 Layout Guidelines*

The PCB layout of any DC/DC converter is critical to the optimal performance of the design. Poor PCB layout can disrupt the operation of an otherwise good schematic design. Even if the converter regulates correctly, bad PCB layout can mean the difference between a robust design and one that cannot be mass produced. Furthermore, to a great extent, the EMI performance of the regulator is dependent on the PCB layout. In a buck converter, the most critical PCB feature is the loop formed by the input capacitor or capacitors and power ground, as shown in Figure 8-33. This loop carries large transient currents that can cause large transient voltages when reacting with the trace inductance. These unwanted transient voltages disrupt the proper operation of the converter. Because of this, the traces in this loop must be wide and short, and the loop area as

Copyright © 2025 Texas Instruments Incorporated

small as possible to reduce the parasitic inductance. Figure 8-34 shows a recommended layout for the critical components of the LMQ664x0-Q1.

- *Place the input capacitors as close as possible to the VIN and GND terminals.*
- *Place bypass capacitor for VCC close to the VCC pin.* This capacitor must be placed close to the device and routed with short, wide traces to the VCC and GND pins.
- *If an external $C_{BOOT}$ capacitor is desired:* Place $C_{BOOT}$ close to the device with short/wide traces to the BOOT and SW pins.
- *Place the feedback divider as close as possible to the $V_{OUT}$ / FB pin of the device.* Place $R_{FBB}$, $R_{FBT}$, and $C_{FF}$, if used, physically close to the device. The connections to $V_{OUT}$ / FB and GND must be short and close to those pins on the device. The connection to $V_{OUT}$ can be somewhat longer. However, the latter trace must not be routed near any noise source (such as the SW node) that can capacitively couple into the feedback path of the regulator.
- *Use at least one ground plane in one of the middle layers.* This plane acts as a noise shield and as a heat dissipation path.
- *Provide wide paths for VIN, VOUT, and GND.* Making these paths as wide and direct as possible reduces any voltage drops on the input or output paths of the converter and maximizes efficiency.
- *Provide enough PCB area for proper heat-sinking.* As stated in Section 8.2.1.2.10, enough copper area must be used to make sure of low $R_{\theta JA}$, commensurate with the maximum load current and ambient temperature. The top and bottom PCB layers must be made with two-ounce copper and no less than one ounce. If the PCB design uses multiple copper layers (recommended), these thermal vias can also be connected to the inner layer heat-spreading ground planes.
- *Keep switch area small.* Keep the copper area connecting the SW pin to the inductor as short and wide as possible. At the same time, the total area of this node must be minimized to help reduce radiated EMI.

See the following PCB layout resources for additional important guidelines:

- *Layout Guidelines for Switching Power Supplies* application report
- *Simple Switcher PCB Layout Guidelines* application report
- *Construction Your Power Supply- Layout Considerations Seminar*
- *Low Radiated EMI Layout Made Simple with LM4360x and LM4600x* application report

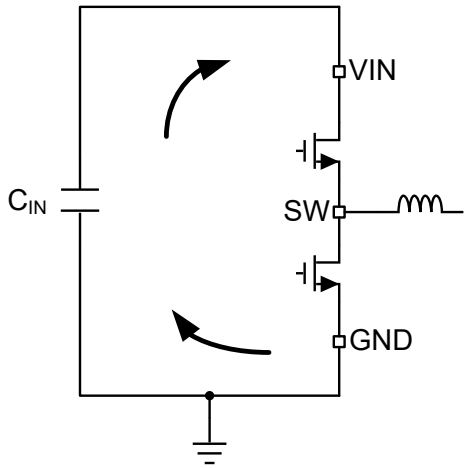



**Figure 8-33. Current Loops With Fast Edges**

#### 8.5.1.1 Ground and Thermal Considerations

As previously mentioned, TI recommends using one of the middle layers as a solid ground plane. A ground plane provides shielding for sensitive circuits and traces as well as a quiet reference potential for the control circuitry. Connect the GND pin to the ground planes using vias next to the bypass capacitors. The GND trace, as well as the VIN and SW traces, must be constrained to one side of the ground planes. The other side of the ground plane contains much less noise; use for sensitive routes.


Copyright © 2025 Texas Instruments Incorporated

TI recommends providing adequate device heat-sinking by having enough copper near the GND pin. See Figure 8-34 for example layout. Use as much copper as possible, for system ground plane, on the top and bottom layers for the best heat dissipation. Use a four-layer board with the copper thickness for the four layers, starting from the top as: 2 oz / 1 oz / 1 oz / 2 oz. A four-layer board with enough copper thickness, and proper layout, provides low current conduction impedance, proper shielding, and lower thermal resistance.

### *8.5.2 Layout Example*

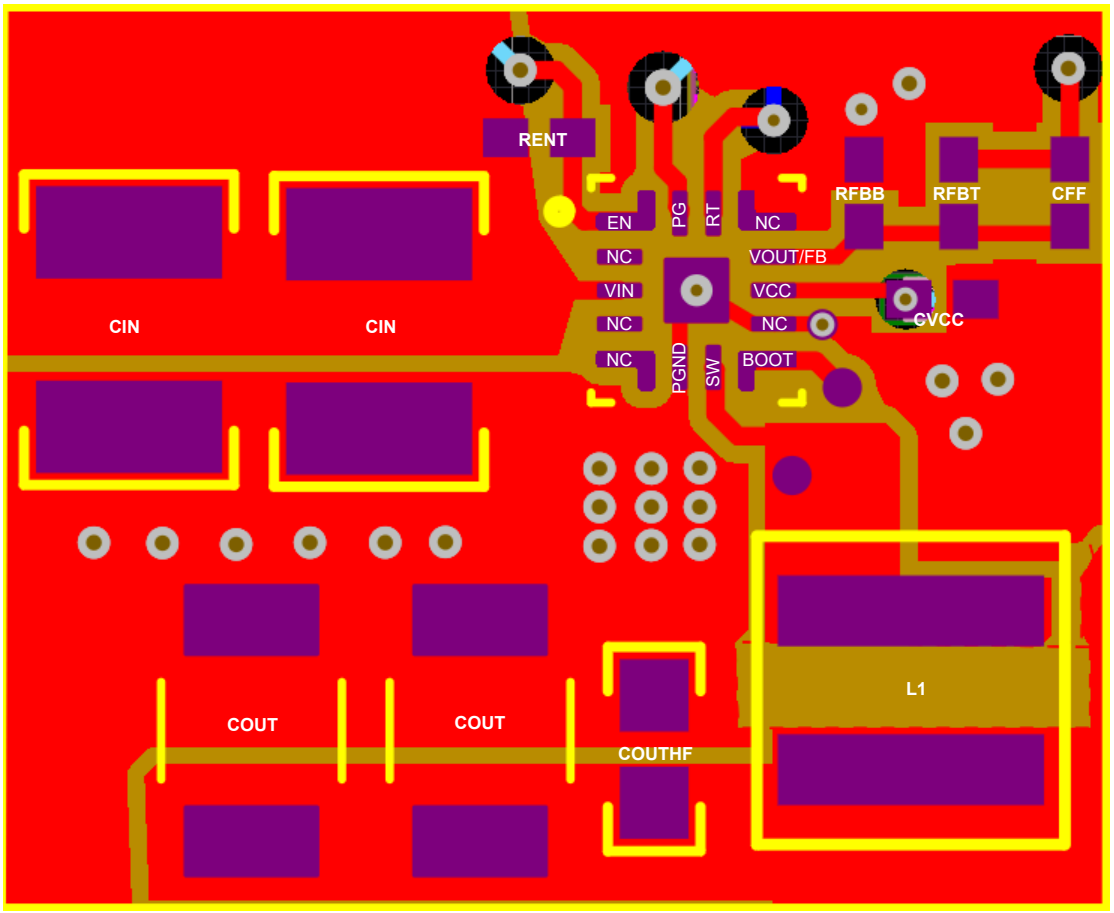



**Figure 8-34. Example Layout**

## 9 Device and Documentation Support

### 9.1 Device Support

#### *9.1.1 Third-Party Products Disclaimer*

TI'S PUBLICATION OF INFORMATION REGARDING THIRD-PARTY PRODUCTS OR SERVICES DOES NOT CONSTITUTE AN ENDORSEMENT REGARDING THE SUITABILITY OF SUCH PRODUCTS OR SERVICES OR A WARRANTY, REPRESENTATION OR ENDORSEMENT OF SUCH PRODUCTS OR SERVICES, EITHER ALONE OR IN COMBINATION WITH ANY TI PRODUCT OR SERVICE.

#### *9.1.2 Device Nomenclature*

Figure 9-1 shows the device naming nomenclature of the LMQ664x0-Q1. See Section 4 for the availability of each variant. Contact TI sales representatives or on TI's E2E forum for detail and availability of other options; minimum order quantities apply.

Copyright © 2025 Texas Instruments Incorporated

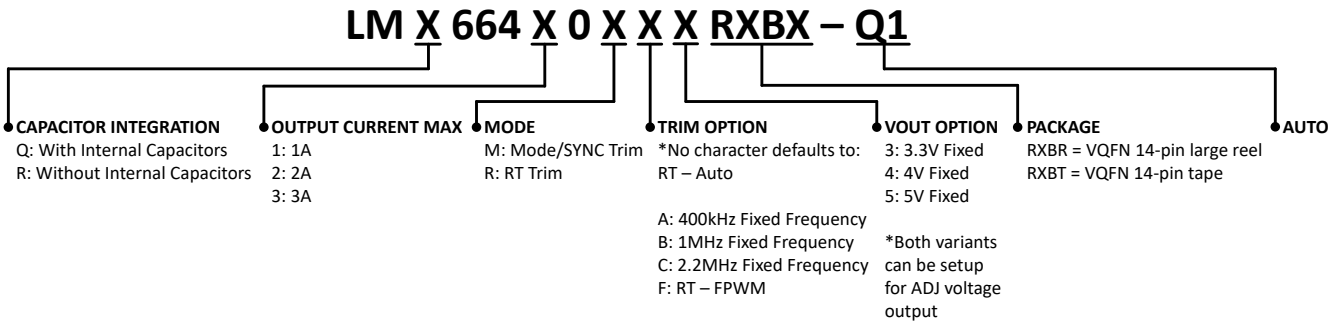



**Figure 9-1. Device Naming Nomenclature**

## 9.2 Documentation Support

### *9.2.1 Related Documentation*

For related documentation see the following:

- Texas Instruments, *Thermal Design by Insight not Hindsight* application report
- Texas Instruments, *A Guide to Board Layout for Best Thermal Resistance for Exposed Pad Packages* application report
- Texas Instruments, *Semiconductor and IC Package Thermal Metrics* application report
- Texas Instruments, *Thermal Design Made Simple with LM43603 and LM43602* application report
- Texas Instruments, *PowerPAD™ Thermally Enhanced Package* application report
- Texas Instruments, *PowerPAD™ Made Easy* application report
- Texas Instruments, *Using New Thermal Metrics* application report
- Texas Instruments, *Layout Guidelines for Switching Power Supplies* application report
- Texas Instruments, *Simple Switcher PCB Layout Guidelines* application report
- Texas Instruments, *Construction Your Power Supply- Layout Considerations Seminar*
- Texas Instruments, *Low Radiated EMI Layout Made Simple with LM4360x and LM4600x* application report

## 9.3 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

## 9.4 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

## 9.5 Trademarks

HotRod™, PowerPAD™, and TI E2E™ are trademarks of Texas Instruments.
All trademarks are the property of their respective owners.

## 9.6 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

## 9.7 Glossary

TI Glossary — This glossary lists and explains terms, acronyms, and definitions.


Copyright © 2025 Texas Instruments Incorporated

## 10 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

| Changes from Revision D (November 2024) to Revision E (December 2025) | Page |
|---|---|
| • Added ZEN 2 switcher technology branding on the first page of the document | 1 |

| Changes from Revision C (December 2023) to Revision D (November 2024) | Page |
|---|---|
| • Changed the switching frequency, Fsw, for LMQ66430MA3RXBRQ1 and LMQ66430MA5RXBRQ1 in the *Device Comparison Table* from 2.2MHz to 400kHz | 3 |

Copyright © 2025 Texas Instruments Incorporated

## 11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.


Copyright © 2025 Texas Instruments Incorporated

## PACKAGING INFORMATION

| Orderable part number | Status (1) | Material type (2) | Package \| Pins | Package qty \| Carrier | RoHS (3) | Lead finish/ Ball material (4) | MSL rating/ Peak reflow (5) | Op temp (°C) | Part marking (6) |
|---|---|---|---|---|---|---|---|---|---|
| LMQ66410MA3RXBRQ1 | Active | Production | VQFN-FCRLF (RXB) \| 14 | 3000 \| LARGE T&R | Yes | NIPDAU | Level-2-260C-1 YEAR | -40 to 150 | 1MA3Q |
| LMQ66410MA3RXBRQ1.A | Active | Production | VQFN-FCRLF (RXB) \| 14 | 3000 \| LARGE T&R | Yes | NIPDAU | Level-2-260C-1 YEAR | -40 to 150 | 1MA3Q |
| LMQ66410MA3RXBRQ1.B | Active | Production | VQFN-FCRLF (RXB) \| 14 | 3000 \| LARGE T&R | - | Call TI | Call TI | -40 to 150 | |
| LMQ66410MA5RXBRQ1 | Active | Production | VQFN-FCRLF (RXB) \| 14 | 3000 \| LARGE T&R | Yes | NIPDAU | Level-2-260C-1 YEAR | -40 to 150 | 1MA5Q |
| LMQ66410MA5RXBRQ1.A | Active | Production | VQFN-FCRLF (RXB) \| 14 | 3000 \| LARGE T&R | Yes | NIPDAU | Level-2-260C-1 YEAR | -40 to 150 | 1MA5Q |
| LMQ66410MA5RXBRQ1.B | Active | Production | VQFN-FCRLF (RXB) \| 14 | 3000 \| LARGE T&R | - | Call TI | Call TI | -40 to 150 | |
| LMQ66410MC3RXBRQ1 | Active | Production | VQFN-FCRLF (RXB) \| 14 | 3000 \| LARGE T&R | Yes | NIPDAU | Level-2-260C-1 YEAR | -40 to 150 | 1MC3Q |
| LMQ66410MC3RXBRQ1.A | Active | Production | VQFN-FCRLF (RXB) \| 14 | 3000 \| LARGE T&R | Yes | NIPDAU | Level-2-260C-1 YEAR | -40 to 150 | 1MC3Q |
| LMQ66410MC3RXBRQ1.B | Active | Production | VQFN-FCRLF (RXB) \| 14 | 3000 \| LARGE T&R | - | Call TI | Call TI | -40 to 150 | |
| LMQ66410MC5RXBRQ1 | Active | Production | VQFN-FCRLF (RXB) \| 14 | 3000 \| LARGE T&R | Yes | NIPDAU | Level-2-260C-1 YEAR | -40 to 150 | 1MC5Q |
| LMQ66410MC5RXBRQ1.A | Active | Production | VQFN-FCRLF (RXB) \| 14 | 3000 \| LARGE T&R | Yes | NIPDAU | Level-2-260C-1 YEAR | -40 to 150 | 1MC5Q |
| LMQ66410MC5RXBRQ1.B | Active | Production | VQFN-FCRLF (RXB) \| 14 | 3000 \| LARGE T&R | - | Call TI | Call TI | -40 to 150 | |
| LMQ66420MA3RXBRQ1 | Active | Production | VQFN-FCRLF (RXB) \| 14 | 3000 \| LARGE T&R | Yes | NIPDAU | Level-2-260C-1 YEAR | -40 to 150 | 2MA3Q |
| LMQ66420MA3RXBRQ1.A | Active | Production | VQFN-FCRLF (RXB) \| 14 | 3000 \| LARGE T&R | Yes | NIPDAU | Level-2-260C-1 YEAR | -40 to 150 | 2MA3Q |
| LMQ66420MA3RXBRQ1.B | Active | Production | VQFN-FCRLF (RXB) \| 14 | 3000 \| LARGE T&R | - | Call TI | Call TI | -40 to 150 | |
| LMQ66420MA5RXBRQ1 | Active | Production | VQFN-FCRLF (RXB) \| 14 | 3000 \| LARGE T&R | Yes | NIPDAU | Level-2-260C-1 YEAR | -40 to 150 | 2MA5Q |

| Orderable part number | Status (1) | Material type (2) | Package \| Pins | Package qty \| Carrier | RoHS (3) | Lead finish/ Ball material (4) | MSL rating/ Peak reflow (5) | Op temp (°C) | Part marking (6) |
|---|---|---|---|---|---|---|---|---|---|
| LMQ66420MA5RXBRQ1.A | Active | Production | VQFN-FCRLF (RXB) \| 14 | 3000 \| LARGE T&R | Yes | NIPDAU | Level-2-260C-1 YEAR | -40 to 150 | 2MA5Q |
| LMQ66420MA5RXBRQ1.B | Active | Production | VQFN-FCRLF (RXB) \| 14 | 3000 \| LARGE T&R | - | Call TI | Call TI | -40 to 150 | |
| LMQ66420MC3RXBRQ1 | Active | Production | VQFN-FCRLF (RXB) \| 14 | 3000 \| LARGE T&R | Yes | NIPDAU | Level-2-260C-1 YEAR | -40 to 150 | 2MC3Q |
| LMQ66420MC3RXBRQ1.A | Active | Production | VQFN-FCRLF (RXB) \| 14 | 3000 \| LARGE T&R | Yes | NIPDAU | Level-2-260C-1 YEAR | -40 to 150 | 2MC3Q |
| LMQ66420MC3RXBRQ1.B | Active | Production | VQFN-FCRLF (RXB) \| 14 | 3000 \| LARGE T&R | - | Call TI | Call TI | -40 to 150 | |
| LMQ66420MC5RXBRQ1 | Active | Production | VQFN-FCRLF (RXB) \| 14 | 3000 \| LARGE T&R | Yes | NIPDAU | Level-2-260C-1 YEAR | -40 to 150 | 2MC5Q |
| LMQ66420MC5RXBRQ1.A | Active | Production | VQFN-FCRLF (RXB) \| 14 | 3000 \| LARGE T&R | Yes | NIPDAU | Level-2-260C-1 YEAR | -40 to 150 | 2MC5Q |
| LMQ66420MC5RXBRQ1.B | Active | Production | VQFN-FCRLF (RXB) \| 14 | 3000 \| LARGE T&R | - | Call TI | Call TI | -40 to 150 | |
| LMQ66430MA3RXBRQ1 | Active | Production | VQFN-FCRLF (RXB) \| 14 | 3000 \| LARGE T&R | Yes | NIPDAU | Level-2-260C-1 YEAR | -40 to 150 | 3MA3Q |
| LMQ66430MA3RXBRQ1.A | Active | Production | VQFN-FCRLF (RXB) \| 14 | 3000 \| LARGE T&R | Yes | NIPDAU | Level-2-260C-1 YEAR | -40 to 150 | 3MA3Q |
| LMQ66430MA3RXBRQ1.B | Active | Production | VQFN-FCRLF (RXB) \| 14 | 3000 \| LARGE T&R | - | Call TI | Call TI | -40 to 150 | |
| LMQ66430MA5RXBRQ1 | Active | Production | VQFN-FCRLF (RXB) \| 14 | 3000 \| LARGE T&R | Yes | NIPDAU | Level-2-260C-1 YEAR | -40 to 150 | 3MA5Q |
| LMQ66430MA5RXBRQ1.A | Active | Production | VQFN-FCRLF (RXB) \| 14 | 3000 \| LARGE T&R | Yes | NIPDAU | Level-2-260C-1 YEAR | -40 to 150 | 3MA5Q |
| LMQ66430MA5RXBRQ1.B | Active | Production | VQFN-FCRLF (RXB) \| 14 | 3000 \| LARGE T&R | - | Call TI | Call TI | -40 to 150 | |
| LMQ66430MC3RXBRQ1 | Active | Production | VQFN-FCRLF (RXB) \| 14 | 3000 \| LARGE T&R | Yes | NIPDAU | Level-2-260C-1 YEAR | -40 to 150 | 3MC3Q |
| LMQ66430MC3RXBRQ1.A | Active | Production | VQFN-FCRLF (RXB) \| 14 | 3000 \| LARGE T&R | Yes | NIPDAU | Level-2-260C-1 YEAR | -40 to 150 | 3MC3Q |
| LMQ66430MC3RXBRQ1.B | Active | Production | VQFN-FCRLF (RXB) \| 14 | 3000 \| LARGE T&R | - | Call TI | Call TI | -40 to 150 | |

| Orderable part number | Status (1) | Material type (2) | Package \| Pins | Package qty \| Carrier | RoHS (3) | Lead finish/ Ball material (4) | MSL rating/ Peak reflow (5) | Op temp (°C) | Part marking (6) |
|---|---|---|---|---|---|---|---|---|---|
| LMQ66430MC5RXBRQ1 | Active | Production | VQFN-FCRLF (RXB) \| 14 | 3000 \| LARGE T&R | Yes | NIPDAU | Level-2-260C-1 YEAR | -40 to 150 | 3MC5Q |
| LMQ66430MC5RXBRQ1.A | Active | Production | VQFN-FCRLF (RXB) \| 14 | 3000 \| LARGE T&R | Yes | NIPDAU | Level-2-260C-1 YEAR | -40 to 150 | 3MC5Q |
| LMQ66430MC5RXBRQ1.B | Active | Production | VQFN-FCRLF (RXB) \| 14 | 3000 \| LARGE T&R | - | Call TI | Call TI | -40 to 150 | |

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

**Important Information and Disclaimer:**The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

**OTHER QUALIFIED VERSIONS OF LMQ66410-Q1, LMQ66420-Q1, LMQ66430-Q1 :**

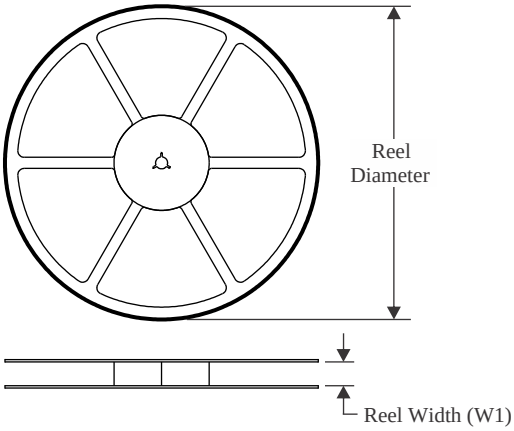
- Catalog : LMQ66410, LMQ66420, LMQ66430

NOTE: Qualified Version Definitions:

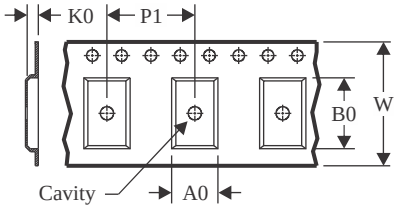
- Catalog - TI's standard catalog product

## TAPE AND REEL INFORMATION

**REEL DIMENSIONS**

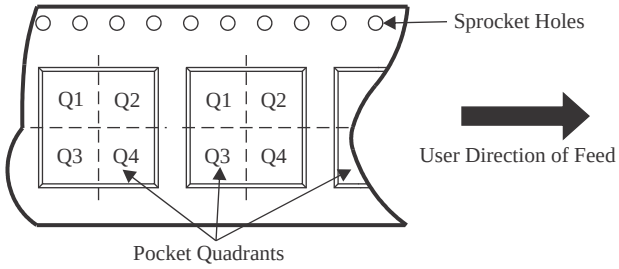



**TAPE DIMENSIONS**




| | |
|---|---|
| A0 | Dimension designed to accommodate the component width |
| B0 | Dimension designed to accommodate the component length |
| K0 | Dimension designed to accommodate the component thickness |
| W | Overall width of the carrier tape |
| P1 | Pitch between successive cavity centers |

**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**

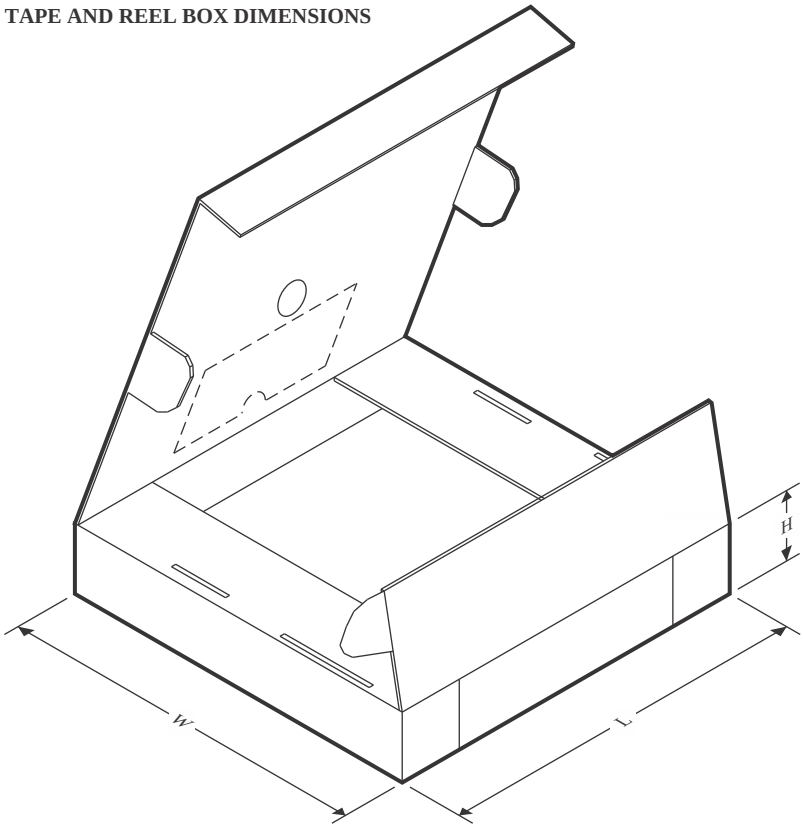



*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| LMQ66410MA3RXBRQ1 | VQFN-FCRLF | RXB | 14 | 3000 | 330.0 | 12.4 | 2.9 | 2.9 | 1.3 | 8.0 | 12.0 | Q2 |
| LMQ66410MA5RXBRQ1 | VQFN-FCRLF | RXB | 14 | 3000 | 330.0 | 12.4 | 2.9 | 2.9 | 1.3 | 8.0 | 12.0 | Q2 |
| LMQ66410MC3RXBRQ1 | VQFN-FCRLF | RXB | 14 | 3000 | 330.0 | 12.4 | 2.9 | 2.9 | 1.3 | 8.0 | 12.0 | Q2 |
| LMQ66410MC5RXBRQ1 | VQFN-FCRLF | RXB | 14 | 3000 | 330.0 | 12.4 | 2.9 | 2.9 | 1.3 | 8.0 | 12.0 | Q2 |
| LMQ66420MA3RXBRQ1 | VQFN-FCRLF | RXB | 14 | 3000 | 330.0 | 12.4 | 2.9 | 2.9 | 1.3 | 8.0 | 12.0 | Q2 |
| LMQ66420MA5RXBRQ1 | VQFN-FCRLF | RXB | 14 | 3000 | 330.0 | 12.4 | 2.9 | 2.9 | 1.3 | 8.0 | 12.0 | Q2 |
| LMQ66420MC3RXBRQ1 | VQFN-FCRLF | RXB | 14 | 3000 | 330.0 | 12.4 | 2.9 | 2.9 | 1.3 | 8.0 | 12.0 | Q2 |
| LMQ66420MC5RXBRQ1 | VQFN-FCRLF | RXB | 14 | 3000 | 330.0 | 12.4 | 2.9 | 2.9 | 1.3 | 8.0 | 12.0 | Q2 |
| LMQ66430MA3RXBRQ1 | VQFN-FCRLF | RXB | 14 | 3000 | 330.0 | 12.4 | 2.9 | 2.9 | 1.3 | 8.0 | 12.0 | Q2 |

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| LMQ66430MA5RXBRQ1 | VQFN-FCRLF | RXB | 14 | 3000 | 330.0 | 12.4 | 2.9 | 2.9 | 1.3 | 8.0 | 12.0 | Q2 |
| LMQ66430MC3RXBRQ1 | VQFN-FCRLF | RXB | 14 | 3000 | 330.0 | 12.4 | 2.9 | 2.9 | 1.3 | 8.0 | 12.0 | Q2 |
| LMQ66430MC5RXBRQ1 | VQFN-FCRLF | RXB | 14 | 3000 | 330.0 | 12.4 | 2.9 | 2.9 | 1.3 | 8.0 | 12.0 | Q2 |

TAPE AND REEL BOX DIMENSIONS




*All dimensions are nominal

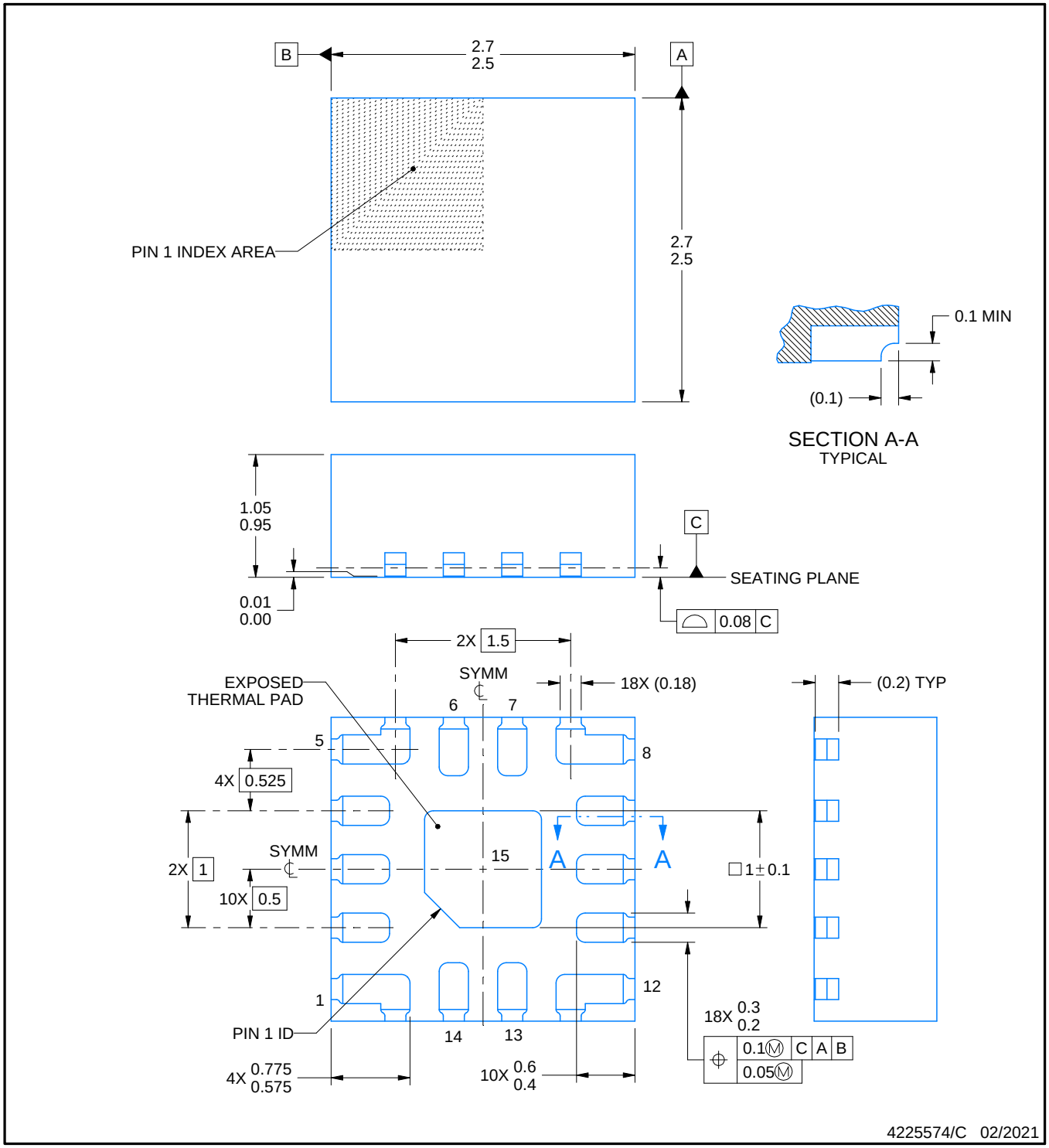
| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|---|---|---|---|---|---|---|---|
| LMQ66410MA3RXBRQ1 | VQFN-FCRLF | RXB | 14 | 3000 | 367.0 | 367.0 | 35.0 |
| LMQ66410MA5RXBRQ1 | VQFN-FCRLF | RXB | 14 | 3000 | 367.0 | 367.0 | 35.0 |
| LMQ66410MC3RXBRQ1 | VQFN-FCRLF | RXB | 14 | 3000 | 367.0 | 367.0 | 35.0 |
| LMQ66410MC5RXBRQ1 | VQFN-FCRLF | RXB | 14 | 3000 | 367.0 | 367.0 | 35.0 |
| LMQ66420MA3RXBRQ1 | VQFN-FCRLF | RXB | 14 | 3000 | 367.0 | 367.0 | 35.0 |
| LMQ66420MA5RXBRQ1 | VQFN-FCRLF | RXB | 14 | 3000 | 367.0 | 367.0 | 35.0 |
| LMQ66420MC3RXBRQ1 | VQFN-FCRLF | RXB | 14 | 3000 | 367.0 | 367.0 | 35.0 |
| LMQ66420MC5RXBRQ1 | VQFN-FCRLF | RXB | 14 | 3000 | 367.0 | 367.0 | 35.0 |
| LMQ66430MA3RXBRQ1 | VQFN-FCRLF | RXB | 14 | 3000 | 367.0 | 367.0 | 35.0 |
| LMQ66430MA5RXBRQ1 | VQFN-FCRLF | RXB | 14 | 3000 | 367.0 | 367.0 | 35.0 |
| LMQ66430MC3RXBRQ1 | VQFN-FCRLF | RXB | 14 | 3000 | 367.0 | 367.0 | 35.0 |
| LMQ66430MC5RXBRQ1 | VQFN-FCRLF | RXB | 14 | 3000 | 367.0 | 367.0 | 35.0 |

# PACKAGE OUTLINE

## RXB0014A

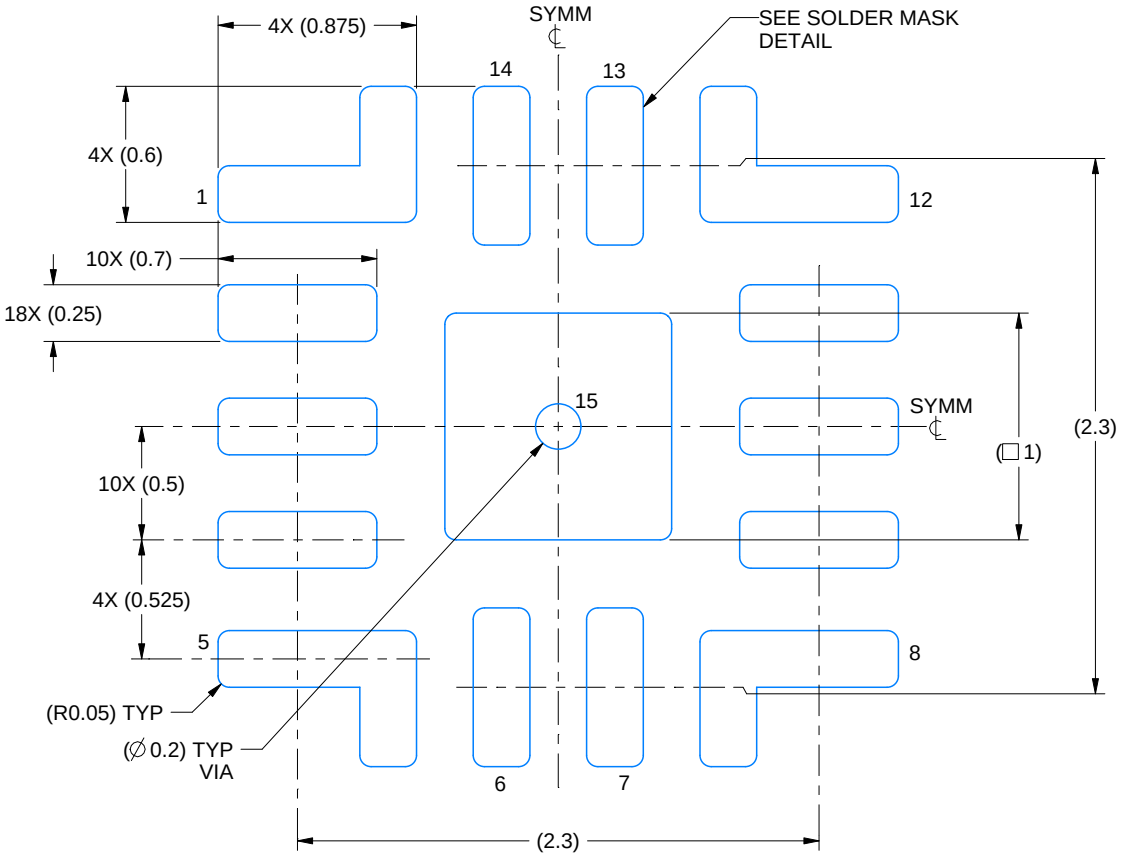
## VQFN-FCRLF - 1.05 mm max height

PLASTIC QUAD FLATPACK - NO LEAD

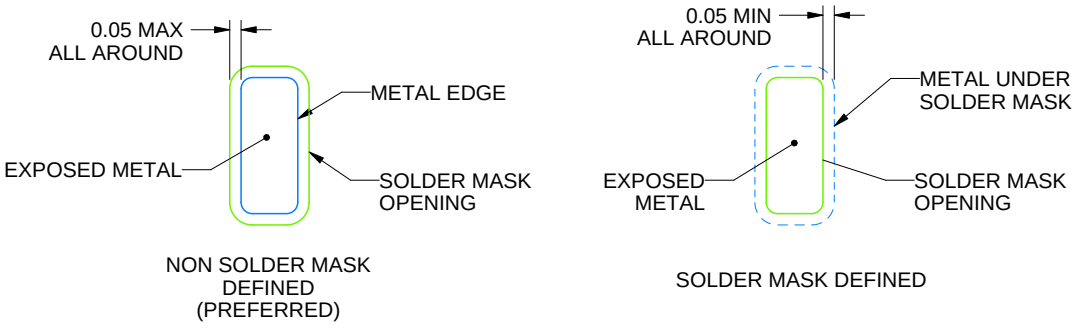



NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.




LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 30X




SOLDER MASK DETAILS

4225574/C 02/2021

NOTES: (continued)

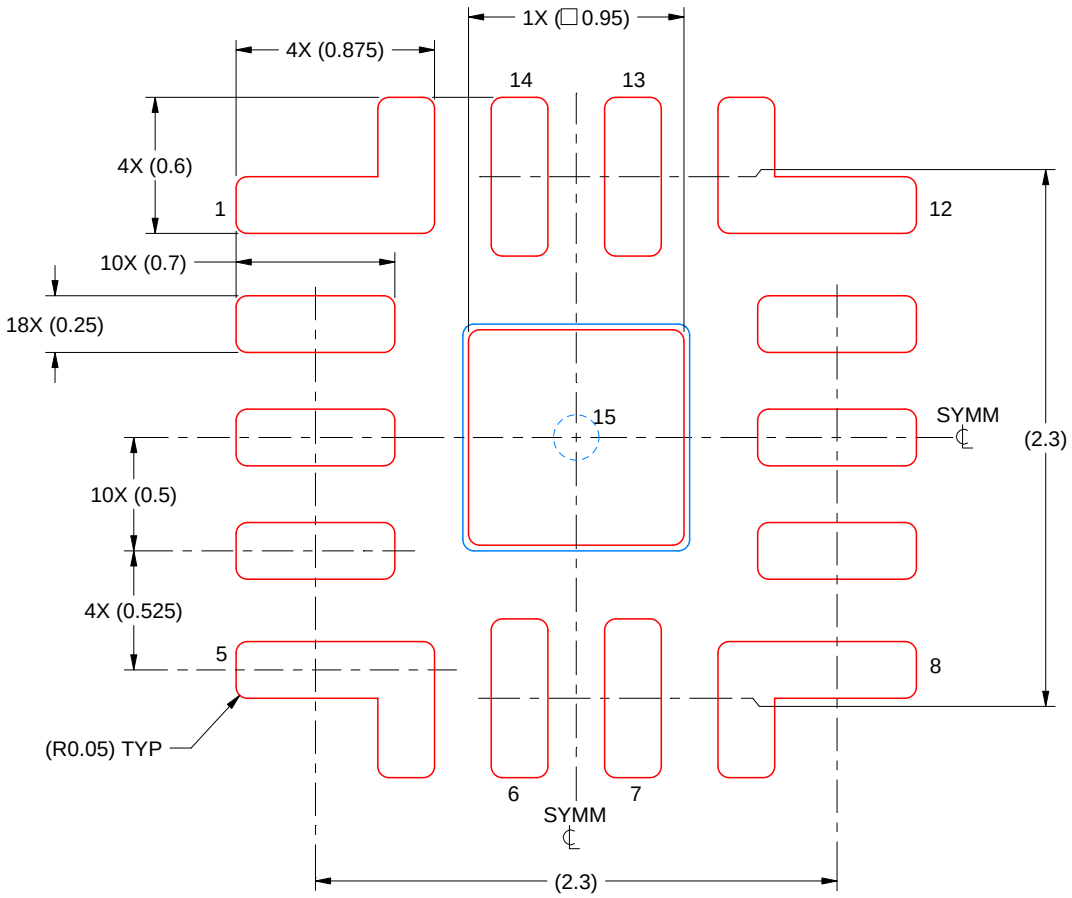
4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.

# EXAMPLE STENCIL DESIGN

## RXB0014A

## VQFN-FCRLF - 1.05 mm max height

PLASTIC QUAD FLATPACK - NO LEAD




SOLDER PASTE EXAMPLE
BASED ON 0.125 MM THICK STENCIL
SCALE: 30X

EXPOSED PAD 15
90% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE

4225574/C 02/2021

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

# IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATASHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES “AS IS” AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, regulatory or other requirements.

These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you fully indemnify TI and its representatives against any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI’s products are provided subject to TI’s Terms of Sale, TI’s General Quality Guidelines, or other applicable terms available either on ti.com or provided in conjunction with such TI products. TI’s provision of these resources does not expand or otherwise alter TI’s applicable warranties or warranty disclaimers for TI products. Unless TI explicitly designates a product as custom or customer-specified, TI products are standard, catalog, general purpose devices.

TI objects to and rejects any additional or different terms you may propose.

Copyright © 2025, Texas Instruments Incorporated

Last updated 10/2025