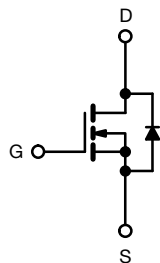


Power MOSFET

TO-220 FULLPAK


N-Channel MOSFET

FEATURES

- Ultra low gate charge
- Reduced gate drive requirement
- Enhanced 30 V V_{GS} rating
- Isolated package
- High voltage isolation = 2.5 kV_{RMS} (t = 60 s, f = 60 Hz)
- Sink to lead creepage distance = 4.8 mm
- Repetitive avalanche rated
- Material categorization: for definitions of compliance please see www.vishay.com/doc?99912


RoHS
COMPLIANT

DESCRIPTION

This series of low charge power MOSFETs achieve significantly lower gate charge over conventional MOSFETs. Utilizing advanced power MOSFETs technology, the device improvements allow for reduced gate drive requirements, faster switching speeds and increased total system savings. These device improvements combined with the proven ruggedness and reliability that are characteristic of Power MOSFETs offer the designer a new standard in power transistors for switching applications.

The TO-220 FULLPAK eliminates the need for additional insulating hardware. The molding compound used provides a high isolation capability and low thermal resistance between the tab and external heatsink.

ORDERING INFORMATION

Package	TO-220 FULLPAK
Lead (Pb)-free	IRFI740GLCPbF

ABSOLUTE MAXIMUM RATINGS ($T_C = 25^\circ\text{C}$, unless otherwise noted)

PARAMETER			SYMBOL	LIMIT	UNIT
Drain-source voltage			V _{DS}	400	V
Gate-source voltage			V _{GS}	± 30	
Continuous drain current	V _{GS} at 10 V	T _C = 25 °C	I _D	5.7	A
		T _C = 100 °C		3.6	
Pulsed drain current ^a			I _{DM}	23	
Linear derating factor				0.32	W/°C
Single pulse avalanche energy ^b			E _{AS}	310	mJ
Repetitive avalanche current ^a			I _{AR}	5.7	A
Repetitive avalanche energy ^a			E _{AR}	4.0	mJ
Maximum power dissipation	T _C = 25 °C		P _D	40	W
Peak diode recovery dV/dt ^c			dV/dt	4.0	V/ns
Operating junction and storage temperature range			T _J , T _{stg}	-55 to +150	°C
Soldering recommendations (peak temperature) ^d	For 10 s			300	
Mounting torque	M3 screw			0.6	Nm

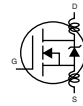
Notes

- Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11)
- $V_{DD} = 50\text{ V}$, starting $T_J = 25^\circ\text{C}$, $L = 16\text{ mH}$, $R_g = 25\ \Omega$, $I_{AS} = 5.7\text{ A}$ (see fig. 12)
- $I_{SD} \leq 10\text{ A}$, $dI/dt \leq 120\text{ A}/\mu\text{s}$, $V_{DD} \leq V_{DS}$, $T_J \leq 150^\circ\text{C}$
- 1.6 mm from case

THERMAL RESISTANCE RATINGS

PARAMETER	SYMBOL	TYP.	MAX.	UNIT
Maximum junction-to-ambient	R_{thJA}	-	65	°C/W
Maximum junction-to-case (drain)	R_{thJC}	-	3.1	

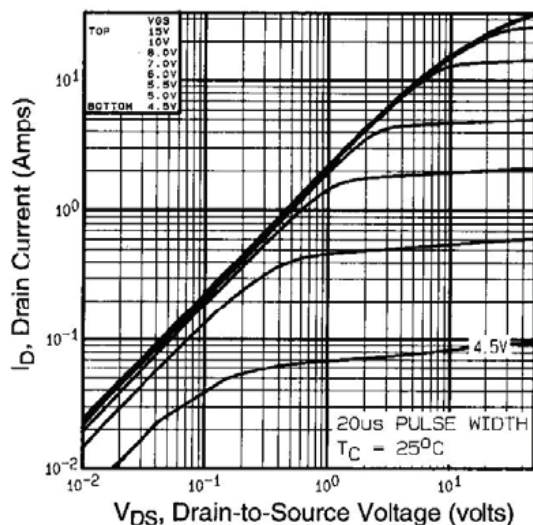
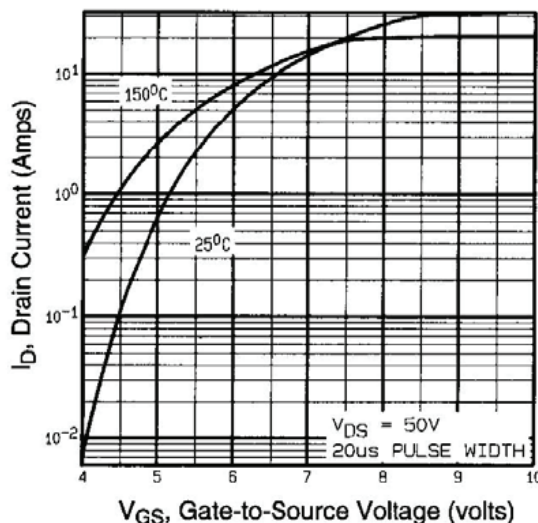
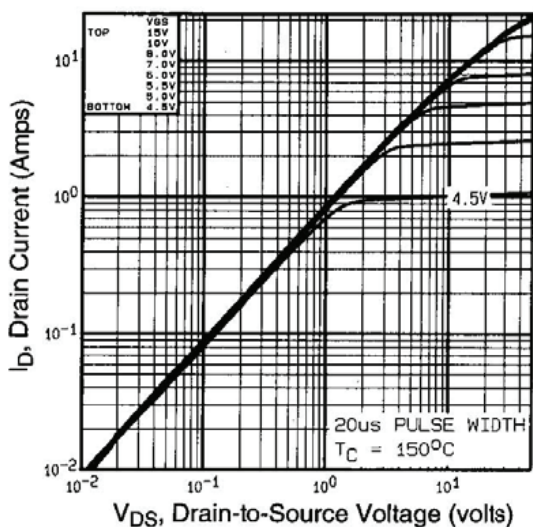
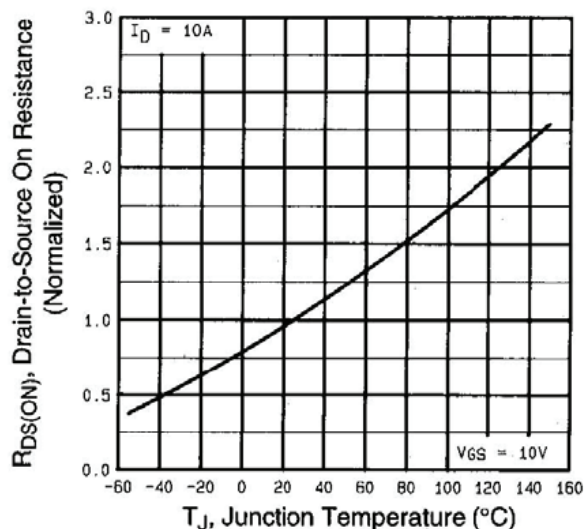
SPECIFICATIONS ($T_J = 25\text{ °C}$, unless otherwise noted)

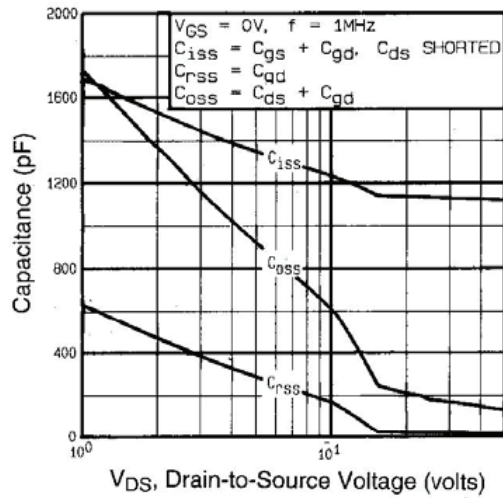
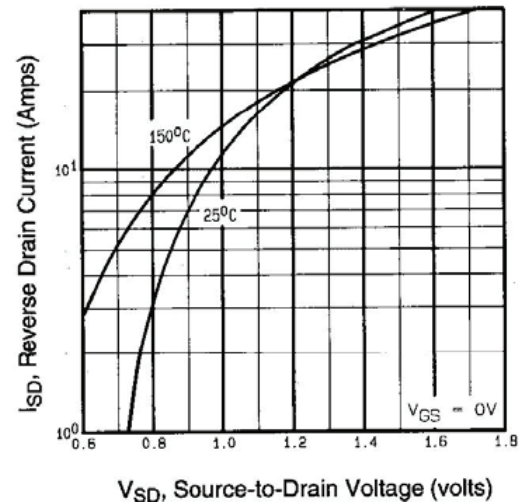
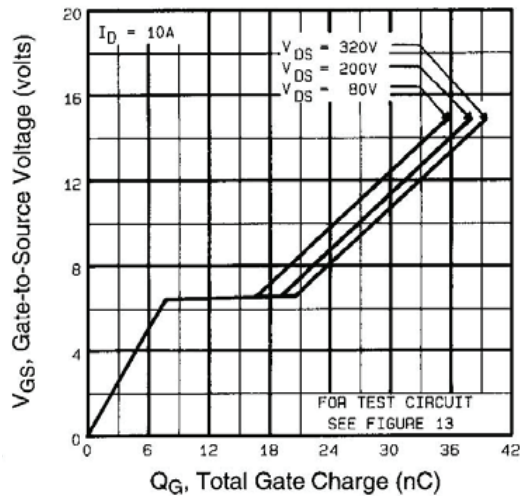
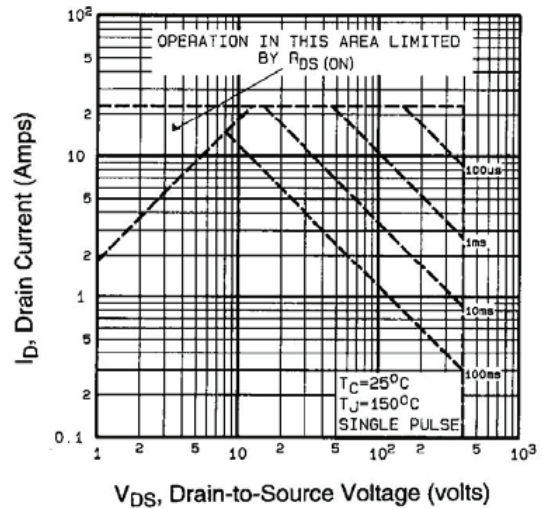
PARAMETER	SYMBOL	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT
Static							
Drain-ssource breakdown voltage	V _{DS}	V _{GS} = 0 V, I _D = 250 μA		400	-	-	V
V _{DS} temperature coefficient	ΔV _{DS} /T _J	Reference to 25 °C, I _D = 1 mA		-	0.76	-	V/°C
Gate-source threshold voltage	V _{GS(th)}	V _{DS} = V _{GS} , I _D = 250 μA		2.0	-	4.0	V
Gate-source leakage	I _{GSS}	V _{GS} = ± 20 V		-	-	± 100	nA
Zero gate voltage drain current	I _{DSS}	V _{DS} = 400 V, V _{GS} = 0 V		-	-	25	μA
		V _{DS} = 320 V, V _{GS} = 0 V, T _J = 125 °C		-	-	250	
Drain-source on-state resistance	R _{DS(on)}	V _{GS} = 10 V	I _D = 3.4 A ^b	-	-	0.55	Ω
Forward transconductance	g _{fs}	V _{DS} = 50 V, I _D = 6.0 A ^b		3.0	-	-	S
Dynamic							
Input capacitance	C _{iss}	V _{GS} = 0 V, V _{DS} = 25 V, f = 1.0 MHz, see fig. 5		-	1100	-	pF
Output capacitance	C _{oss}			-	190	-	
Reverse transfer capacitance	C _{rss}			-	18	-	
Drain to sink capacitance	C	f = 1.0 MHz		-	12	-	
Total gate charge	Q _g	V _{GS} = 10 V	I _D = 10 A, V _{DS} = 320 V, see fig. 6 and 13 ^b	-	-	39	nC
Gate-source charge	Q _{gs}			-	-	10	
Gate-drain charge	Q _{gd}			-	-	19	
Turn-on delay time	t _{d(on)}	V _{DD} = 200 V, I _D = 10 A, R _g = 9.1Ω, R _D = 20 Ω, see fig. 10 ^b		-	11	-	ns
Rise time	t _r			-	31	-	
Turn-off delay time	t _{d(off)}			-	25	-	
Fall time	t _f			-	20	-	
Gate input resistance	R _g	f = 1 MHz, open drain		0.3	-	1.7	Ω
Internal drain inductance	L _D	Between lead, 6 mm (0.25") from package and center of die contact 		-	4.5	-	nH
Internal source inductance	L _S			-	7.5	-	
Drain-Source Body Diode Characteristics							
Continuous source-drain diode current	I _S	MOSFET symbol showing the integral reverse p - n junction diode 		-	-	5.7	A
Pulsed diode forward current ^a	I _{SM}			-	-	23	
Body diode voltage	V _{SD}	T _J = 25 °C, I _S = 5.7 A, V _{GS} = 0 V ^b		-	-	2.0	V
Body diode reverse recovery time	t _{rr}	T _J = 25 °C, I _F = 10 A, dI/dt = 100 A/μs ^b		-	380	570	ns
Body diode reverse recovery charge	Q _{rr}			-	2.8	4.2	μC
Forward turn-on time	t _{on}	Intrinsic turn-on time is negligible (turn-on is dominated by L _S and L _D)					

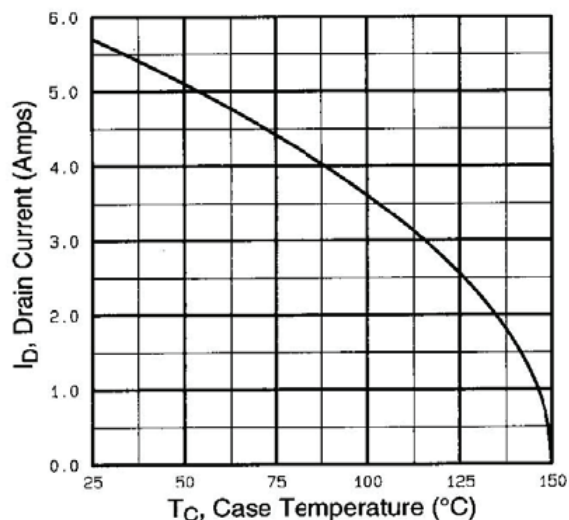
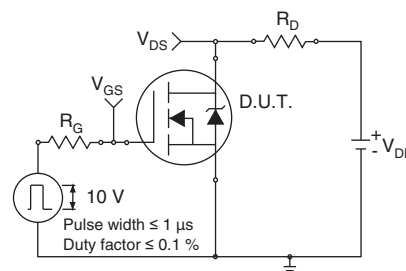
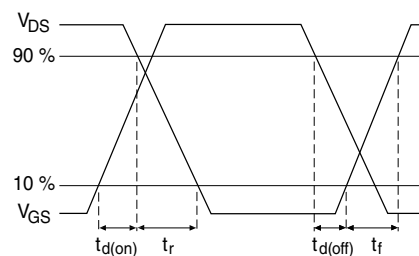
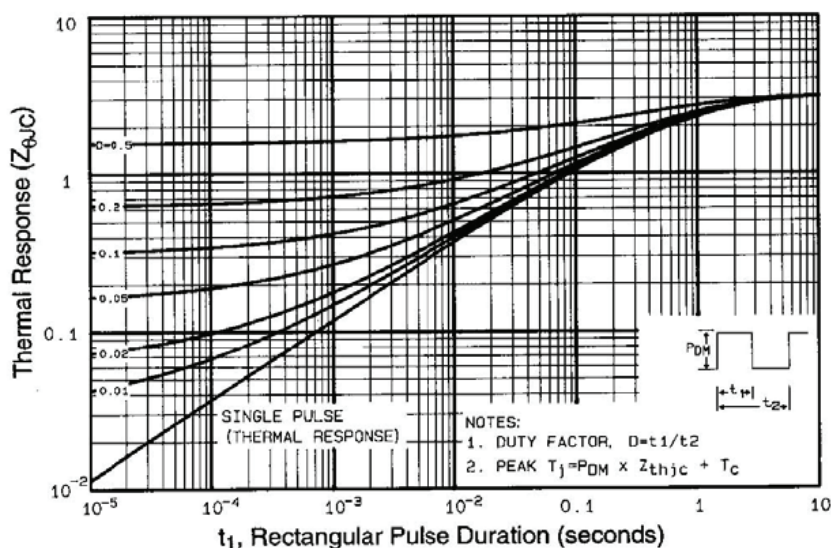
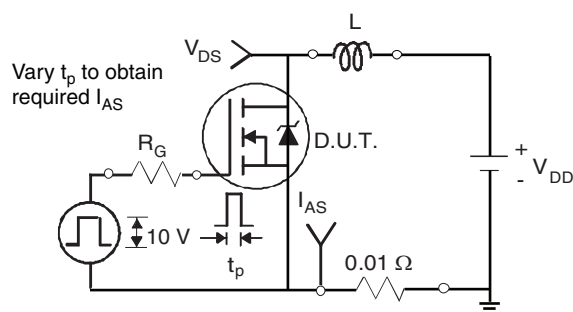
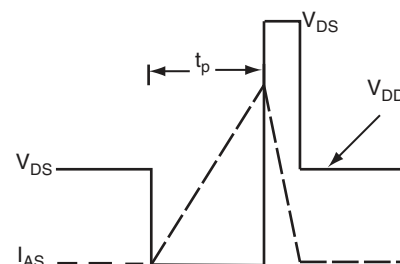
Notes

a. Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11)

b. Pulse width $\leq 300\text{ }\mu\text{s}$; duty cycle $\leq 2\%$

TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)

Fig. 1 - Typical Output Characteristics, $T_C = 25\text{ }^\circ\text{C}$

Fig. 3 - Typical Transfer Characteristics

Fig. 2 - Typical Output Characteristics, $T_C = 150\text{ }^\circ\text{C}$

Fig. 4 - Normalized On-Resistance vs. Temperature


Fig. 5 - Typical Capacitance vs. Drain-to-Source Voltage

Fig. 7 - Typical Source-Drain Diode Forward Voltage

Fig. 6 - Typical Gate Charge vs. Gate-to-Source Voltage

Fig. 8 - Maximum Safe Operating Area


Fig. 9 - Maximum Drain Current vs. Case Temperature

Fig. 10a - Switching Time Test Circuit

Fig. 10b - Switching Time Waveforms

Fig. 11 - Maximum Effective Transient Thermal Impedance, Junction-to-Case

Fig. 12a - Unclamped Inductive Test Circuit

Fig. 12b - Unclamped Inductive Waveforms

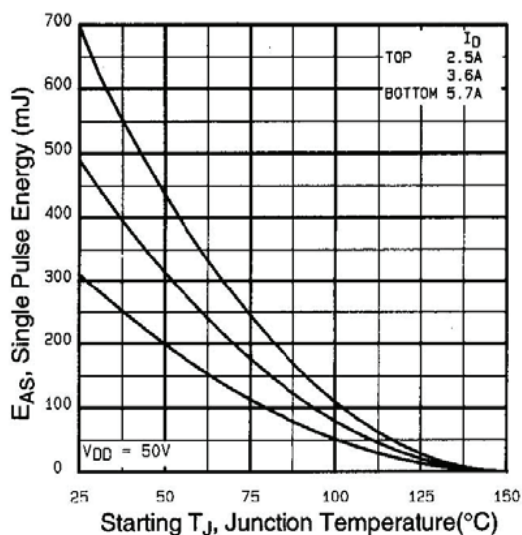


Fig. 12c - Maximum Avalanche Energy vs. Drain Current

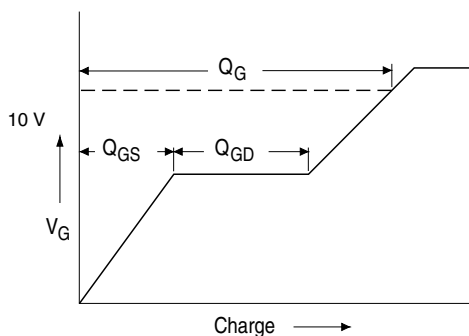


Fig. 13a - Basic Gate Charge Waveform

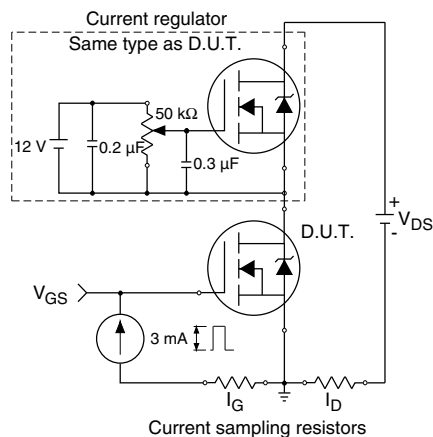
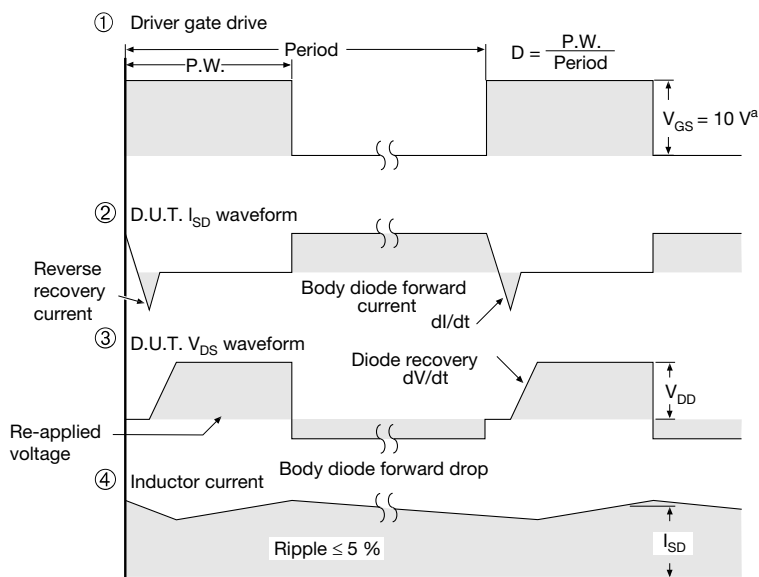
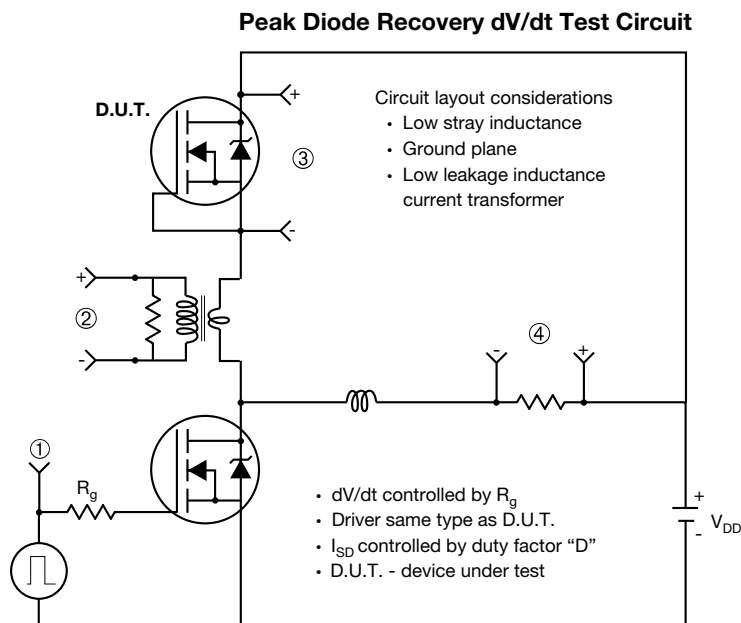


Fig. 13b - Gate Charge Test Circuit


Note

a. $V_{GS} = 5 V$ for logic level devices

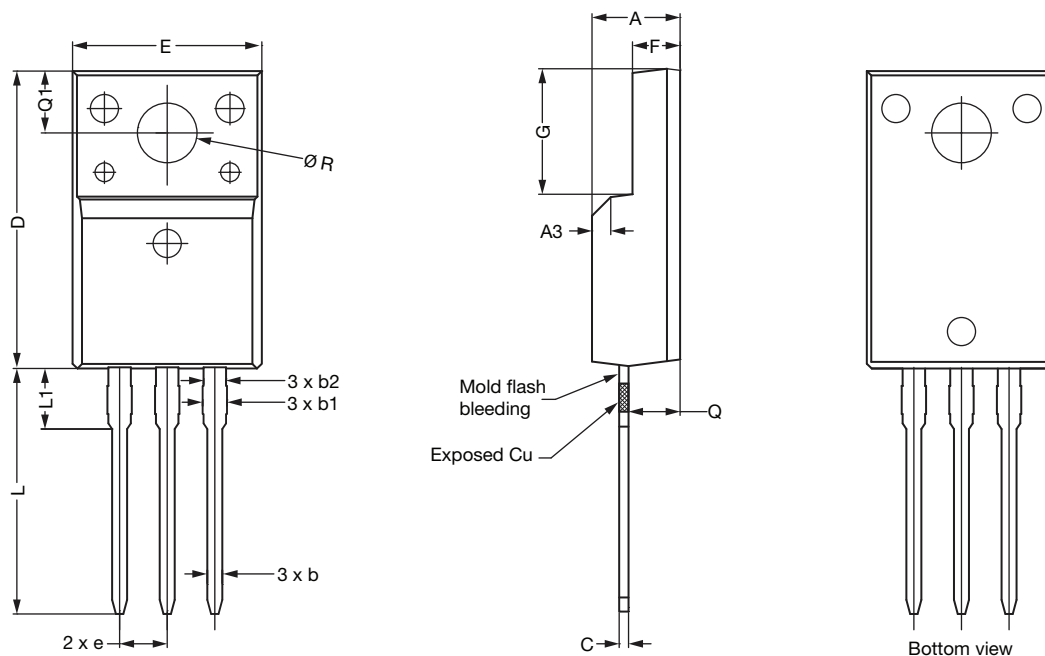
Fig. 14 - For N-Channel

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TO-220 FULLPAK (High Voltage)

OPTION 1: FACILITY CODE = 9



DIM.	MILLIMETERS		
	MIN.	NOM.	MAX.
A	4.60	4.70	4.80
b	0.70	0.80	0.91
b1	1.20	1.30	1.47
b2	1.10	1.20	1.30
C	0.45	0.50	0.63
D	15.80	15.87	15.97
e	2.54 BSC		
E	10.00	10.10	10.30
F	2.44	2.54	2.64
G	6.50	6.70	6.90
L	12.90	13.10	13.30
L1	3.13	3.23	3.33
Q	2.65	2.75	2.85
Q1	3.20	3.30	3.40
Ø R	3.08	3.18	3.28

Notes

1. To be used only for process drawing
2. These dimensions apply to all TO-220 FULLPAK leadframe versions 3 leads
3. All critical dimensions should C meet $C_{pk} > 1.33$
4. All dimensions include burrs and plating thickness
5. No chipping or package damage
6. Facility code will be the 1st character located at the 2nd row of the unit marking



OPTION 2: FACILITY CODE = Y



DIM.	MILLIMETERS		INCHES	
	MIN.	MAX.	MIN.	MAX.
A	4.570	4.830	0.180	0.190
A1	2.570	2.830	0.101	0.111
A2	2.510	2.850	0.099	0.112
b	0.622	0.890	0.024	0.035
b2	1.229	1.400	0.048	0.055
b3	1.229	1.400	0.048	0.055
c	0.440	0.629	0.017	0.025
D	8.650	9.800	0.341	0.386
d1	15.88	16.120	0.622	0.635
d3	12.300	12.920	0.484	0.509
E	10.360	10.630	0.408	0.419
e	2.54 BSC		0.100 BSC	
L	13.200	13.730	0.520	0.541
L1	3.100	3.500	0.122	0.138
n	6.050	6.150	0.238	0.242
Ø P	3.050	3.450	0.120	0.136
u	2.400	2.500	0.094	0.098
V	0.400	0.500	0.016	0.020

ECN: E19-0180-Rev. D, 08-Apr-2019
DWG: 5972

Notes

1. To be used only for process drawing
2. These dimensions apply to all TO-220 FULLPAK leadframe versions 3 leads
3. All critical dimensions should C meet $C_{pk} > 1.33$
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5. No chipping or package damage
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