

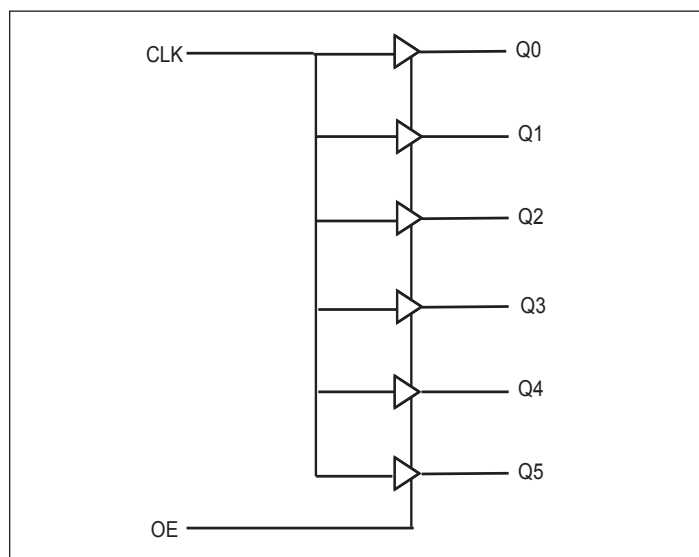
PI6C49X0206T

Low Skew, 1-To-6 LVCMOS / LVTTTL Fanout Buffer

Description

The PI6C49X0206T is a low skew, 1-to-6 LVCMOS/LVTTTL High Performance Fanout Buffer. The PI6C49X0206T has a single ended clock input. The single ended clock input accepts LVCMOS or LVTTTL input levels. The PI6C49X0206T features a pair of LVCMOS/LVTTTL outputs. Guaranteed output and part-to-part skew characteristics make the PI6C49X0206T ideal for clock distribution applications demanding well defined performance and repeatability.

Block Diagram



Features

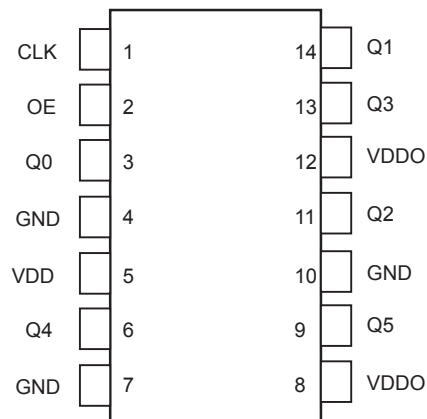
- 6 LVCMOS / LVTTTL Outputs
- LVCMOS / LVTTTL Clock Input accepts LVCMOS or LVTTTL Input Levels
- Maximum Output Frequency: 250MHz
- Part-to-Part Skew: 250ps (typical)
- Full 3.3V, 2.5V, 1.8V Operation Mode, or 3.3V/ 2.5V/ 1.8V core with 2.5V, 1.8V, 1.5V Supply Modes
- Ambient Operating Temperature: -40°C to 85°C
- Packaging (Pb-free & Green available):
 - 14-pin, 173-mil wide TSSOP (L)
- Totally Lead-Free & Fully RoHS Compliant (Notes 1 & 2)
- Halogen and Antimony Free. "Green" Device (Note 3)
- For automotive applications requiring specific change control (i.e. parts qualified to AEC-Q100/101/104/200, PPAP capable, and manufactured in IATF 16949 certified facilities), please [contact us](https://www.diodes.com/quality/product-definitions/) or your local Diodes representative.

<https://www.diodes.com/quality/product-definitions/>

Notes:

1. No purposely added lead. Fully EU Directive 2002/95/EC (RoHS), 2011/65/EU (RoHS 2) & 2015/863/EU (RoHS 3) compliant.
2. See <https://www.diodes.com/quality/lead-free/> for more information about Diodes Incorporated's definitions of Halogen- and Antimony-free, "Green" and Lead-free.
3. Halogen- and Antimony-free "Green" products are defined as those which contain <900ppm bromine, <900ppm chlorine (<1500ppm total Br + Cl) and <1000ppm antimony compounds.

Pin Configuration



Pin Description

Pin Number	Pin Name	Type		Pin Description
1	CLK	Input	Pulldown	LVC MOS / LVTTTL clock input.
2	OE	Input		Output Enable pin
3, 6, 9, 11, 13, 14	Q0, Q4, Q5, Q2, Q3, Q1	Output		Single clock output. LVC MOS / LVTTTL interface levels.
4, 7, 10	GND	Power		Power supply ground.
5	VDD	Power		Core supply pins.
8, 12	VDDO	Power		Output supply pins.

Note: Pulldown refer to internal input resistors, typical values in Pin Characteristics table.

Table 1. Pin Characteristics

Symbol	Parameter	Min.	Typ.	Max.	Units
C_N	Capacitance		4		pF
$R_{PULLDOWN}$	Input Pulldown Resistor		51		k Ω

Table 2. Output Logic

Inputs		Output
CLK	OE	Qn
X	L	L
L	H	L
H	H	H

Maximum Ratings

(Above which useful life may be impaired. For user guidelines, not tested.)

Maximum Supply Voltage, VDD, VDDO	4.6V
Inputs, V _I	-0.5V to VDD +0.5V
Output, V _O	-0.5V to VDDO +0.5V
Storage Temperature	-65°C to 150°C
ESD Protection (HBM)	2000V

Note:

Stresses greater than those listed under MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

Power Supply DC Characteristics

T_A = -40°C to 85°C

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
VDD	Core Supply Voltage	3.3V Operation	3.135	3.3	3.465	V
		2.5V Operation	2.375	2.5	2.625	
		1.8V Operation	1.6	1.8	2.0	
VDDO	Output Power Supply Voltage	3.3V Supply	3.135	3.3	3.465	V
		2.5V Supply	2.375	2.5	2.625	
		1.8V Supply	1.6	1.8	2.0	
		1.5V Supply	1.425	1.5	1.575	
IDD	Power Supply Current	No load			2	mA
IDDO	Output Supply Current	5pF load, 25MHz, VDDO = 3.3V		6	9.5	mA
		5pF load, 25MHz, VDDO = 2.5V		5.7	7.2	mA
		5pF load, 25MHz, VDDO = 1.8V		4.5	5.5	mA
		5pF load, 25MHz, VDDO = 1.5V		3.5	4.6	mA
		5pF load, 200MHz, VDDO = 3.3V		57	72	mA
		5pF load, 200MHz, VDDO = 2.5V		44	54	mA
		5pF load, 200MHz, VDDO = 1.8V		32	39	mA
		5pF load, 200MHz, VDDO = 1.5V		19	24	mA

LVC MOS / LV TTL DC Characteristics

T_A = -45°C to 85°C

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
V _{IH}	Input High Voltage	VDD = 3.3V	2		VDD+0.3	V
		VDD = 2.5V	1.7		VDD+0.3	
		VDD = 1.8V	0.65*VDD		VDD+0.3	
V _{IL}	Input Low Voltage	VDD = 3.3V	-0.3		0.8	V
		VDD = 2.5V	-0.3		0.8	
		VDD = 1.8V	-0.3		0.35*VDD	

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
I_{IH}	Input High Current	$V_{DD} = V_{IN} = 3.465V$			150	μA
		$V_{DD} = V_{IN} = 2.625V$			150	
		$V_{DD} = V_{IN} = 2.0V$			150	
I_{IL}	Input Low Current	$V_{DD} = 3.465V, V_{IN} = 0$	-5			μA
		$V_{DD} = 2.625V, V_{IN} = 0$	-5			
		$V_{DD} = 2.0V, V_{IN} = 0$	-5			
V_{OH}	Output High Voltage	$V_{DDO} = 3.3V$	50 Ω to $V_{DDO} / 2$	2.6		V
			$I_{OH} = -100\mu A$	2.9		V
		$V_{DDO} = 2.5V$	50 Ω to $V_{DDO} / 2$	1.8		V
			$I_{OH} = -100\mu A$	2.2		V
		$V_{DDO} = 1.8V$	50 Ω to $V_{DDO} / 2$	1.2		V
			$I_{OH} = -100\mu A$	1.6		V
		$V_{DDO} = 1.5V$	50 Ω to $V_{DDO} / 2$	0.96		V
			$I_{OH} = -100\mu A$	1.3		V
V_{OL}	Output Low Voltage	$V_{DDO} = 3.3V$	50 Ω to $V_{DDO} / 2$		0.6	V
			$I_{OL} = 100\mu A$		0.2	V
		$V_{DDO} = 2.5V$	50 Ω to $V_{DDO} / 2$		0.6	V
			$I_{OL} = 100\mu A$		0.2	V
		$V_{DDO} = 1.8V$	50 Ω to $V_{DDO} / 2$		0.6	V
			$I_{OL} = 100\mu A$		0.2	V
		$V_{DDO} = 1.5V$	50 Ω to $V_{DDO} / 2$		0.6	V
			$I_{OL} = 100\mu A$		0.2	V

AC Characteristics

$V_{DD} = 3.3V \pm 5\%$, $T_A = -45^\circ C$ to $85^\circ C$

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
f_{MAX}	Output Frequency	$V_{DDO} = 3.3V$			250	MHz
		$V_{DDO} = 2.5V$			250	
		$V_{DDO} = 1.8V$			250	
		$V_{DDO} = 1.5V$			250	
t_{PLH}	Propagation Delay, Low-to-High ⁽¹⁾	$V_{DDO} = 3.3V, f \leq 250MHz$	1.2	1.6	2.8	ns
		$V_{DDO} = 2.5V, f \leq 250MHz$	1.45	1.9	3.3	
		$V_{DDO} = 1.8V, f \leq 250MHz$	2.2	2.8	3.6	
		$V_{DDO} = 1.5V, f \leq 250MHz$	3.25	4	4.7	
$tsk(o)$	Output Skew ⁽²⁾	$V_{DDO} = 2.5V, 3.3V$		68	100	ps
		$V_{DDO} = 1.5V, 1.8V$		80	150	ps
$tsk(pp)$	Part-to-Part Skew ⁽³⁾			250	800	ps

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Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
t_R	Output Rise Time ⁽⁴⁾	VDDO = 3.3V	300		800	ps
		VDDO = 2.5V	300		800	
		VDDO = 1.8V	300		800	
		VDDO = 1.5V	600		1000	
t_F	Output Fall Time ⁽⁴⁾	VDDO = 3.3V	300		800	ps
		VDDO = 2.5V	300		800	
		VDDO = 1.8V	300		800	
		VDDO = 1.5V	600		1000	
odc	Output Duty Cycle	$f \leq 133\text{MHz}$	45		55	%
		$133\text{MHz} < f \leq 250\text{MHz}$	40		60	%
t_{jit}	Additive RMS Jitter	156.25MHz (@12kHz to 20MHz)		0.03		ps
		125MHz (@12kHz to 20MHz)		0.05		ps
t_{OED}	Output Disable Time				6	ns
t_{OE}	Output Enable Time				6	ns

Parameters measured at f_{MAX} unless otherwise noted.

NOTE:

1. Measured from VDD /2 of the input to VDDO /2 of the output.
2. Defined as skew between outputs at the same supply voltage and with equal load conditions. Measured at VDDO /2.
3. Defined as skew between outputs on different devices operating at the same supply voltages and with equal load conditions. Using the same type of inputs on each device, the outputs are measured at VDDO /2.
4. Defined from 20% to 80%

VDD = 2.5V $\pm$ 5%, T_A = -45°C to 85°C

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
f_{MAX}	Output Frequency	VDDO = 2.5V			250	MHz
		VDDO = 1.8V			250	
		VDDO = 1.5V			250	
t_{PLH}	Propagation Delay, Low-to-High ⁽¹⁾	VDDO = 2.5V, $f \leq 250\text{MHz}$	1.56	2	2.7	ns
		VDDO = 1.8V, $f \leq 250\text{MHz}$	2.3	2.9	3.7	
		VDDO = 1.5V, $f \leq 250\text{MHz}$	3.34	4	4.83	
$tsk(o)$	Output Skew ⁽²⁾	VDDO = 1.8V, 2.5V		68	100	ps
		VDDO = 1.5V		80	150	ps
$tsk(pp)$	Part-to-Part Skew ⁽³⁾			250	800	ps
t_R	Output Rise Time ⁽⁴⁾	VDDO = 2.5V	300		800	ps
		VDDO = 1.8V	300		800	
		VDDO = 1.5V	500		1000	
t_F	Output Fall Time ⁽⁴⁾	VDDO = 2.5V	300		800	ps
		VDDO = 1.8V	300		800	
		VDDO = 1.5V	500		1000	

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Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
odc	Output Duty Cycle	$f \leq 133\text{MHz}$	45		55	%
		$133\text{MHz} < f \leq 250\text{MHz}$	40		60	%
t_{jit}	Additive RMS Jitter	156.25MHz (@12kHz to 20MHz)		0.03		ps
		125MHz (@12kHz to 20MHz)		0.05		ps
t_{OED}	Output Disable Time				10	ns
t_{OE}	Output Enable Time				10	ns

Parameters measured at f_{MAX} unless otherwise noted.

NOTE:

1. Measured from VDD /2 of the input to VDDO /2 of the output.
2. Defined as skew between outputs at the same supply voltage and with equal load conditions. Measured at VDDO /2.
3. Defined as skew between outputs on different devices operating at the same supply voltages and with equal load conditions. Using the same type of inputs on each device, the outputs are measured at VDDO /2.
4. Defined from 20% to 80%

VDD = 1.8V $\pm$ 0.2V, $T_A = -45^\circ\text{C}$ to 85°C

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
f_{MAX}	Output Frequency	VDDO = 1.8V			250	MHz
		VDDO = 1.5V			250	
t_{PLH}	Propagation Delay, Low-to-High ⁽¹⁾	VDDO = 1.8V, $f \leq 250\text{MHz}$	2.57	3.25	4	ns
		VDDO = 1.5V, $f \leq 250\text{MHz}$	3.57	4.3	5.1	
$tsk(o)$	Output Skew ⁽²⁾	VDDO = 1.8V		68	100	ps
		VDDO = 1.5V		80	150	ps
$tsk(pp)$	Part-to-Part Skew ⁽³⁾			250	800	ps
t_R	Output Rise Time ⁽⁴⁾	VDDO = 1.8V	300		800	ps
		VDDO = 1.5V	500		1000	
t_F	Output Fall Time ⁽⁴⁾	VDDO = 1.8V	300		800	ps
		VDDO = 1.5V	500		1000	
odc	Output Duty Cycle	$f \leq 133\text{MHz}$	45		55	%
		$133\text{MHz} < f \leq 250\text{MHz}$	40		60	%
t_{jit}	Additive RMS Jitter	156.25MHz (@12kHz to 20MHz)		0.03		ps
		125MHz (@12kHz to 20MHz)		0.06		ps
t_{OED}	Output Disable Time				14	ns
t_{OE}	Output Enable Time				14	ns

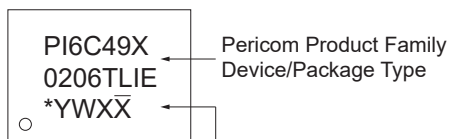
Parameters measured at f_{MAX} unless otherwise noted.

NOTE:

1. Measured from VDD /2 of the input to VDDO /2 of the output.
2. Defined as skew between outputs at the same supply voltage and with equal load conditions. Measured at VDDO /2.
3. Defined as skew between outputs on different devices operating at the same supply voltages and with equal load conditions. Using the same type of inputs on each device, the outputs are measured at VDDO /2.
4. Defined from 20% to 80%

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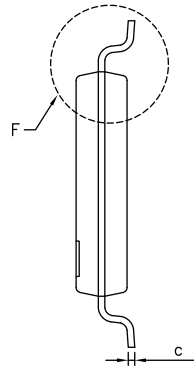
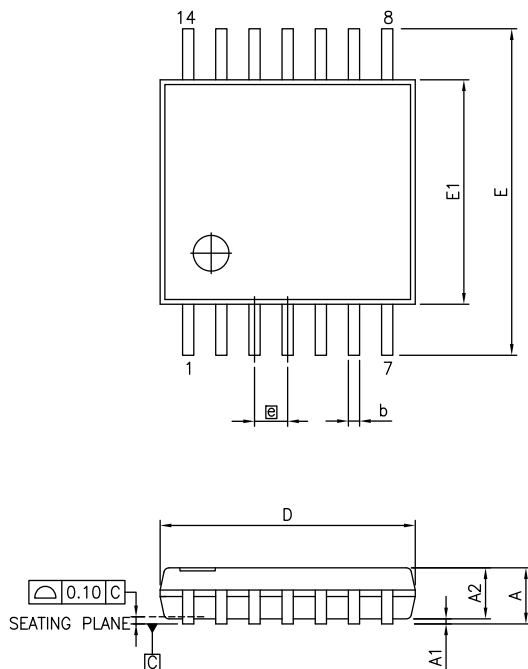
Part Marking



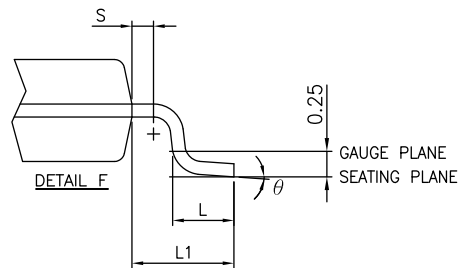
*: Die Rev
Y: Date Code (Year)
W: Date Code (Workweek)
1st X: Assembly Code
2nd X: Fab Code
Note: Date Code per MA-1251

Packaging Mechanical

14-TSSOP (L)



SYMBOLS	MIN.	NOM.	MAX.
A	—	—	1.20
A1	0.05	—	0.15
A2	0.80	1.00	1.05
b	0.19	—	0.30
c	0.09	—	0.20
D	4.90	5.00	5.10
E1	4.30	4.40	4.50
E	6.20	6.40	6.60
e	0.65 BSC		
L1	1.00 REF		
L	0.45	0.60	0.75
S	0.20	—	—
θ	0°	—	8°



NOTES:

1. ALL DIMENSIONS IN MILLIMETERS. ANGLES IN DEGREES.
2. JEDEC MO-153F
3. DIMENSIONS DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS.

16-0060



DATE: 03/24/16

DESCRIPTION: 14-Pin, 173mil Wide TSSOP

PACKAGE CODE: L (L14)

DOCUMENT CONTROL #: PD-1309

REVISION: E

For latest package info.

please check: <http://www.diodes.com/design/support/packaging/pericom-packaging/packaging-mechanicals-and-thermal-characteristics/>

Mechanical Data

Mechanical Data is not available at this time. To obtain advance information regarding the Mechanical Data, please contact your local sales representative.

PI6C49X0206T

Ordering Information

Orderable Part Number	Package Code	Package Description
PI6C49X0206TLIEX	L	14-pin, 173mil Wide (TSSOP)

Notes:

1. No purposely added lead. Fully EU Directive 2002/95/EC (RoHS), 2011/65/EU (RoHS 2) & 2015/863/EU (RoHS 3) compliant.
2. See <https://www.diodes.com/quality/lead-free/> for more information about Diodes Incorporated's definitions of Halogen- and Antimony-free, "Green" and Lead-free.
3. Halogen- and Antimony-free "Green" products are defined as those which contain <900ppm bromine, <900ppm chlorine (<1500ppm total Br + Cl) and <1000ppm antimony compounds.
4. I = Industrial
5. E = Pb-free and Green
6. X suffix = Tape/Reel

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