

4-Mb (256K x 16) Static RAM

Features

- Very high speed: 55 ns and 70 ns
- Wide voltage range: 1.65V – 2.25V
- Pin-compatible with CY62147CV18
- Ultra-low active power
 - Typical active current: 1 mA @ $f = 1 \text{ MHz}$
 - Typical active current: 6 mA @ $f = f_{\text{max}}$
- Ultra low standby power
- Easy memory expansion with $\overline{\text{CE}}$, and $\overline{\text{OE}}$ features
- Automatic power-down when deselected
- CMOS for optimum speed/power
- Packages offered 48-ball BGA

Functional Description^[1]

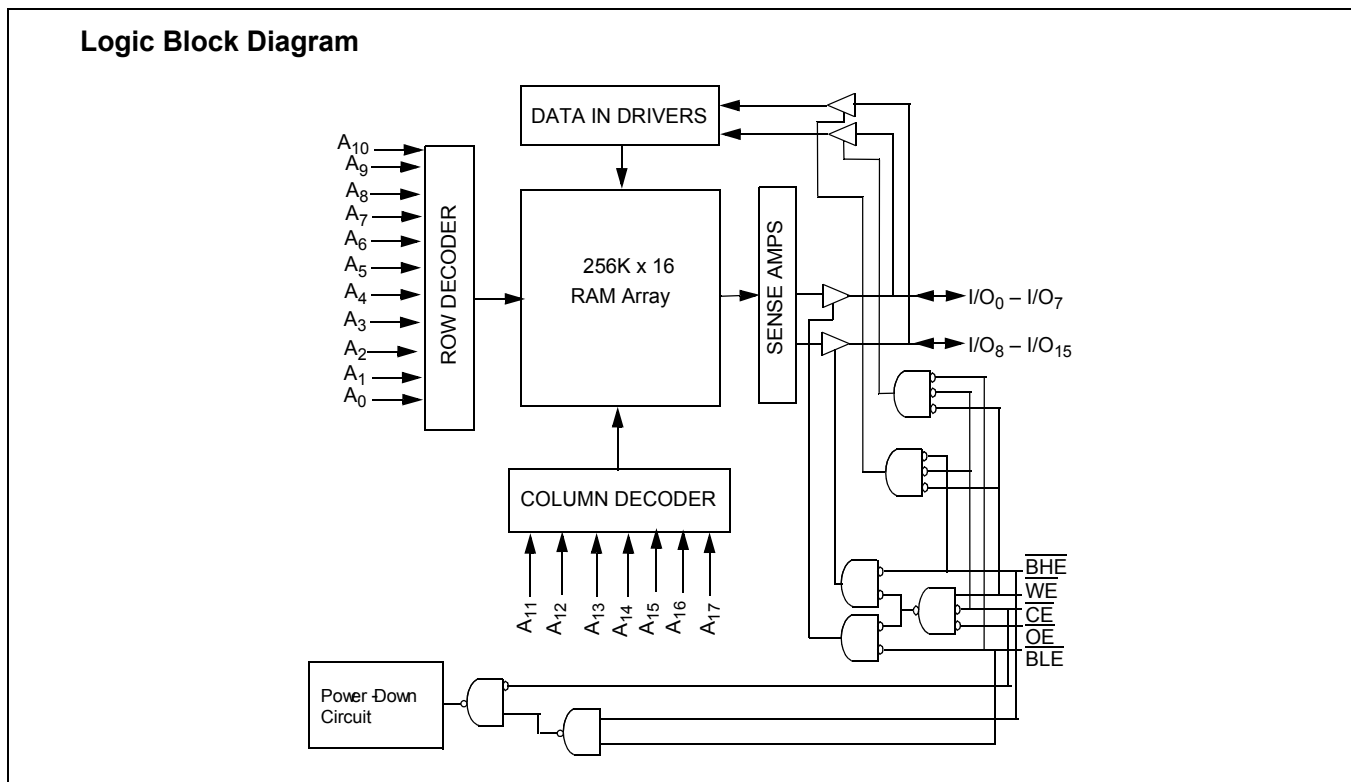
The CY62147DV18 is a high-performance CMOS static RAM organized as 256K words by 16 bits. This device features advanced circuit design to provide ultra-low active current. This is ideal for providing More Battery Life™ (MoBL™) in portable applications such as cellular telephones. The device also has an automatic power-down feature that significantly reduces power consumption. The device can also be put into standby

mode reducing power consumption by more than 99% when deselected (CE HIGH or both BLE and BHE are HIGH). The input/output pins (I/O₀ through I/O₁₅) are placed in a high-impedance state when: deselected (CE HIGH), outputs are disabled (OE HIGH), both Byte High Enable and Byte Low Enable are disabled (BHE, BLE HIGH), or during a write operation (CE LOW and WE LOW).

Writing to the device is accomplished by asserting Chip Enable (CE) and Write Enable (WE) inputs LOW. If Byte Low Enable (BLE) is LOW, then data from I/O pins (I/O₀ through I/O₇), is written into the location specified on the address pins (A₀ through A₁₇). If Byte High Enable (BHE) is LOW, then data from I/O pins (I/O₈ through I/O₁₅) is written into the location specified on the address pins (A₀ through A₁₇).

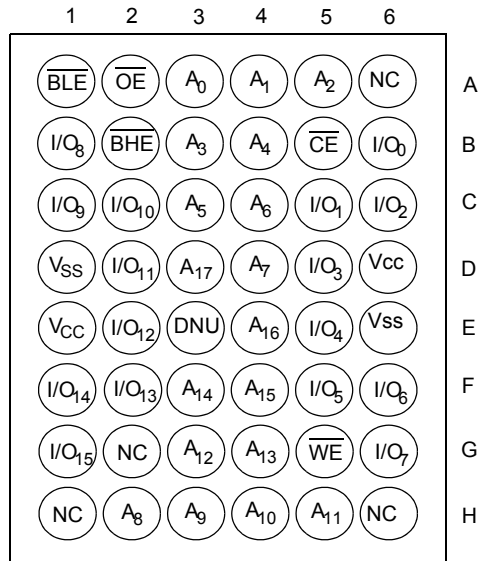
Reading from the device is accomplished by asserting Chip Enable (CE) and Output Enable (OE) LOW while forcing the Write Enable (WE) HIGH. If Byte Low Enable (BLE) is LOW, then data from the memory location specified by the address pins will appear on I/O₀ to I/O₇. If Byte High Enable (BHE) is LOW, then data from memory will appear on I/O₈ to I/O₁₅. See the truth table for a complete description of read and write modes.

The CY62147DV18 is available in a 48-ball FBGA package.



Note:

1. For best practice recommendations, please refer to the Cypress application note “System Design Guidelines” on <http://www.cypress.com>.

Pin Configuration^[2, 3, 4]
FBGA (Top View)

Notes:

- NC pins are not internally connected on the die.
- DNU pins have to be left floating or tied to V_{SS} to ensure proper application.
- Pins H1, G2, and H6 in the BGA package are address expansion pins for 8 Mb, 16 Mb, and 32 Mb, respectively.

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature -65°C to + 150°C

Ambient Temperature with
Power Applied -55°C to + 125°C

Supply Voltage to Ground
Potential -0.2V to + $V_{CC(MAX)}$ + 0.2V

DC Voltage Applied to Outputs
in High Z State^[5,6] -0.2V to $V_{CC(MAX)}$ + 0.2V

DC Input Voltage^[5,6] -0.2V to $V_{CC(MAX)}$ + 0.2V

Output Current into Outputs (LOW) 20 mA

Static Discharge Voltage > 2001V
(per MIL-STD-883, Method 3015)

Latch-up Current > 200 mA

Operating Range

Device	Range	Ambient Temperature (T _A)	V _{CC} ^[7]
CY62147DV18L	Industrial	-40°C to +85°C	1.65V to 2.25V
CY62147DV18LL			

Product Portfolio

Product	V _{CC} Range (V)			Speed (ns)	Power Dissipation					
					Operating I _{CC} (mA)				Standby I _{SB2} (μA)	
					f = 1MHz		f = f _{max}			
	Min.	Typ. ^[7]	Max.		Typ. ^[7]	Max.	Typ. ^[7]	Max.	Typ. ^[7]	Max.
CY62147DV18L	1.65	1.8	2.25	55	1.0	2.0	6	15	0.5	18
CY62147DV18LL								10		12
CY62147DV18L	1.65	1.8	2.25	70	1.0	2.0	6	15	0.5	18
CY62147DV18LL								10		12

Electrical Characteristics Over the Operating Range

Parameter	Description	Test Conditions		CY62147DV18-55			CY62147DV18-70			Unit
				Min.	Typ. ^[7]	Max.	Min.	Typ. ^[7]	Max.	
V _{OH}	Output HIGH Voltage	I _{OH} = -0.1 mA	V _{CC} = 1.65V	1.4			1.4			V
V _{OL}	Output LOW Voltage	I _{OL} = 0.1 mA	V _{CC} = 1.65V			0.2			0.2	V
V _{IH}	Input HIGH Voltage	V _{CC} = 1.65V to 2.25V		1.4		V _{CC} + 0.2V	1.4		V _{CC} + 0.2V	V
V _{IL}	Input LOW Voltage	V _{CC} = 1.65V to 2.25V		-0.2		0.4	-0.2		0.4	V
I _{IX}	Input Leakage Current	GND ≤ V _I ≤ V _{CC}		-1		+1	-1		+1	μA
I _{OZ}	Output Leakage Current	GND ≤ V _O ≤ V _{CC} , Output Disabled		-1		+1	-1		+1	μA
I _{CC}	V _{CC} Operating Supply Current	f = f _{MAX} = 1/t _{RC}	V _{CC(max)} = 1.95V	L	6	12		6	12	mA
			I _{OUT} = 0 mA CMOS levels	LL		8			8	
			V _{CC(max)} = 2.25V	L	6	15		6	15	mA
			I _{OUT} = 0 mA CMOS levels	LL		10			10	
		f = 1 MHz	V _{CC(max)} = 1.95V	L	1	1.5		1	1.5	mA
				LL						
			V _{CC(max)} = 2.25V	L	1	2		1	2	mA
				LL						

Notes:

- V_{IL(min.)} = -2.0V for pulse durations less than 20 ns.
- V_{IH(max.)} = V_{CC} + 0.75V for pulse durations less than 20ns.
- Typical values are included for reference only and are not guaranteed or tested. Typical values are measured at V_{CC} = V_{CC(typ.)}, T_A = 25°C.

Electrical Characteristics Over the Operating Range (continued)

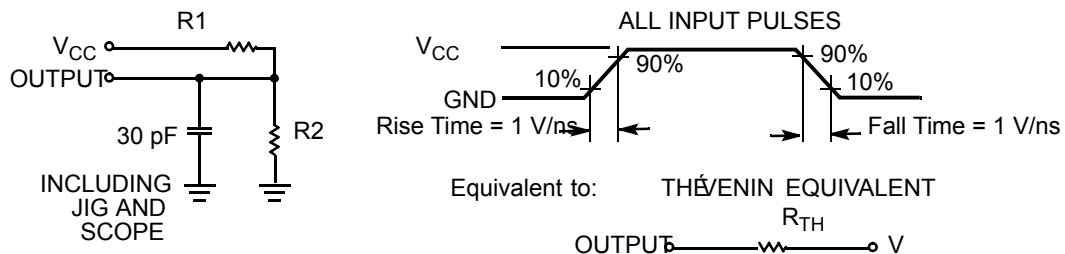
Parameter	Description	Test Conditions			CY62147DV18-55			CY62147DV18-70			Unit
					Min.	Typ. ^[7]	Max.	Min.	Typ. ^[7]	Max.	
I _{SB1}	Automatic CE Power-Down Current — CMOS Inputs	CE ≥ V _{CC} –0.2V, V _{IN} ≥V _{CC} –0.2V, V _{IN} ≤0.2V); f = f _{MAX} (Address and Data Only), f = 0 (OE, WE, BHE and BLE)	V _{CC(max)} =1.95V	L		0.5	12		0.5	12	μA
				LL			8			8	
			V _{CC(max)} =2.25V	L		0.5	18		0.5	18	
				LL			12			12	
I _{SB2}	Automatic CE Power-down Current — CMOS Inputs	CE ≥ V _{CC} – 0.2V, V _{IN} ≥ V _{CC} –0.2V or V _{IN} ≤ 0.2V, f = 0	V _{CC(max)} =1.95V	L		0.5	12		0.5	12	μA
				LL			8			8	
			V _{CC(max)} =2.25V	L		0.5	18		0.5	18	
				LL			12			12	

Capacitance for all Packages^[8]

Parameter	Description	Test Conditions	Max.	Unit
C _{IN}	Input Capacitance	T _A = 25°C, f = 1 MHz,	10	pF
C _{OUT}	Output Capacitance	V _{CC} = V _{CC(typ)}	10	pF

Thermal Resistance

Parameter	Description	Test Conditions	BGA	Unit
Θ _{JA}	Thermal Resistance (Junction to Ambient) ^[8]	Still Air, soldered on a 3 × 4.5 inch, four-layer printed circuit board	75	°C/W
Θ _{JC}	Thermal Resistance (Junction to Case) ^[8]		10	°C/W

AC Test Loads and Waveforms


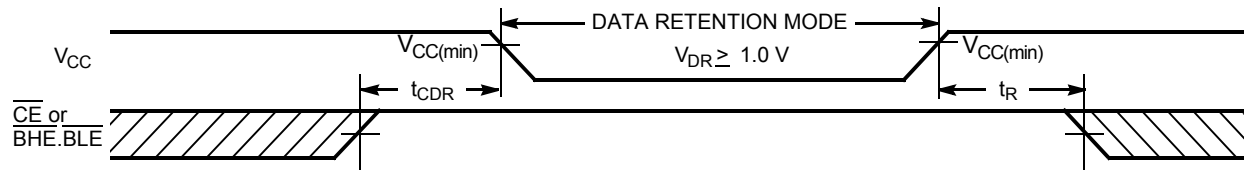
Parameters	1.80V	Unit
R1	13500	Ω
R2	10800	Ω
R _{TH}	6000	Ω
V _{TH}	0.80	V

Data Retention Characteristics (Over the Operating Range)

Parameter	Description	Conditions	Min.	Typ. ^[7]	Max.	Unit
V _{DR}	V _{CC} for Data Retention		1.0			V
I _{CCDR}	Data Retention Current	V _{CC} = 1.0V CE ≥ V _{CC} - 0.2V, V _{IN} ≥ V _{CC} - 0.2V or V _{IN} ≤ 0.2V	L		6	μA
			LL		4	
t _{CDR} ^[8]	Chip Deselect to Data Retention Time		0			ns
t _R	Operation Recovery Time		t _{RC}			ns

Notes:

8. Tested initially and after any design or process changes that may affect these parameters.

Data Retention Waveform^[9]

Switching Characteristics Over the Operating Range^[10]

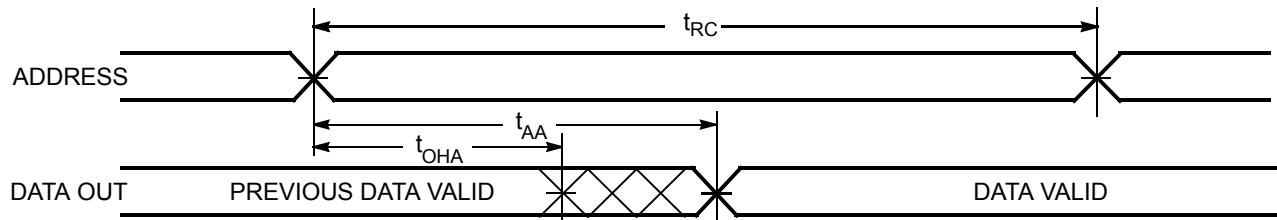
Parameter	Description	55 ns		70 ns		Unit
		Min.	Max.	Min.	Max.	
Read Cycle						
t _{RC}	Read Cycle Time	55		70		ns
t _{AA}	Address to Data Valid		55		70	ns
t _{OHA}	Data Hold from Address Change	10		10		ns
t _{ACE}	CE LOW to Data Valid		55		70	ns
t _{DOE}	OE LOW to Data Valid		25		35	ns
t _{LZOE}	OE LOW to LOW Z ^[11]	5		5		ns
t _{HZOE}	OE HIGH to High Z ^[11, 12]		16		16	ns
t _{LZCE}	CE LOW to Low Z ^[11]	10		10		ns
t _{HZCE}	CE HIGH to High Z ^[11, 12]		20		25	ns
t _{PU}	CE LOW to Power-Up	0		0		ns
t _{PD}	CE HIGH to Power-Down		55		70	ns
t _{DBE}	BLE / BHE LOW to Data Valid		55		70	ns
t _{LZBE}	BLE / BHE LOW to Low Z ^[11]	10		10		ns
t _{HZBE}	BLE / BHE HIGH to HIGH Z ^[11, 12]		20		25	ns
Write Cycle ^[13]						
t _{WC}	Write Cycle Time	55		70		ns
t _{SCE}	CE LOW to Write End	40		50		ns
t _{AW}	Address Set-up to Write End	40		50		ns
t _{HA}	Address Hold from Write End	0		0		ns
t _{SA}	Address Set-up to Write Start	0		0		ns
t _{PWE}	WE Pulse Width	40		45		ns
t _{BW}	BLE / BHE LOW to Write End	40		50		ns
t _{SD}	Data Set-Up to Write End	25		30		ns
t _{HD}	Data Hold from Write End	0		0		ns
t _{HZWE}	WE LOW to High-Z ^[11, 12]		20		25	ns
t _{LZWE}	WE HIGH to Low-Z ^[11]	10		10		ns

Notes:

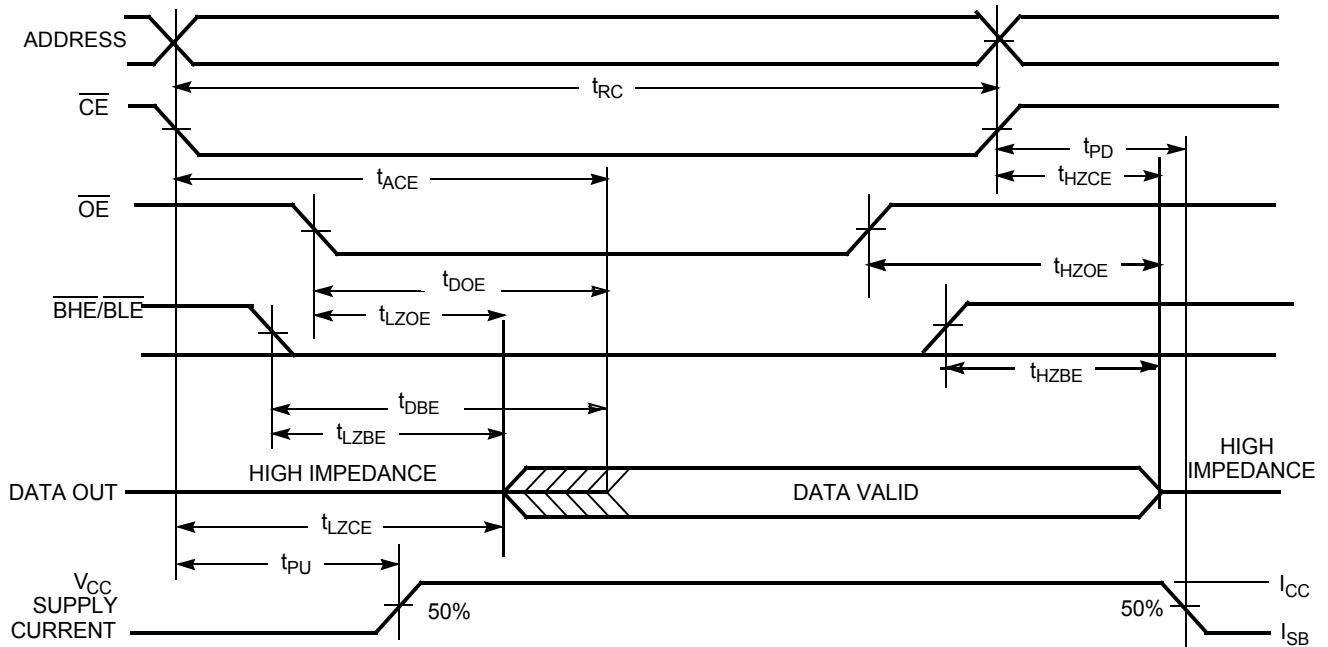
9. $\overline{\text{BHE}}/\overline{\text{BLE}}$ is the AND of both $\overline{\text{BHE}}$ and $\overline{\text{BLE}}$. Chip can be deselected by either disabling the chip enable signal or by disabling both $\overline{\text{BHE}}$ and $\overline{\text{BLE}}$.
10. Test conditions for all parameters other than three-state parameters assume signal transition time of 1V/ns or less, timing reference levels of $V_{CC(\text{typ})}/2$, input pulse levels of 0 to $V_{CC(\text{typ})}$, and output loading of the specified I_{OL}/I_{OH} as shown in the "AC Test Loads and Waveforms" section.
11. At any given temperature and voltage condition, t_{HZCE} is less than t_{LZCE} , t_{HZBE} is less than t_{LZBE} , t_{HZOE} is less than t_{LZOE} , and t_{HZWE} is less than t_{LZWE} for any given device.
12. t_{HZOE} , t_{HZCE} , t_{HZBE} , and t_{HZWE} transitions are measured when the outputs enter a high impedance state.
13. The internal Write time of the memory is defined by the overlap of WE, CE = V_{IL} , BHE and/or BLE = V_{IL} . All signals must be ACTIVE to initiate a write and any of these signals can terminate a write by going INACTIVE. The data input set-up and hold timing should be referenced to the edge of the signal that terminates the write.

Switching Waveforms

Read Cycle 1 (Address Transition Controlled)^[14, 15]

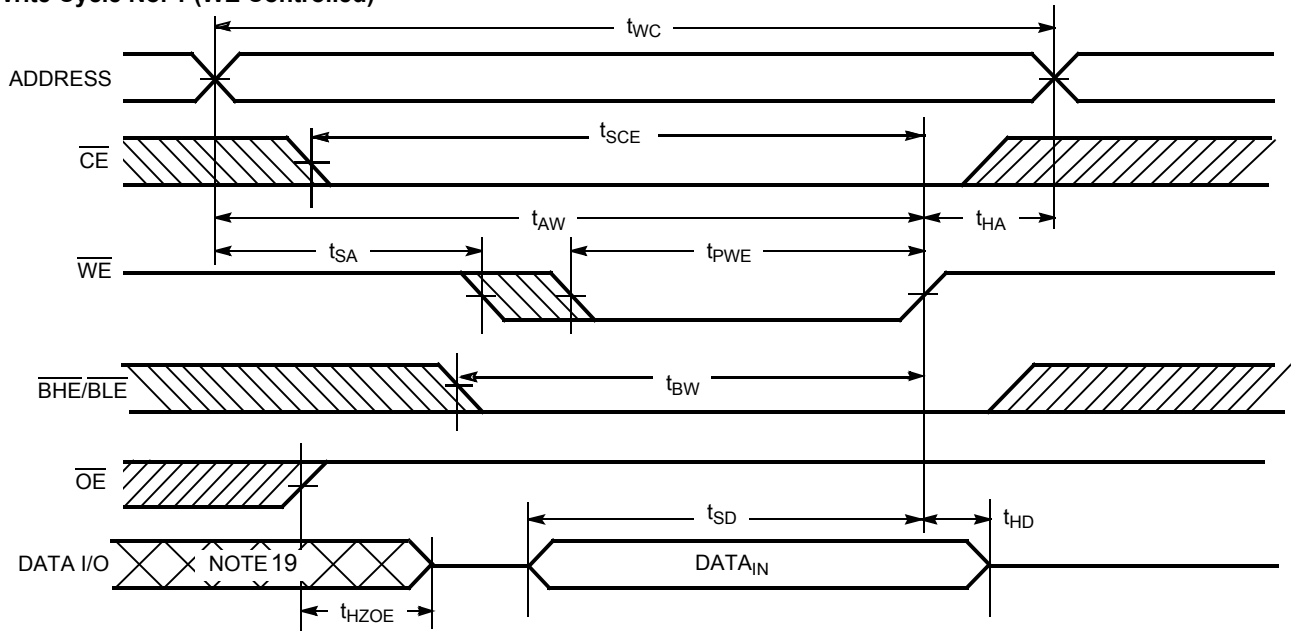
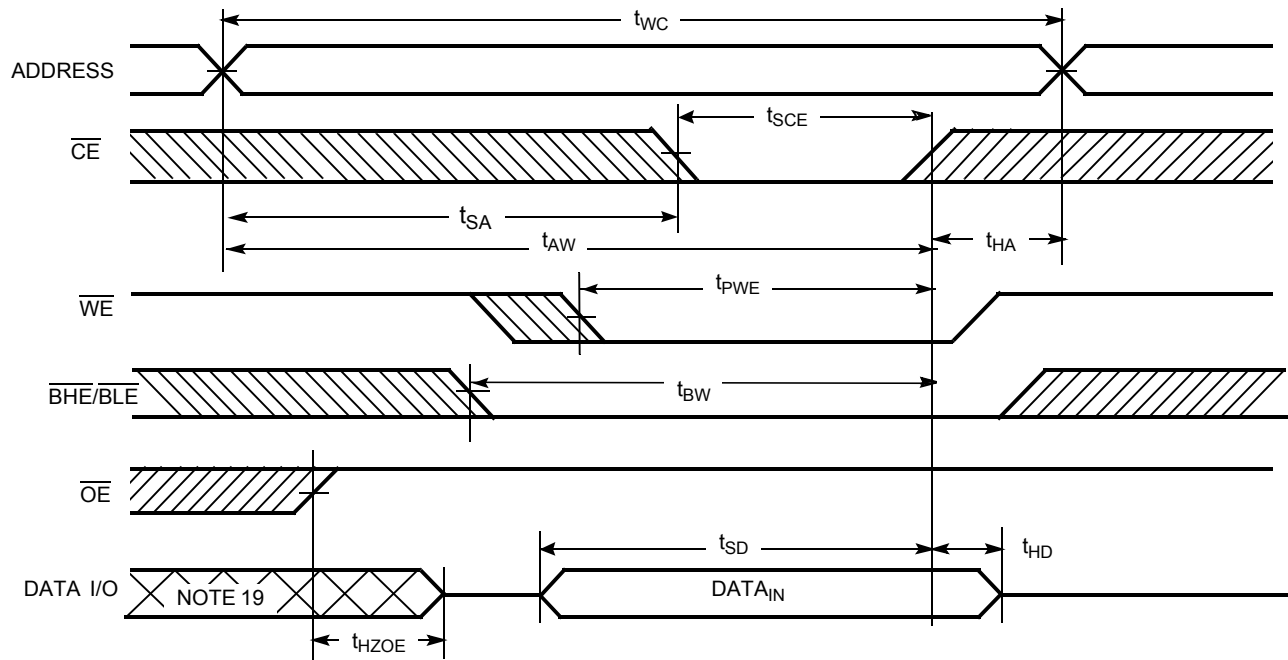


Read Cycle No. 2 ($\overline{\text{OE}}$ Controlled)^[15, 16]

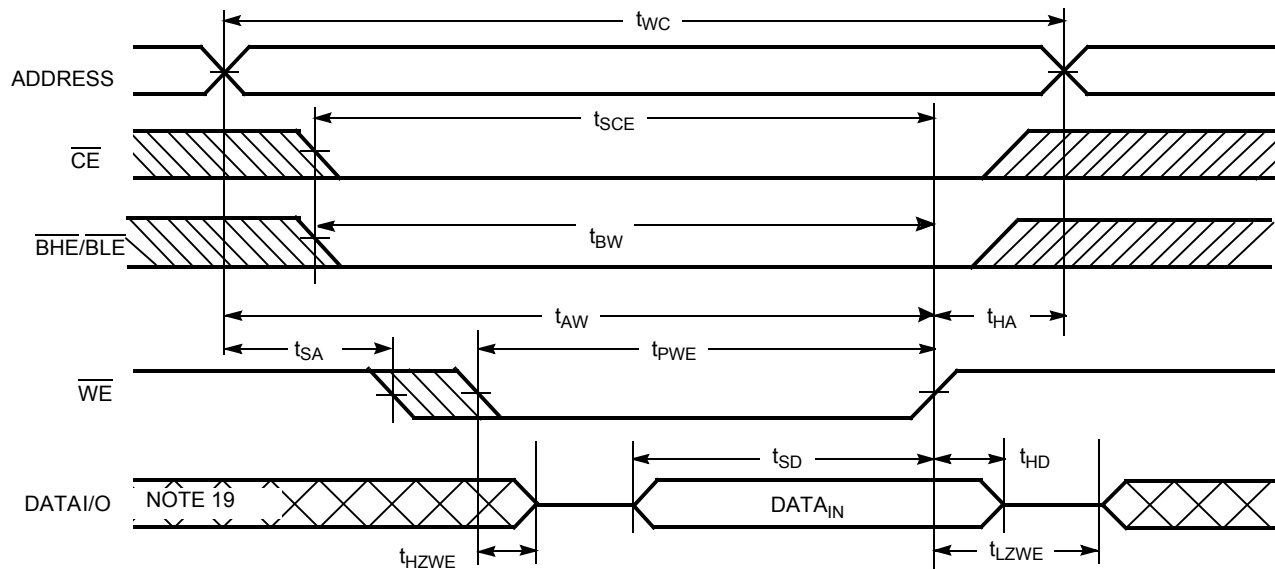
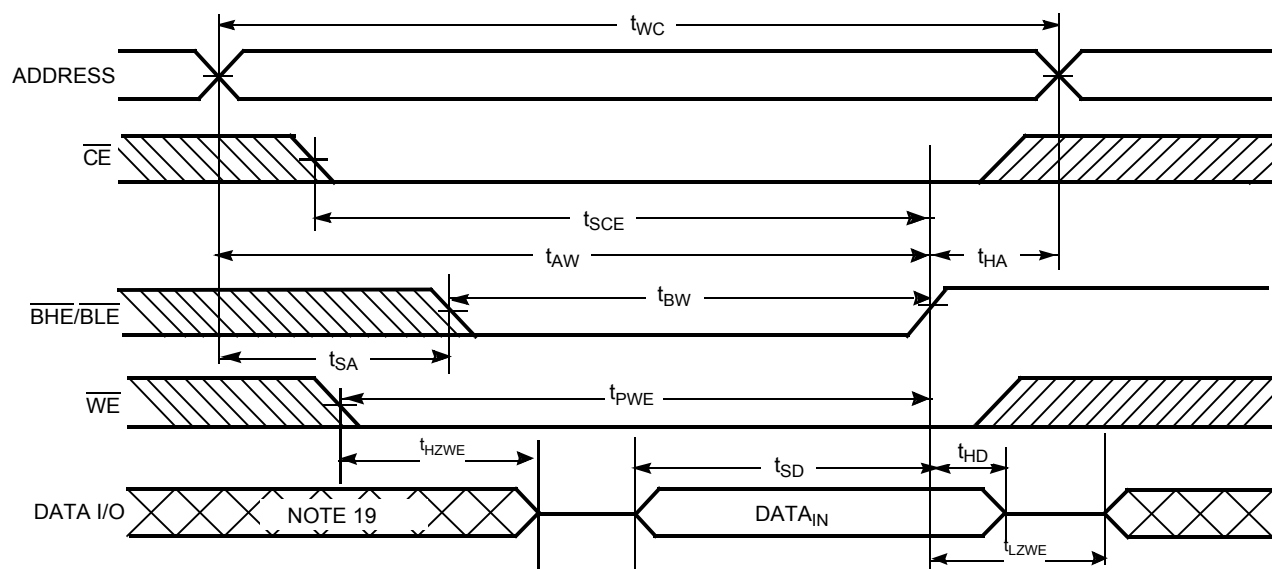


Notes:

14. The device is continuously selected. $\overline{\text{OE}}$, $\overline{\text{CE}} = V_{\text{IL}}$, $\overline{\text{BHE}}$ and/or $\overline{\text{BLE}} = V_{\text{IL}}$.
15. WE is HIGH for read cycle.
16. Address valid prior to or coincident with $\overline{\text{CE}}$ and $\overline{\text{BHE}}$, $\overline{\text{BLE}}$ transition LOW.

Switching Waveforms (continued)
Write Cycle No. 1 ($\overline{\text{WE}}$ Controlled) ^[13, 17, 18]

Write Cycle No. 2 ($\overline{\text{CE}}$ Controlled) ^[13, 17, 18]

Notes:

17. Data I/O is high impedance if $\overline{\text{OE}} = V_{IH}$.
18. If $\overline{\text{CE}}$ goes HIGH simultaneously with $\text{WE} = V_{IH}$, the output remains in a high-impedance state.
19. During this period, the I/Os are in output state and input signals should not be applied.

Switching Waveforms (continued)
Write Cycle No. 3 ($\overline{\text{WE}}$ Controlled, $\overline{\text{OE}}$ LOW) ^[18]

Write Cycle No. 4 ($\overline{\text{BHE/BLE}}$ Controlled, $\overline{\text{OE}}$ LOW) ^[18]


Truth Table

$\overline{\text{CE}}$	$\overline{\text{WE}}$	$\overline{\text{OE}}$	$\overline{\text{BHE}}$	$\overline{\text{BLE}}$	Inputs/Outputs	Mode	Power
H	X	X	X	X	High Z	Deselect/Power-Down	Standby (I_{SB})
X	X	X	H	H	High Z	Deselect/Power-Down	Standby (I_{SB})
L	H	L	L	L	Data Out (I/O_0 – I/O_{15})	Read	Active (I_{CC})
L	H	L	H	L	Data Out (I/O_0 – I/O_7); I/O_8 – I/O_{15} in High Z	Read (Lower byte only)	Active (I_{CC})
L	H	L	L	H	Data Out (I/O_8 – I/O_{15}); I/O_0 – I/O_7 in High Z	Read (Higher byte only)	Active (I_{CC})
L	H	H	L	L	High Z	Output Disabled	Active (I_{CC})
L	H	H	H	L	High Z	Output Disabled	Active (I_{CC})
L	H	H	L	H	High Z	Output Disabled	Active (I_{CC})
L	L	X	L	L	Data In (I/O_0 – I/O_{15})	Write	Active (I_{CC})
L	L	X	H	L	Data In (I/O_0 – I/O_7); I/O_8 – I/O_{15} in High Z	Write (Lower byte only)	Active (I_{CC})
L	L	X	L	H	Data In (I/O_8 – I/O_{15}); I/O_0 – I/O_7 in High Z	Write (Higher byte only)	Active (I_{CC})

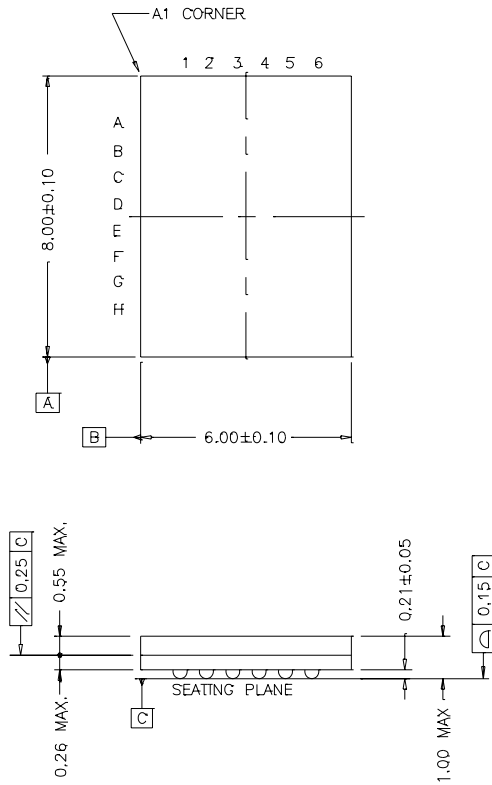
Ordering Information

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
55	CY62147DV18L-55BVI	BV48A	48-ball Fine Pitch BGA (6 mm × 8mm × 1 mm)	Industrial
	CY62147DV18LL-55BVI			
70	CY62147DV18L-70BVI	BV48A	48-ball Fine Pitch BGA (6 mm × 8mm × 1 mm)	Industrial
	CY62147DV18LL-70BVI			
55	CY62147DV18L-55BVXI	BV48A	48-ball Fine Pitch BGA (6 mm × 8mm × 1 mm) Pb-free	Industrial
	CY62147DV18LL-55BVXI			
70	CY62147DV18L-70BVXI	BV48A	48-ball Fine Pitch BGA (6 mm × 8mm × 1 mm) Pb-free	Industrial
	CY62147DV18LL-70BVXI			

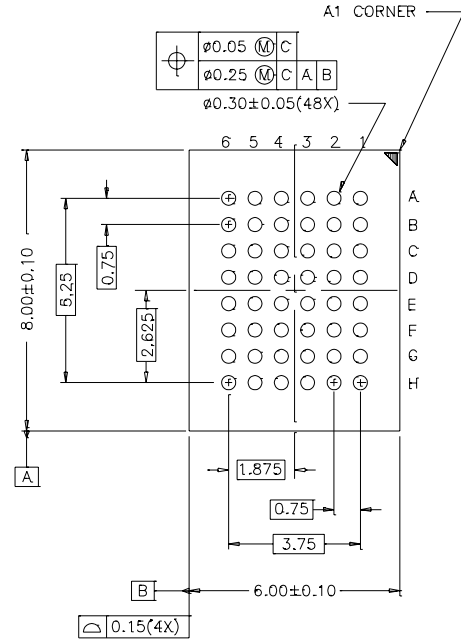
Package Diagram

48-Lead VFBGA (6 x 8 x 1 mm) BV48A

TOP VIEW



BOTTOM VIEW



51-85150-*B

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Document History Page

Document Title: CY62147DV18 MoBL2™ 4-Mb (256K x 16) Static RAM Document Number: 38-05343				
REV.	ECN NO.	Issue Date	Orig. of Change	Description of Change
**	127482	06/17/03	HRT	New Data Sheet
*A	131009	11/26/03	CBD	Changed From Advance to Preliminary
*B	229908	See ECN	AJU	Changed From Preliminary to Final Added 70 ns speed bin Changed V _{CC} MAX spec from 2.20V to 2.25V Modified V _{IH} spec on footnote #6 from V _{CC(MAX)} + 0.5V to V _{CC(MAX)} + 0.75V Changed I _{CC} TYP values from 8 mA to 6 mA Changed I _{CC} MAX values at V _{CC} (max) = 1.95V from 15 mA to 12 mA (L bin) and 10 mA to 8mA (LL bin) Changed I _{CC} MAX values at V _{CC} (max) = 2.25V from 18 mA to 15 mA (L bin) and 12mA to 10 mA (LL bin) With modified V _{CC} MAX spec, changed I _{SB1} and I _{SB2} MAX values from 15 uA to 18 uA (L bin) and 10 uA to 12 uA (LL bin) Modified input and output capacitance values Removed footnote #9 from earlier rev Removed MAX value for V _{DR} Modified t _{HZOE} from 20 ns to 16 ns Added Pb-free ordering information