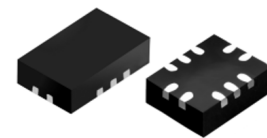


## Dual electronic fuse (eFuse) for 5 V and 12 V rails



QFN10 (2 x 3 mm)

### Features

- 5 V and 12 V channels into one chip
- Output over voltage clamp
- Fixed current limit : 3 A on 5 V, 4 A on 12 V
- Latched-off thermal protection
- Input undervoltage lockout
- Adjustable output voltage slew rate for each channel
- Integrated 40 mΩ Power FETs
- SAS disable pin
- Current monitor output
- QFN10-2x3 package

### Applications

- HD and SSD drives
- Set-top boxes
- DVD and Blu-ray disc drivers

### Description

The **STEF512PUR** is an integrated dual electronic eFuse, designed to protect circuitry on the output from overcurrent and overvoltage events, in those applications requiring hot swap operation and in-rush current control.

The device embeds two independent electronic fuses, one for the 5 V rails and one for the 12 V rails. Thanks to the very low ON-resistance of the integrated power FETs, the voltage drop from the main supply to the load is very low during normal operation.

The startup time can be adjusted by the user for each eFuse, via two small soft-start capacitors, connected to the relevant pins.

In this way the inrush current at startup can be kept under control.

The maximum load current is precisely limited, by utilizing a sense FET topology, to factory-defined values (3 A for 5 V output and 4 A for 12 V output).

The device also provides precise overvoltage clamp for each channel, preventing the load being damaged from power supply failures, and undervoltage lockout (UVLO), assuring that the input voltage is above the minimum operating threshold, before the power device is turned on.

When an overload condition occurs, the **STEF512PUR** limits the output current to the predefined safe value. If the anomalous overload condition persists, the device goes into thermal shutdown, the internal switch is opened and the load disconnected from the power supply.

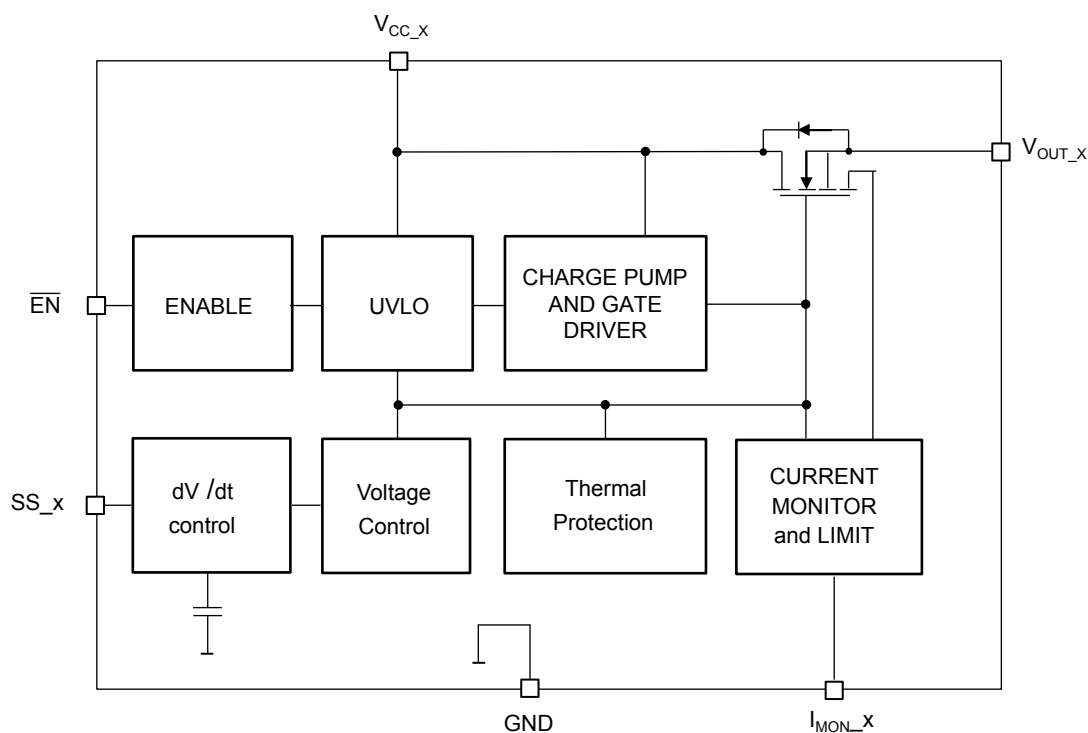
In the QFN10 package two current monitor pins are available, providing continuous information on the load current for each channel.

Maturity status link

[STEF512PUR](#)

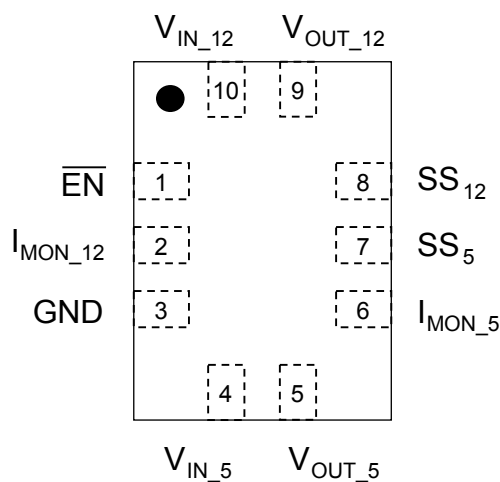
# 1 Diagram

**Figure 1. Block diagram (one channel)**



## 2 Pin configuration

**Figure 2. Pin connection (top view)**

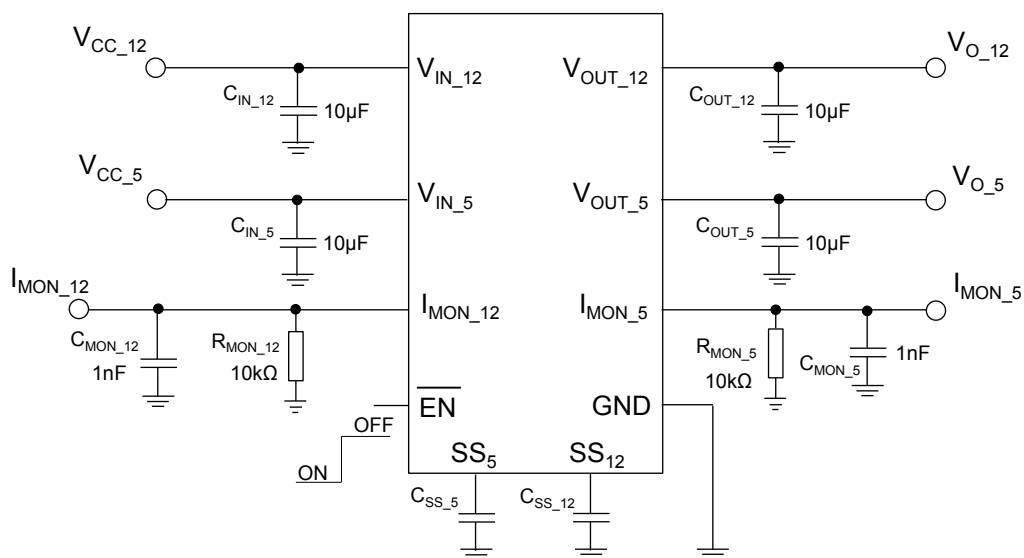


**Table 1. Pin description**

| Symbol          | Pin n° | Description                                                                                                                                                         |
|-----------------|--------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| $V_{IN\_12}$    | 10     | 12 V rail supply voltage                                                                                                                                            |
| $V_{IN\_5}$     | 4      | 5 V rail supply voltage                                                                                                                                             |
| $V_{OUT\_12}$   | 9      | 12 V rail output voltage                                                                                                                                            |
| $V_{OUT\_5}$    | 5      | 5 V rail output voltage                                                                                                                                             |
| $GND$           | 3      | Ground                                                                                                                                                              |
| $\overline{EN}$ | 1      | SAS disable input: set this pin logic-low to turn on the device, high to turn off the device. This pin is internally pulled down via 1 M $\Omega$ resistor.         |
| $SS_5$          | 7      | Soft Start adjustment pin for the 5 V rail. A capacitor must be connected between this pin and GND to program the output voltage slew-rate. Do not leave floating.  |
| $SS_{12}$       | 8      | Soft-start adjustment pin for the 12 V rail. A capacitor must be connected between this pin and GND to program the output voltage slew-rate. Do not leave floating. |
| $I_{MON\_5}$    | 6      | 5 V rail current monitor. Connect a resistor between this pin and GND.                                                                                              |
| $I_{MON\_12}$   | 2      | 12 V rail current monitor. Connect a resistor between this pin and GND.                                                                                             |

### 3 Typical application

Figure 3. Typical application diagram



## 4 Maximum ratings

**Table 2. Absolute maximum ratings**

| Symbol                  | Parameter                         | Value       | Unit |
|-------------------------|-----------------------------------|-------------|------|
| $V_{IN\_5}, V_{IN\_12}$ | Input supply voltage (max 100 ms) | - 0.3 to 25 | V    |
| $V_{IN\_5}, V_{IN\_12}$ | Input supply voltage              | - 0.3 to 20 | V    |
| $V_{OUT\_5}$            | Output voltage <sup>(1)</sup>     | 10          | V    |
| $V_{OUT\_12}$           | Output voltage <sup>(1)</sup>     | 18          | V    |
| $\overline{V_{EN}}$     | Enable pin voltage                | - 0.3 to 7  | V    |
| $SS_x$                  | Soft-start pin voltage            | - 0.3 to 7  | V    |
| $I_{MON\_x}$            | Monitor pin voltage               | - 0.3 to 7  | V    |
| ESD                     | Charge device model               | $\pm 500$   | V    |
|                         | Human body model                  | $\pm 2000$  |      |
| $T_{J-OP}$              | Operating junction temperature    | - 40 to 125 | °C   |
| $T_{J-MAX}$             | Maximum junction temperature      | 150         | °C   |
| $T_{STG}$               | Storage temperature               | - 55 to 150 | °C   |

1. In any case  $V_{OUT} < V_{IN} + 0.3$

**Table 3. Thermal data**

| Symbol     | Parameter                           | Value | Unit |
|------------|-------------------------------------|-------|------|
| $R_{thJA}$ | Thermal resistance junction-ambient | 105   | °C/W |
| $R_{thJC}$ | Thermal resistance junction to case | 16    | °C/W |

## 5 Electrical characteristics

$T_J = 25\text{ }^{\circ}\text{C}$ ,  $V_{IN\_5} = 5\text{ V}$ ,  $V_{IN\_12} = 12\text{ V}$ ,  $\overline{EN} = 0\text{ V}$ ;  $C_{IN} = 10\text{ }\mu\text{F}$ ;  $C_{OUT} = 10\text{ }\mu\text{F}$ ; unless otherwise specified.

**Table 4. Electrical characteristics**

| Symbol                 | Parameter                                                        | Test conditions                                                 | Min. | Typ. | Max. | Unit            |
|------------------------|------------------------------------------------------------------|-----------------------------------------------------------------|------|------|------|-----------------|
| <b>5 V eFuse</b>       |                                                                  |                                                                 |      |      |      |                 |
| $V_{Clamp\_5}$         | Output clamping voltage                                          | $V_{IN\_5} = 8\text{ V}$ , $I_{OUT} = 5\text{ mA}$              | 5.5  | 5.7  | 5.9  | V               |
| $V_{UVLO\_5}$          | Undervoltage lockout                                             | Turn-on, voltage rising                                         | 4.25 | 4.35 | 4.45 | V               |
| $V_{Hyst\_5}$          | UVLO hysteresis                                                  | Turn-off, voltage falling                                       |      | 1.78 |      | V               |
| $R_{DSon\_5}$          | On-resistance                                                    | $T_J = 25\text{ }^{\circ}\text{C}$                              |      | 36   |      | m $\Omega$      |
|                        |                                                                  | $T_J = 125\text{ }^{\circ}\text{C}$                             |      |      | 50   |                 |
| $I_{L\_5}$             | Off state leakage current                                        | $\overline{V_{EN}} = 5\text{ V}$ , $V_{OUT\_5} = \text{GND}$    |      | 1    | 5    | $\mu\text{A}$   |
| $I_{D5}$               | Maximum continuous current                                       | $T_A = 25\text{ }^{\circ}\text{C}$                              |      | 2.5  |      | A               |
| $I_{Short\_5}$         | Short-circuit current limit                                      |                                                                 | 0.6  | 1    | 1.4  | A               |
| $I_{Lim\_5}$           | Overload current limit                                           |                                                                 | 2.5  | 3    | 3.3  | A               |
| $dV/dt\_5$             | Output voltage ramp time                                         | From 10 % to 90 % of $V_{OUT}$<br>$C_{dv/dt} = 100\text{ nF}$   | 11   | 13   | 15   | ms              |
| $A_{I\_5}$             | Current monitor output current gain, $I_{MON\_5} / I_{OUT\_5}$   | $I_{OUT\_5} > 200\text{ mA}$                                    | 27   | 30   | 33   | $\mu\text{A/A}$ |
| <b>12 V eFuse</b>      |                                                                  |                                                                 |      |      |      |                 |
| $V_{Clamp\_12}$        | Output clamping voltage                                          | $V_{IN\_12} = 17\text{ V}$ , $I_{OUT} = 5\text{ mA}$            | 14.5 | 15   | 15.5 | V               |
| $V_{UVLO\_12}$         | Undervoltage lockout                                             | Turn-on, voltage rising                                         | 9.4  | 9.7  | 10   | V               |
| $V_{Hyst\_12}$         | UVLO hysteresis (12 V rail)                                      | Turn-off, voltage falling                                       |      | 2    |      | V               |
| $R_{DSon\_12}$         | On-resistance (12 V rail)                                        | $T_J = 25\text{ }^{\circ}\text{C}$                              |      | 40   |      | m $\Omega$      |
|                        |                                                                  | $T_J = 125\text{ }^{\circ}\text{C}$                             |      |      | 70   |                 |
| $I_{L\_12}$            | Off state leakage current                                        | $\overline{V_{EN}} = 5\text{ V}$ , $V_{OUT\_12} = \text{GND}$   |      | 1    | 5    | $\mu\text{A}$   |
| $I_{D12}$              | Continuous current <sup>(1)(2)</sup>                             | $T_A = 25\text{ }^{\circ}\text{C}$                              |      | 3.5  |      | A               |
| $I_{Short\_12}$        | Short-circuit current limit                                      |                                                                 |      | 1.8  |      | A               |
| $I_{Lim\_12}$          | Overload current limit                                           |                                                                 | 3.6  | 4    | 4.5  | A               |
| $dV/dt\_12$            | Output voltage ramp time                                         | From 10 % to 90 % of $V_{OUT}$ ,<br>$C_{dv/dt} = 100\text{ nF}$ | 10   | 12   | 14   | ms              |
| $A_{I\_12}$            | Current monitor output current gain, $I_{MON\_12} / I_{OUT\_12}$ | $I_{OUT\_12} \geq 200\text{ mA}$                                | 27   | 30   | 33   | $\mu\text{A/A}$ |
| <b>Common features</b> |                                                                  |                                                                 |      |      |      |                 |
| $V_{IL}$               | Low level input voltage                                          | Output enabled                                                  |      |      | 0.7  | V               |
| $V_{IH}$               | High level input voltage                                         | Output disabled                                                 | 2.1  |      |      | V               |
| $R_P$                  | Pull-down resistor                                               |                                                                 |      | 1000 |      | k $\Omega$      |
| $I_q$                  | Quiescent current (excluding $\overline{EN}$ current)            | Device operating                                                |      | 250  | 1000 | $\mu\text{A}$   |

| Symbol                    | Parameter                                             | Test conditions           | Min. | Typ. | Max. | Unit        |
|---------------------------|-------------------------------------------------------|---------------------------|------|------|------|-------------|
| $I_q$                     | Quiescent current (excluding $\overline{EN}$ current) | Off-state, = 5 V          |      | 40   | 80   | $\mu A$     |
| $\overline{I_{EN}}$       | Enable pin current                                    | $V_{\overline{EN}} = 5 V$ |      | 5    | 10   | $\mu A$     |
| <b>Thermal protection</b> |                                                       |                           |      |      |      |             |
| TSD                       | Shutdown temperature <sup>(1)</sup>                   |                           |      | 165  |      | $^{\circ}C$ |
|                           | Hysteresis                                            |                           |      | 20   |      |             |

1. *Guaranteed by design, but not tested in production.*
2. *The maximum continuous current is the current level above which the control loop starts increasing the ON resistance of the pass element.*

**Table 5. Recommended operating condition**

| Symbol    | Parameter          | Test Conditions | Min. | Typ. | Max. | Unit    |
|-----------|--------------------|-----------------|------|------|------|---------|
| $C_{IN}$  | Input capacitance  | Stability       | 1    | 47   |      | $\mu F$ |
| $C_{OUT}$ | Output capacitance |                 | 10   | 47   |      |         |

## 6 Device functional description

The STEF512 embeds a 5 V and a 12 V electronic fuses (eFuses). Each eFuse is an intelligent load switch, able limit the voltage or the current during fault events, such as input overvoltage or output overload respectively. For this purpose it contains 2 analogue control loops, one limiting the output voltage and one limiting the input current. The current limiting loop is also used during the start-up phase of the eFuse to limit the inrush current into the output capacitor.

During normal operation the eFuse behaves as a low-resistance Power FET, therefore the output voltage follows the input one. In case of overvoltage or overcurrent event, the eFuse limits the  $V_{GS}$  of the internal FET, in order to clamp the output voltage or current respectively. During such events the die temperature increases due to the power dissipation and so, if the fault persists and the overtemperature threshold is overcome, the device goes into thermal shutdown, the internal FET is turned-off and the load disconnected from the power supply.

Once the eFuse is in thermal shutdown, it does not restart automatically. The eFuse can be restarted manually by toggling the  $\overline{EN}$  pin or performing a power-up cycle, (this will be effective as soon as the die temperature drops by at least the overtemperature hysteresis).

Each eFuse provides factory-trimmed undervoltage lockout feature and user-adjustable output voltage rise time.

### 6.1 Undervoltage lockout

Undervoltage lockout circuit prevents each eFuse to turn-on if the supply voltage is below the UVLO rising threshold. During operation, if the input voltage falls below ( $V_{UVLO\_x} - V_{Hyst\_x}$ ), the output of the relevant channel is turned off.

If the supply voltage comes back into the operative range, the relevant channel restarts with soft-start cycle.

### 6.2 Startup sequence and voltage clamp

The typical start-up sequence of each eFuse is as follows:

- The power supply is connected to the  $V_{IN\_x}$  pin and higher than the undervoltage lockout threshold
- The disable pin  $\overline{EN}$  is asserted by the user to low logic level (or left floating), enabling the device
- Typically, 1.2 ms after the eFuse starts ramping up the output voltage
- Each channel will ramp up with a rate set by the relevant  $C_{SSx}$
- If the input voltage continues rising, above the overvoltage threshold ( $V_{Clamp\_x}$ ), as a consequence of a failure in the power supply, the eFuse limits the output voltage to  $V_{Clamp\_x}$ . The eFuse keeps operating in this state until it hits its overtemperature threshold and shuts down

### 6.3 Current limit function

Each eFuse provides 2 kinds of current limit protection mechanisms:

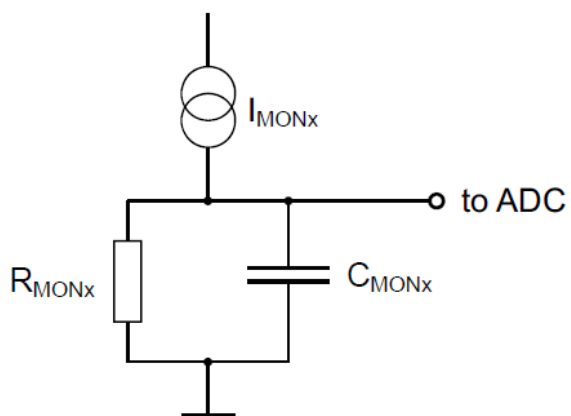
- In case of overload, the device starts increasing the power MOS resistance. The overload current limit ( $I_{Lim\_x}$ ) is 3 A typ. for the 5 V fuse and 4 A (typ.) for the 12 V
- In the case of strong overload or short circuit, the short-circuit current limit is activated and the current is clamped to  $I_{Short\_x}$ : 1 A typ. on 5 V channel and 1.8 A typ. on 12 V channel

### 6.4 eFuse current monitor

The eFuse is equipped with current monitoring capability that allows the host processor to read the current flowing through each channel. An  $I_{MON\_x}$  ( $x = 5, 12$ ) current proportional to the load current flowing through the eFuse is imposed on an external  $R_{MON\_x}$ , converting the sensing current into voltage for further processing by the ADC. An external RC filter is used to provide a stable signal (see figure below).

The current monitoring amplifier gain ( $A_{I\_x} = I_{MON\_x} / I_{OUT\_x}$ ) is typically 30  $\mu A/A$ , as defined in the electrical characteristic [Table 4. Electrical characteristics](#).

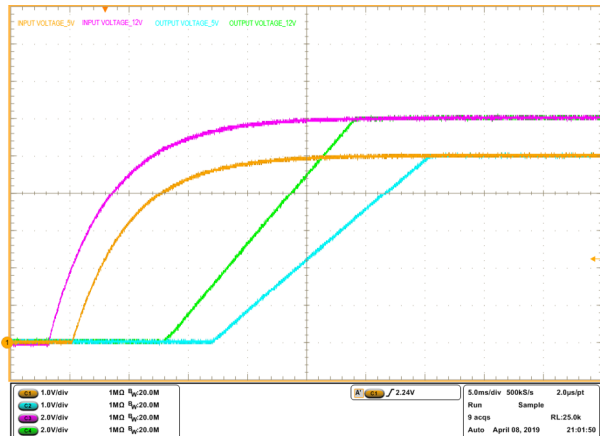
Figure 4. Current monitor simplified circuit



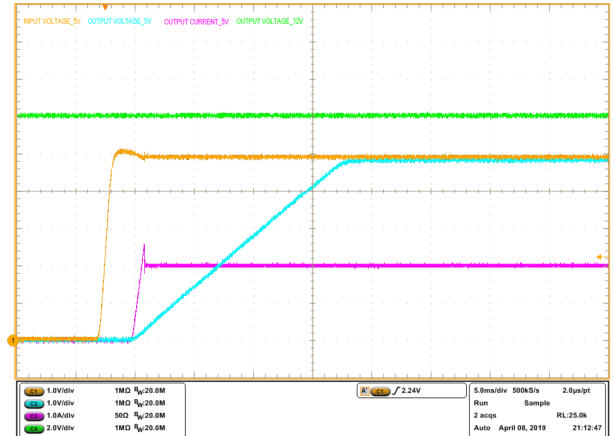
## 7 Typical characteristics

The following plots are referred to the typical application circuit and, unless otherwise noted, at  $T_A = 25\text{ }^{\circ}\text{C}$ .

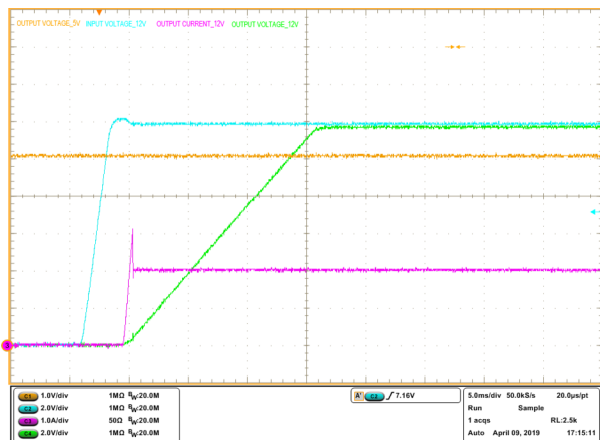
**Figure 5. Start-up no load from  $V_{CC}$**



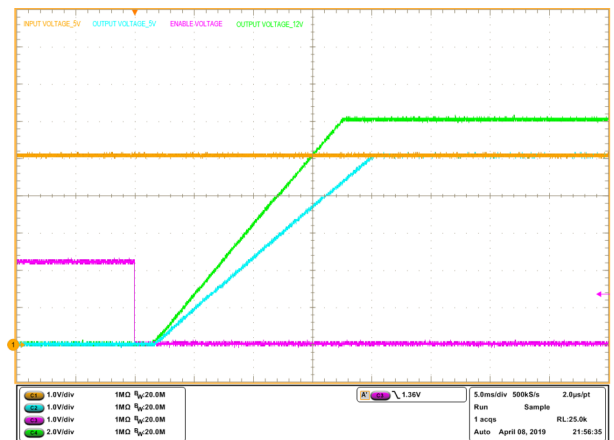
**Figure 6. Out5 start-up with 2 A load**

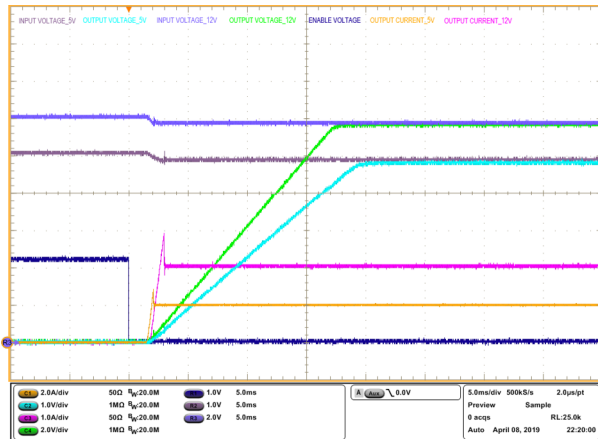
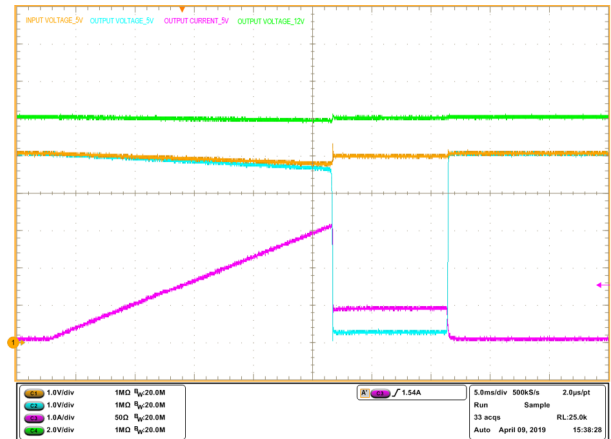
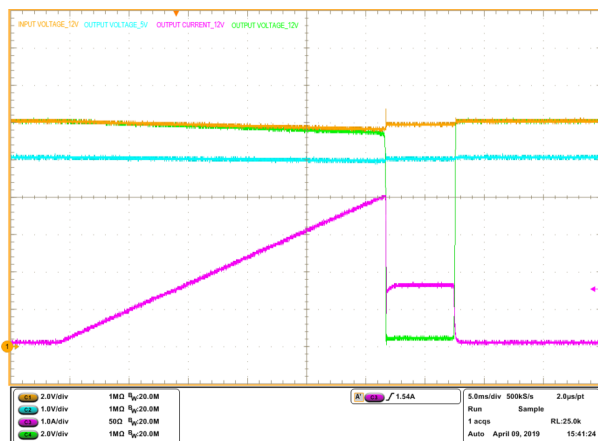
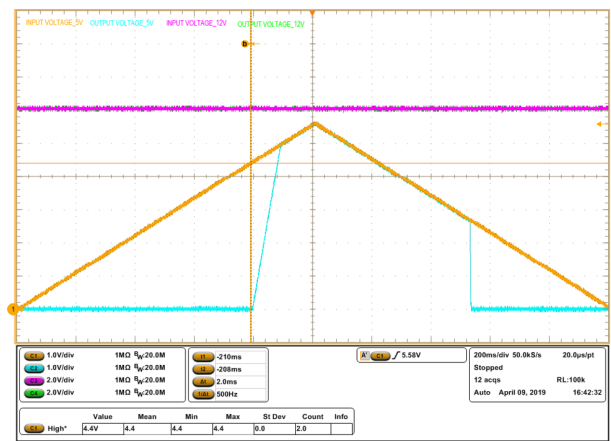
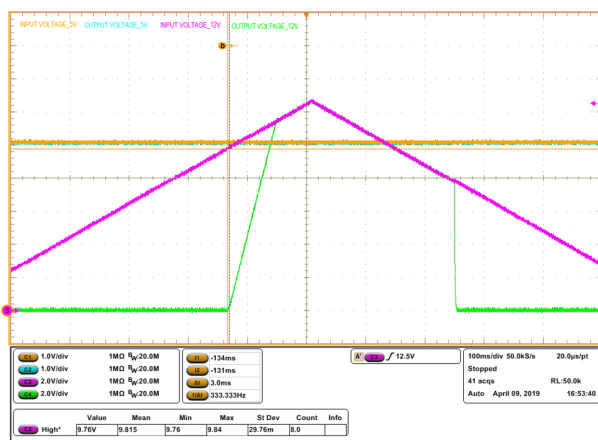
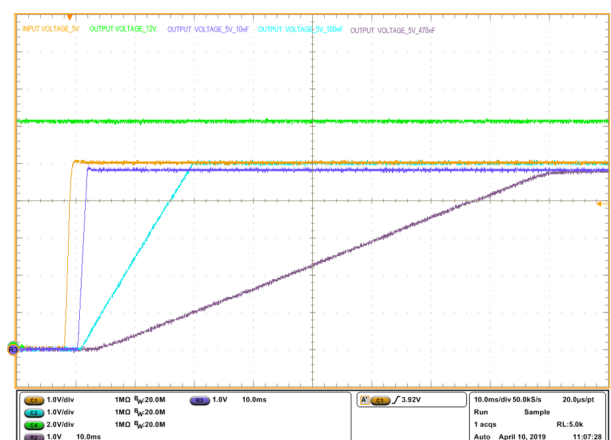


**Figure 7. Out12 start-up with 2 A**

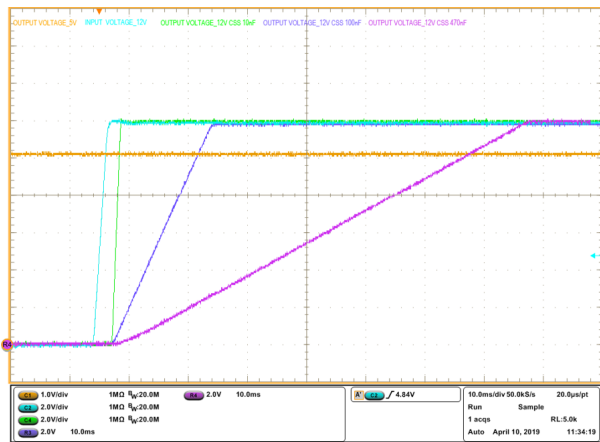


**Figure 8. Start-up by EN, no load**

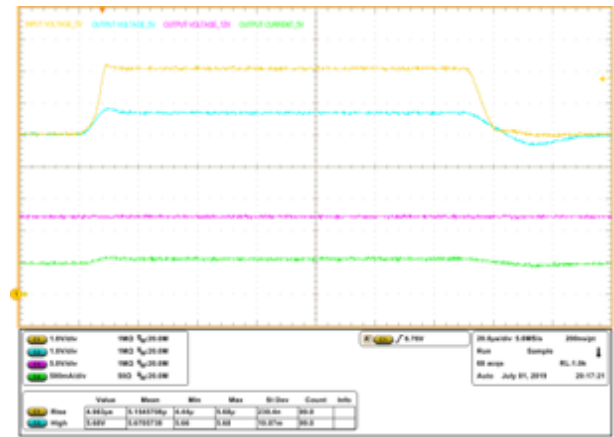


**Figure 9. Start\_up by En @ 2 A load**

**Figure 10. Out5 current limit and short**

**Figure 11. Out12 current limit and short**

**Figure 12. Out5 UVLO rising**

**Figure 13. Out12 UVLO rising**

**Figure 14. Out5 start-up vs. C<sub>SS</sub>**


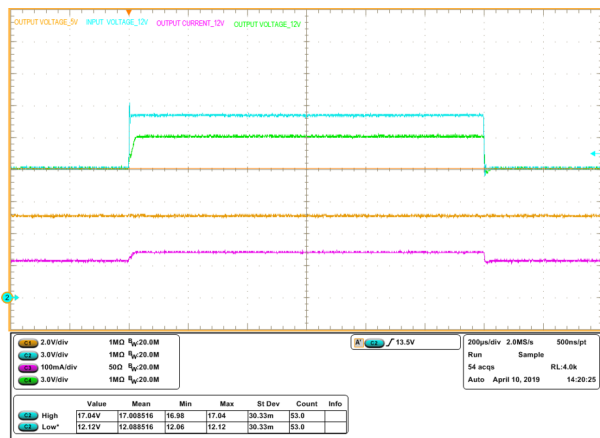
**Figure 15. Out12 start-up vs. C<sub>SS</sub>**



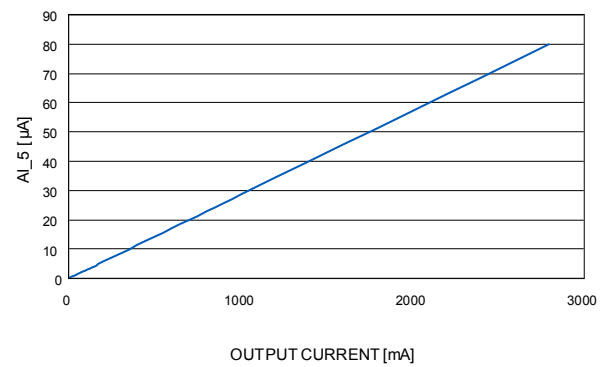
**Figure 16. Out5 voltage clamp**



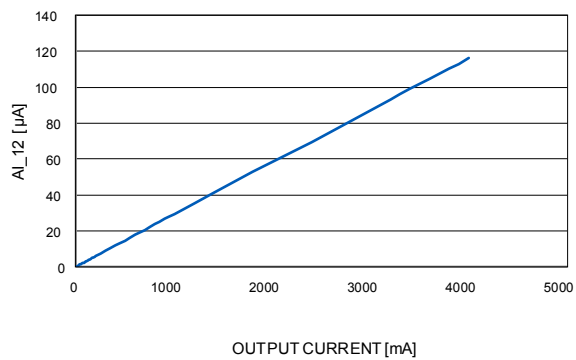
**Figure 17. Out12 voltage clamp**



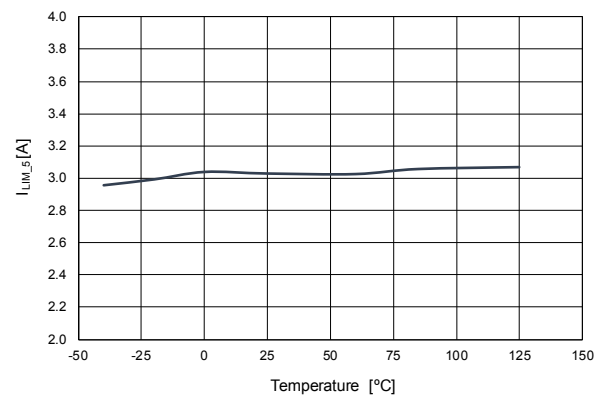
**Figure 18. I<sub>mon5</sub> gain**



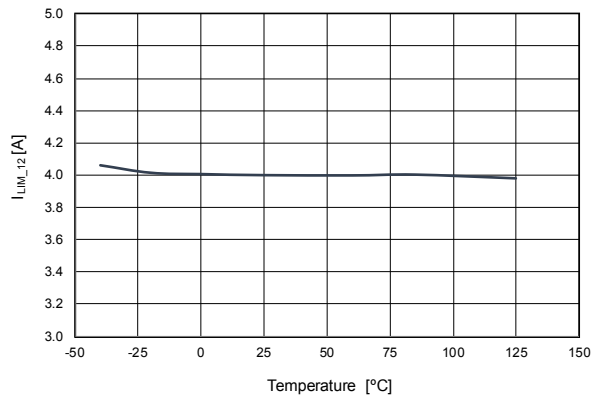
**Figure 19. I<sub>mon12</sub> Gain**



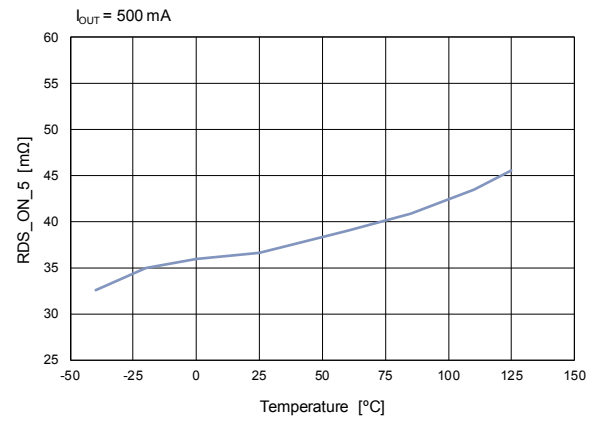
**Figure 20. 5 V channel I<sub>lim</sub> vs. temperature**



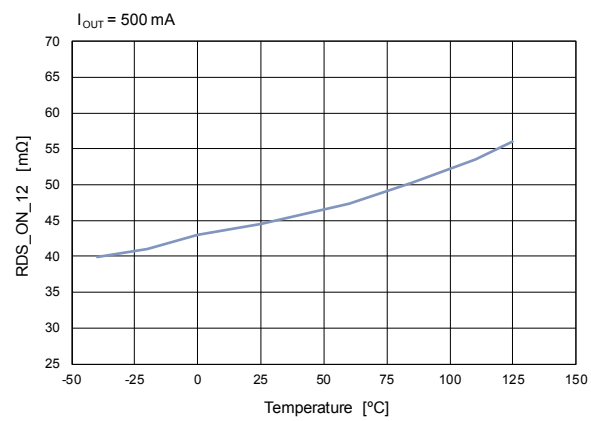
**Figure 21. 12 V channel  $I_{lim}$  vs. temperature**



**Figure 22. 5 V channel  $R_{DS\_ON}$  vs. temperature**



**Figure 23. 12 V channel  $R_{DS\_ON}$  vs. temperature**

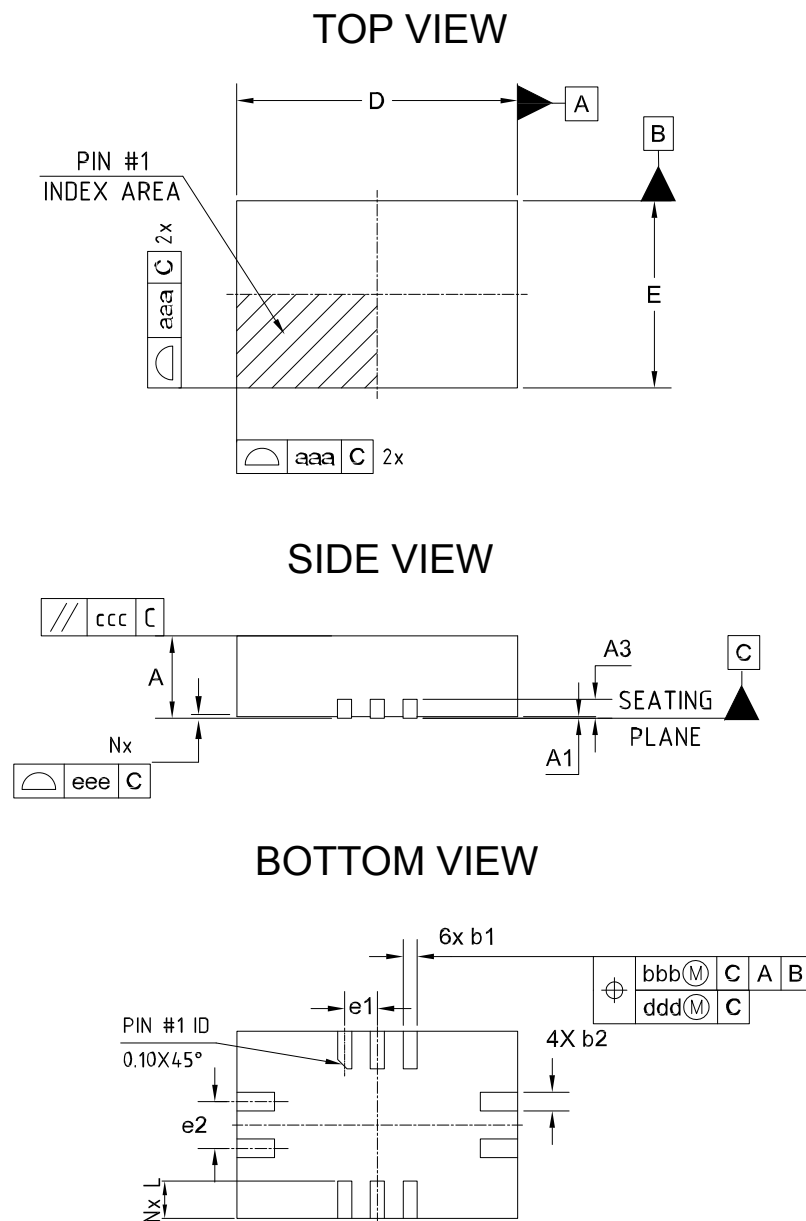


## 8 Package information

In order to meet environmental requirements, ST offers these devices in different grades of **ECOPACK** packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions and product status are available at: [www.st.com](http://www.st.com). ECOPACK is an ST trademark.

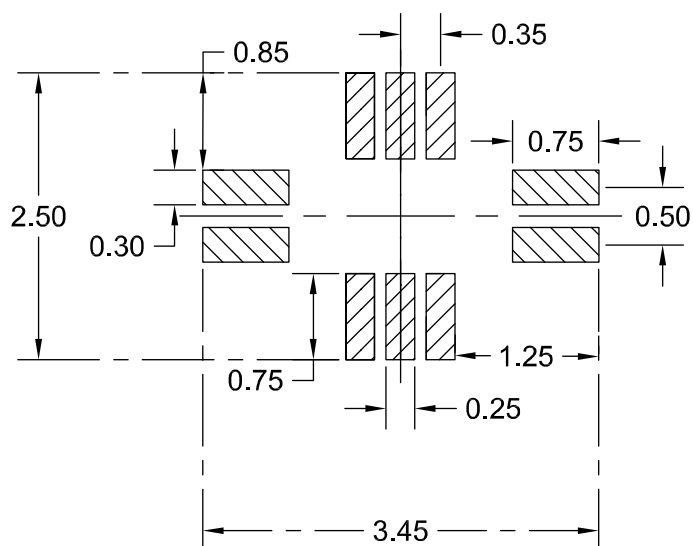
### 8.1 QFN10 (2 x 3 mm) package information

**Figure 24. QFN10 (2 x 3 mm) package outline**



**Table 6. QFN10 (2 x 3 mm) mechanical data**

| Dim. | mm         |      |      |
|------|------------|------|------|
|      | Min.       | Typ. | Max. |
| A    | 0.70       | 0.75 | 0.80 |
| A1   | 0          | 0.02 | 0.05 |
| A3   | 0.203 ref. |      |      |
| b1   | 0.10       | 0.15 | 0.20 |
| b2   | 0.15       | 0.20 | 0.25 |
| D    | 3.00 BSC   |      |      |
| E    | 2.00 BSC   |      |      |
| e1   | 0.35 BSC   |      |      |
| e2   | 0.50 BSC   |      |      |
| L    | 0.30       | 0.40 | 0.50 |
| aaa  |            | 0.05 |      |
| bbb  | 0.10       |      |      |
| ccc  | 0.10       |      |      |
| ddd  | 0.05       |      |      |
| eee  | 0.08       |      |      |

**Figure 25. QFN10 (2 x 3 mm) recommended footprint**


## 9 Ordering information

**Table 7. Order codes**

| Order code | Finish good    | Package | Current limit configuration | Marking |
|------------|----------------|---------|-----------------------------|---------|
| STEF512PUR | STEF512PUR\$7Q | QFN10   | 3 A on 5 V , 4 A on 12 V    | W51     |

## Revision history

**Table 8. Document revision history**

| Date        | Revision | Changes                                                                                        |
|-------------|----------|------------------------------------------------------------------------------------------------|
| 07-Jan-2020 | 1        | Initial release.                                                                               |
| 13-Jan-2020 | 2        | Added $A_{I\_5}$ and $A_{I\_12}$ Min. and Max. values in Table 4. Electrical characteristics.  |
| 21-Sep-2020 | 3        | Updated $I_{LIM\_5}$ Min. value in Table 4. Electrical characteristics.<br>Minor text changes. |

## Contents

|          |                                            |           |
|----------|--------------------------------------------|-----------|
| <b>1</b> | <b>Diagram .....</b>                       | <b>2</b>  |
| <b>2</b> | <b>Pin configuration .....</b>             | <b>3</b>  |
| <b>3</b> | <b>Typical application.....</b>            | <b>4</b>  |
| <b>4</b> | <b>Maximum ratings .....</b>               | <b>5</b>  |
| <b>5</b> | <b>Electrical characteristics.....</b>     | <b>6</b>  |
| <b>6</b> | <b>Device functional description .....</b> | <b>8</b>  |
| 6.1      | Undervoltage lockout .....                 | 8         |
| 6.2      | Startup sequence and voltage clamp .....   | 8         |
| 6.3      | Current limit function .....               | 8         |
| 6.4      | eFuse current monitor.....                 | 8         |
| <b>7</b> | <b>Typical characteristics .....</b>       | <b>10</b> |
| <b>8</b> | <b>Package information.....</b>            | <b>14</b> |
| 8.1      | QFN10 (2 x 3 mm) package information ..... | 14        |
| <b>9</b> | <b>Ordering information .....</b>          | <b>16</b> |
|          | <b>Revision history .....</b>              | <b>17</b> |

## List of tables

|                 |                                            |    |
|-----------------|--------------------------------------------|----|
| <b>Table 1.</b> | Pin description . . . . .                  | 3  |
| <b>Table 2.</b> | Absolute maximum ratings . . . . .         | 5  |
| <b>Table 3.</b> | Thermal data . . . . .                     | 5  |
| <b>Table 4.</b> | Electrical characteristics . . . . .       | 6  |
| <b>Table 5.</b> | Recommended operating condition . . . . .  | 7  |
| <b>Table 6.</b> | QFN10 (2 x 3 mm) mechanical data . . . . . | 15 |
| <b>Table 7.</b> | Order codes . . . . .                      | 16 |
| <b>Table 8.</b> | Document revision history . . . . .        | 17 |

## List of figures

|            |                                           |    |
|------------|-------------------------------------------|----|
| Figure 1.  | Block diagram (one channel)               | 2  |
| Figure 2.  | Pin connection (top view)                 | 3  |
| Figure 3.  | Typical application diagram               | 4  |
| Figure 4.  | Current monitor simplified circuit        | 9  |
| Figure 5.  | Start-up no load from $V_{CC}$            | 10 |
| Figure 6.  | Out5 start-up with 2 A load               | 10 |
| Figure 7.  | Out12 start-up with 2 A                   | 10 |
| Figure 8.  | Start-up by EN, no load                   | 10 |
| Figure 9.  | Start-up by En @ 2 A load                 | 11 |
| Figure 10. | Out5 current limit and short              | 11 |
| Figure 11. | Out12 current limit and short             | 11 |
| Figure 12. | Out5 UVLO rising                          | 11 |
| Figure 13. | Out12 UVLO rising                         | 11 |
| Figure 14. | Out5 start-up vs. $C_{SS}$                | 11 |
| Figure 15. | Out12 start-up vs. $C_{SS}$               | 12 |
| Figure 16. | Out5 voltage clamp                        | 12 |
| Figure 17. | Out12 voltage clamp                       | 12 |
| Figure 18. | I <sub>mon5</sub> gain                    | 12 |
| Figure 19. | I <sub>mon12</sub> Gain                   | 12 |
| Figure 20. | 5 V channel $I_{lim}$ vs. temperature     | 12 |
| Figure 21. | 12 V channel $I_{lim}$ vs. temperature    | 13 |
| Figure 22. | 5 V channel $R_{DS\_ON}$ vs. temperature  | 13 |
| Figure 23. | 12 V channel $R_{DS\_ON}$ vs. temperature | 13 |
| Figure 24. | QFN10 (2 x 3 mm) package outline          | 14 |
| Figure 25. | QFN10 (2 x 3 mm) recommended footprint    | 15 |

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