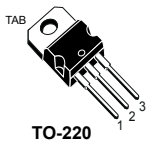
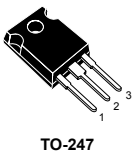
STP15NK50Z, STW15NK50Z

Datasheet

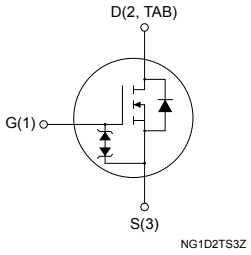
N-channel 500 V, 300 mΩ typ., 14 A SuperMESH Power MOSFETs in TO-220 and TO-247 packages



TO-220



TO-247



Product status links
STP15NK50Z
STW15NK50Z

Product summary	
Order code	**STP15NK50Z**
Marking	P15NK50Z
Package	TO-220
Packing	Tube
Order code	**STW15NK50Z**
Marking	W15NK50Z
Package	TO-247
Packing	Tube

Features

Order code	V_{DS}	$R_{DS(on)}$ max.	I_D
STP15NK50Z	500 V	340 mΩ	14 A
STW15NK50Z			

- Extremely high dv/dt capability
- Improved ESD capability
- 100% avalanche tested
- Gate charge minimized
- Very low intrinsic capacitance
- Zener-protected

Applications

- Switching applications

Description

These high-voltage devices are Zener-protected N-channel Power MOSFETs developed using the SuperMESH technology by STMicroelectronics, an optimization of the well-established PowerMESH. In addition to a significant reduction in on-resistance, these devices are designed to ensure a high level of dv/dt capability for the most demanding applications.

1 Electrical ratings

Table 1. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{DS}	Drain-source voltage	500	V
V_{GS}	Gate-source voltage	±30	V
I_D	Drain current (continuous) at T_C = 25 °C	14	A
	Drain current (continuous) at T_C = 100 °C	8.8	
I_{DM}(1)	Drain current (pulsed)	56	A
P_{TOT}	Total power dissipation at T_C = 25 °C	160	W
ESD	Gate-source human body model (C = 100 pF, R = 1.5 kΩ)	4	kV
dv/dt(2)	Peak diode recovery voltage slope	4.5	V/ns
T_J	Operating junction temperature range	-50 to 150	°C
T_{stg}	Storage temperature range		

1. *Pulse width limited by safe operating area.*
2. *I_{SD} ≤ 14 A, di/dt ≤ 200 A/µs, V_{DS} (peak) < $V_{(BR)DSS}$.*

Table 2. Thermal data

Symbol	Parameter	Value		Unit
		TO-220	TO-247	
R_{thJC}	Thermal resistance, junction-to-case	0.78		°C/W
R_{thJA}	Thermal resistance, junction-to-ambient	62.5	50	°C/W

Table 3. Avalanche characteristics

Symbol	Parameter	Value	Unit
I_{AR}	Avalanche current, repetitive or not-repetitive (pulse width limited by T_J max.)	14	A
E_{AS}	Single pulse avalanche energy (starting T_J = 25 °C, I_D = I_{AR}, V_{DD} = 50 V)	300	mJ

2 Electrical characteristics

T_C = 25 °C unless otherwise specified.

Table 4. On/off states

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	I_D = 1 mA, V_{GS} = 0 V	500			V
I_{DSS}	Zero gate voltage drain current	V_{GS} = 0 V, V_{DS} = 500 V			1	µA
		V_{GS} = 0 V, V_{DS} = 500 V, T_C = 125 °C(1)			50	
I_{GSS}	Gate-body leakage current	V_{DS} = 0 V, V_{GS} = ±20 V			±10	µA
$V_{GS(th)}$	Gate threshold voltage	V_{DS} = V_{GS}, I_D = 100 µA	3	3.75	4.5	V
$R_{DS(on)}$	Static drain-source on-resistance	V_{GS} = 10 V, I_D = 7 A		300	340	mΩ

1. *Specified by design, not tested in production.*

Table 5. Dynamic

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
C_{iss}	Input capacitance	V_{DS} = 25 V, f = 1 MHz, V_{GS} = 0 V	-	2260		pF
C_{oss}	Output capacitance		-	264		pF
C_{rss}	Reverse transfer capacitance		-	64		pF
$C_{oss\ eq.}$ (1)	Equivalent output capacitance	V_{DS} = 0 to 400 V, V_{GS} = 0 V	-	150		pF
Q_g	Total gate charge	V_{DD} = 400 V, I_D = 14 A, V_{GS} = 0 to 10 V (see the Figure 16. Test circuit for gate charge behavior)	-	76	106(2)	nC
Q_{gs}	Gate-source charge		-	15		nC
Q_{gd}	Gate-drain charge		-	40		nC

1. *$C_{oss\ eq.}$ is defined as a constant equivalent capacitance giving the same charging time as C_{oss} when V_{DS} increases from 0 to 80% V_{DSS}.*
2. *Specified by design, not tested in production.*

Table 6. Switching times

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on delay time	V_{DD} = 250 V, I_D = 7 A, R_G = 4.7 Ω, V_{GS} = 10 V (see the Figure 15. Test circuit for resistive load switching times and Figure 20. Switching time waveform)	-	20	-	ns
t_r	Rise time		-	23	-	ns
$t_{d(off)}$	Turn-off delay time		-	62	-	ns
t_f	Fall time		-	15	-	ns

Table 7. Source-drain diode

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
I_{SD}	Source-drain current		-		14	A
I_{SDM} (1)	Source-drain current (pulsed)		-		56	A
V_{SD} (2)	Forward on voltage	I_{SD} = 14 A, V_{GS} = 0 V	-		1.6	V
t_{rr}	Reverse recovery time	I_{SD} = 14 A, di/dt = 100 A/µs, V_{DD} = 29 V, T_J = 150 °C (see the Figure 17. Test circuit for inductive load switching and diode recovery times)	-	428		ns
Q_{rr}	Reverse recovery charge		-	4.2		µC
I_{RRM}	Reverse recovery current		-	20		A

1. *Pulse width is limited by safe operating area.*
2. *Pulsed: pulse duration = 300 µs, duty cycle 1.5%.*

2.1 Electrical characteristics (curves)

Figure 1. Safe operating area for TO-220

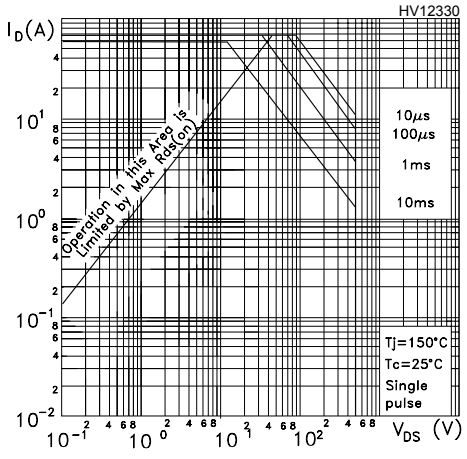


Figure 2. Normalized transient thermal impedance for TO-220

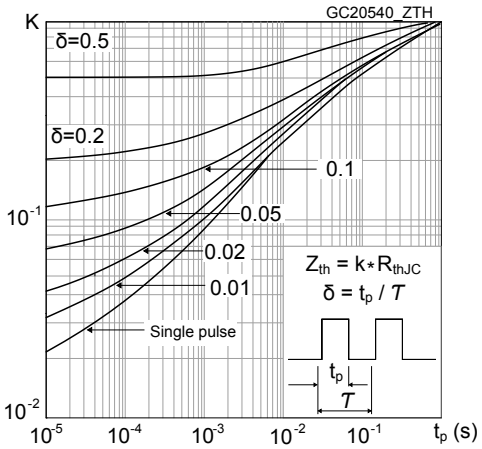


Figure 3. Safe operating area for TO-247

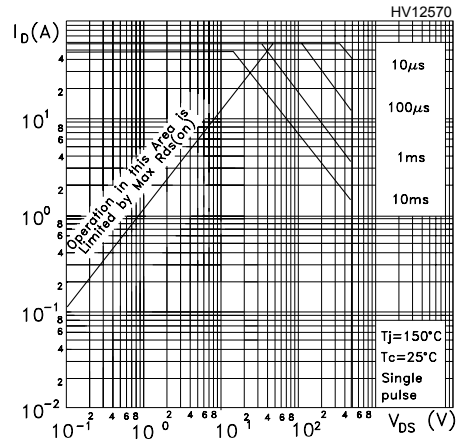


Figure 4. Normalized transient thermal impedance for TO-247

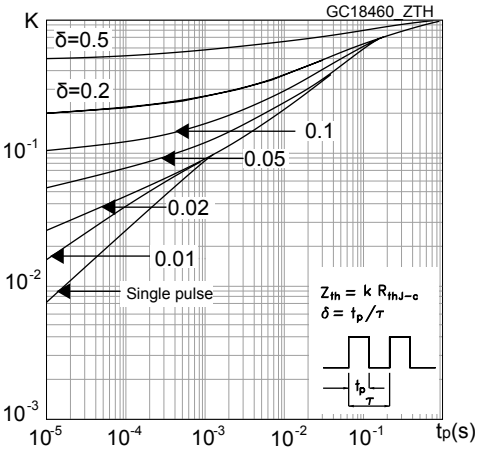


Figure 5. Typical output characterisics

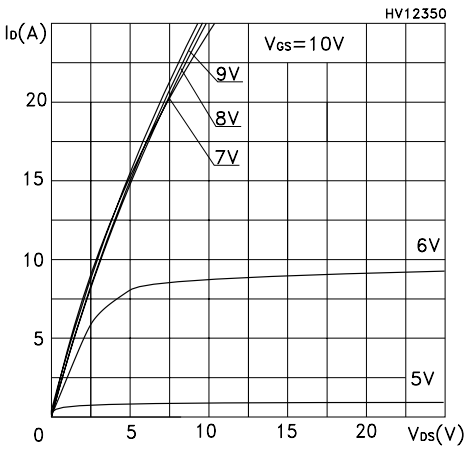


Figure 6. Typical transfer characteristics

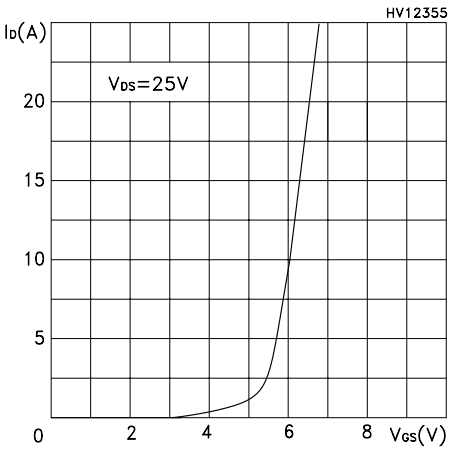


Figure 7. Typical gate charge characteristics

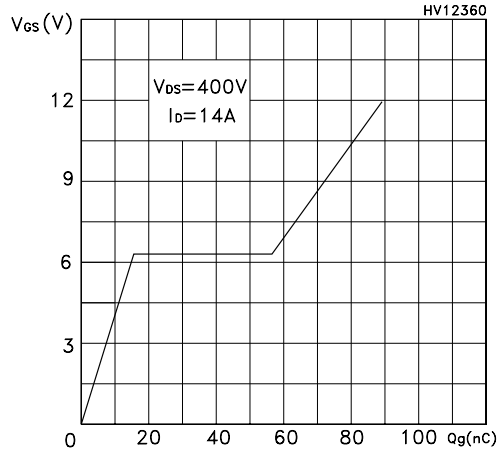


Figure 8. Typical drain-source on-resistance

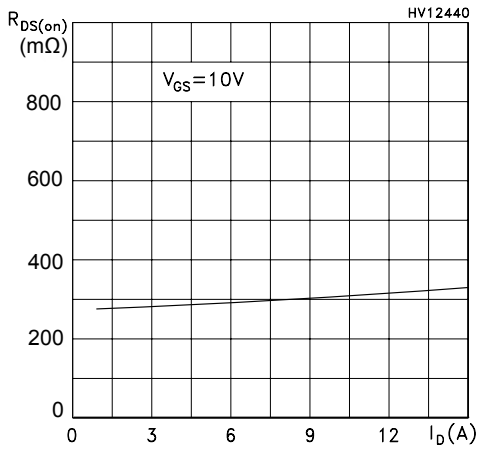


Figure 9. Typical capacitance characteristics

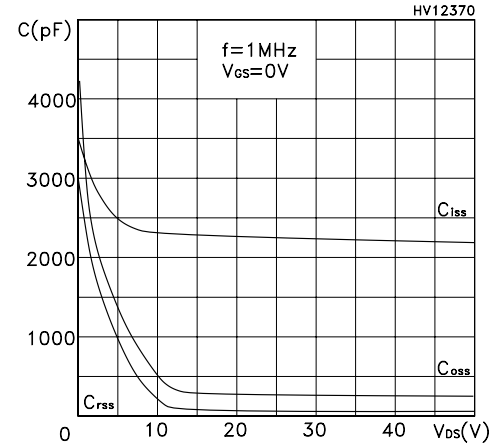


Figure 10. Normalized gate threshold vs temperature

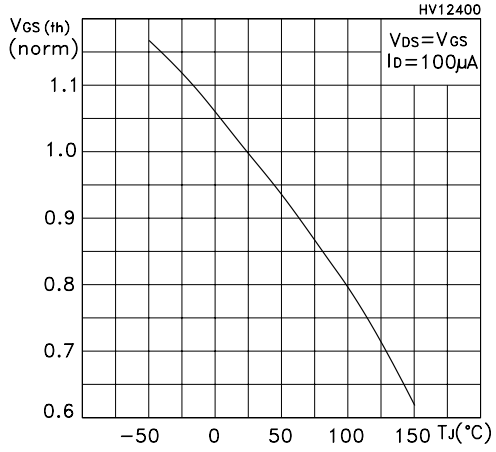


Figure 11. Normalized on-resistance vs temperature

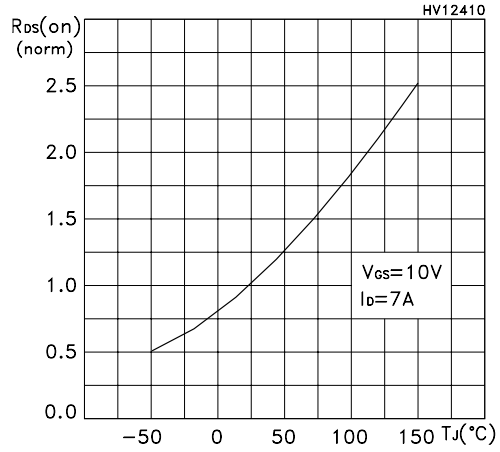


Figure 12. Normalized breakdown voltage vs temperature

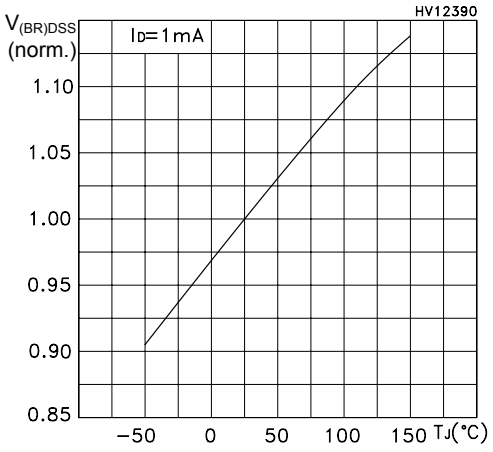


Figure 13. Maximum avalanche energy vs temperature

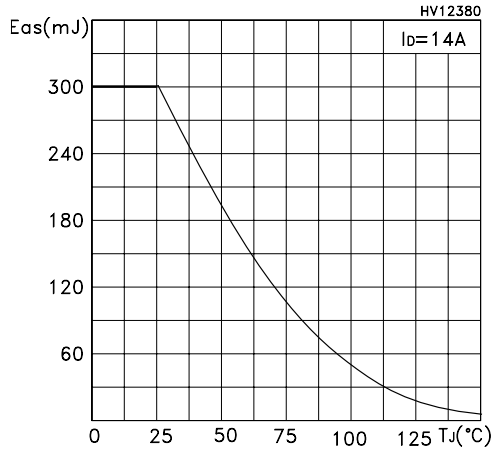
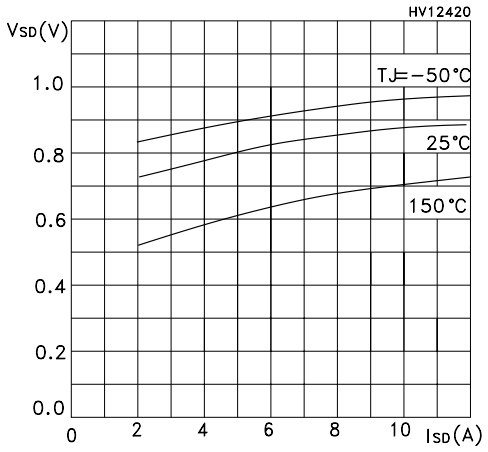


Figure 14. Typical reverse diode forward characteristics



3 Test circuits

Figure 15. Test circuit for resistive load switching times

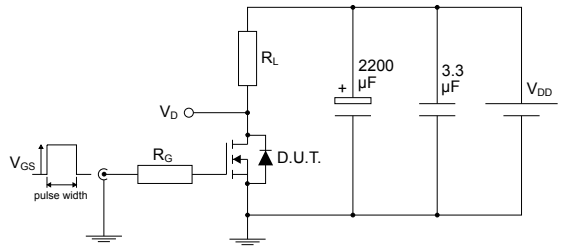


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Figure 16. Test circuit for gate charge behavior

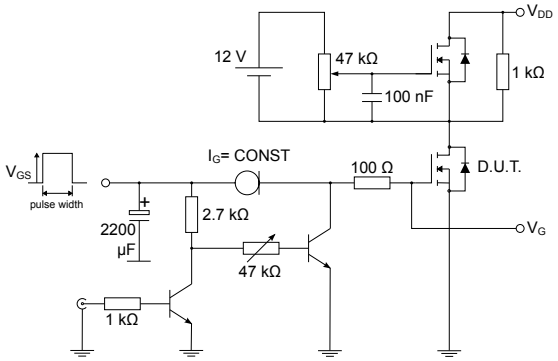

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Figure 17. Test circuit for inductive load switching and diode recovery times

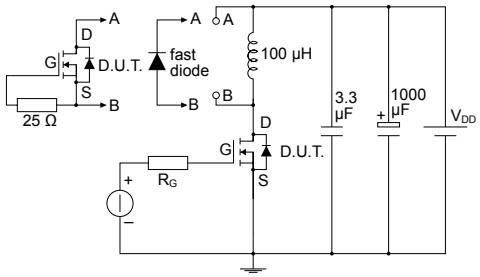

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Figure 18. Unclamped inductive load test circuit

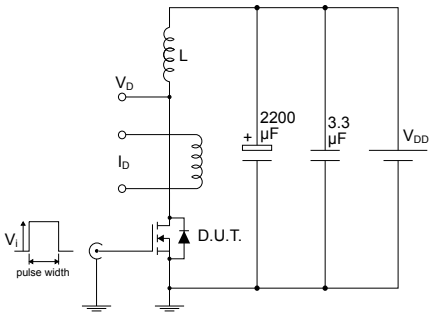

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Figure 19. Unclamped inductive waveform

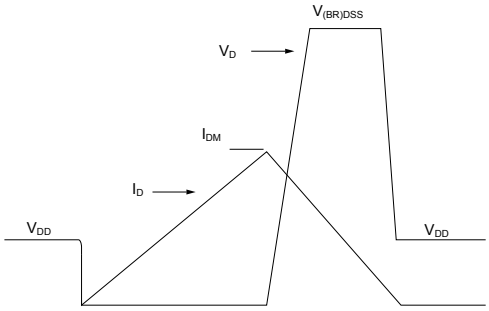

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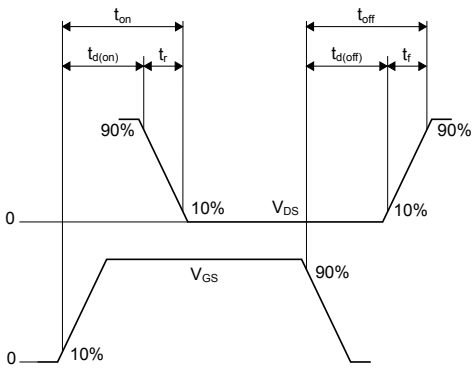
Figure 20. Switching time waveform



AM01473v1

4 Package information

To meet environmental requirements, ST offers these devices in different grades of ECOPACK packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions, and product status are available at: www.st.com. ECOPACK is an ST trademark.

4.1 TO-220 type A package information

Figure 21. TO-220 type A package outline

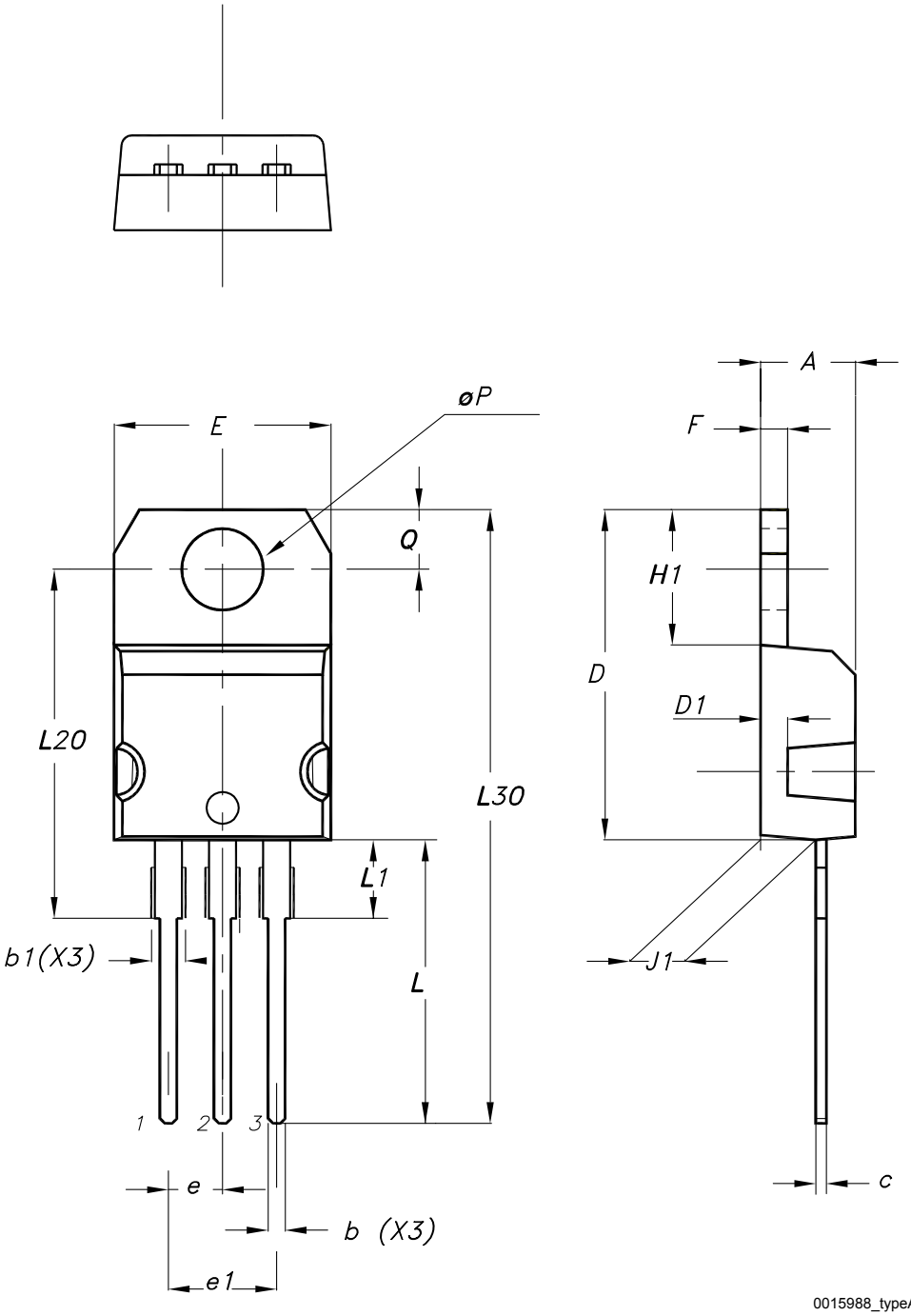
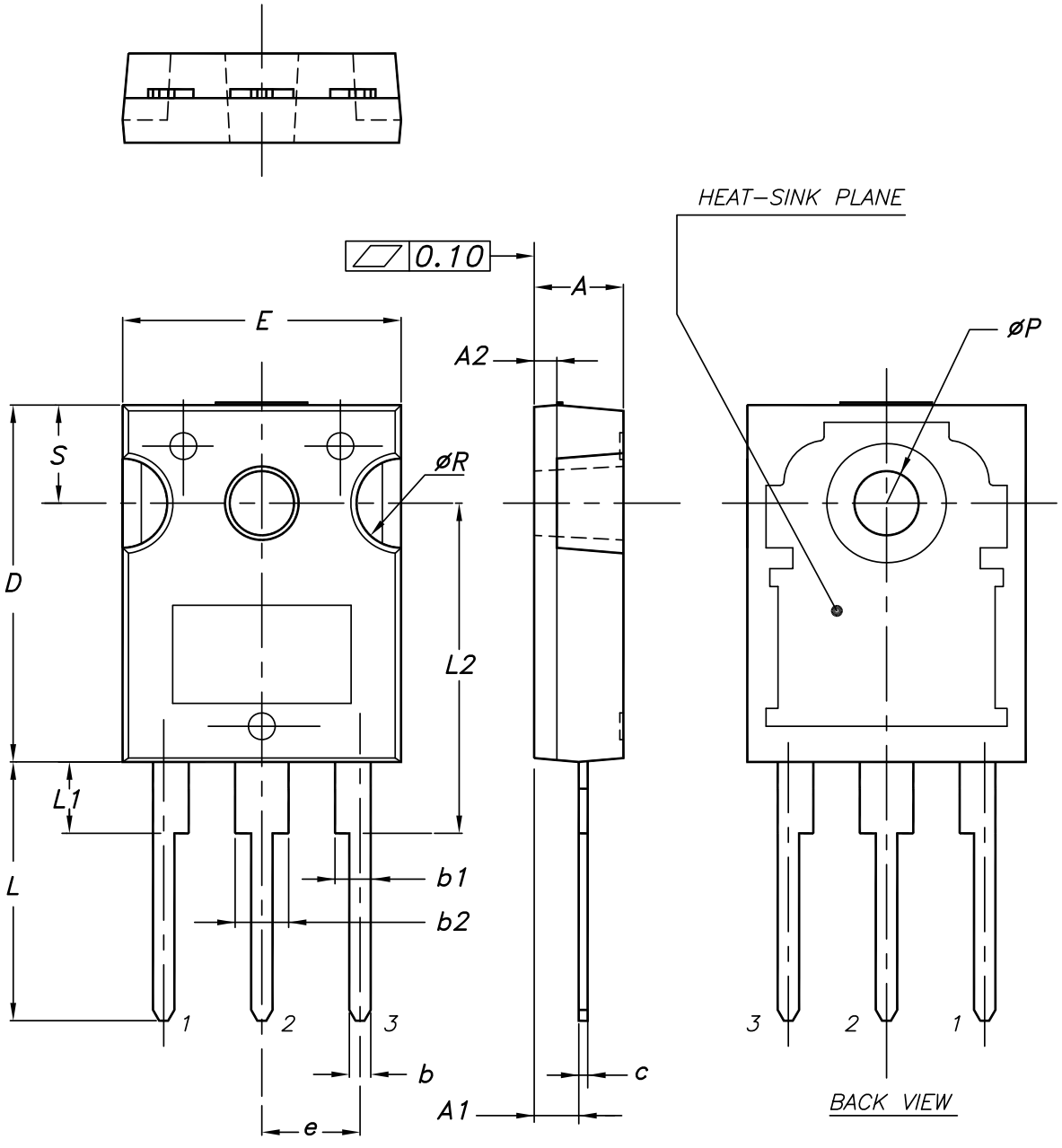


Table 8. **TO-220 type A package mechanical data**

Dim.	mm		
	Min.	Typ.	Max.
A	4.40		4.60
b	0.61		0.88
b1	1.14		1.55
c	0.48		0.70
D	15.25		15.75
D1		1.27	
E	10.00		10.40
e	2.40		2.70
e1	4.95		5.15
F	1.23		1.32
H1	6.20		6.60
J1	2.40		2.72
L	13.00		14.00
L1	3.50		3.93
L20		16.40	
L30		28.90	
øP	3.75		3.85
Q	2.65		2.95
Slug flatness		0.03	0.10

4.2 TO-247 package information

Figure 22. **TO-247 package outline**



0075325_11

Table 9. **TO-247 package mechanical data**

Dim.	mm		
	Min.	Typ.	Max.
A	4.85		5.15
A1	2.20		2.60
A2		1.27	
b	1.0		1.40
b1	2.0		2.40
b2	3.0		3.40
c	0.40		0.80
D	19.85		20.15
E	15.45		15.75
e	5.30	5.45	5.60
L	14.20		14.80
L1	3.70		4.30
L2		18.50	
ØP	3.55		3.65
ØR	4.50		5.50
S	5.30	5.50	5.70

Revision history

Table 10. **Document revision history**

Date	Version	Changes
21-Jun-2004	2	Complete version
20-Jul-2006	3	New template, no content change
05-Jan-2007	4	Modified unit on *On/off states*
09-Feb-2026	5	The part numbers STB15NK50Z, STB15NK50Z-1 and STP15NK50ZFP have been removed and the document has been updated accordingly. Updated Section 4: Package information. Minor text changes.

Contents

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