

8A, 100V, 0.400 Ohm, P-Channel Power MOSFET

This P-Channel enhancement mode silicon gate power field effect transistor is designed for applications such as switching regulators, switching convertors, motor drivers, relay drivers, and drivers for high power bipolar switching transistors requiring high speed and low gate drive power. These types can be operated directly from integrated circuits.

Formerly developmental type TA17511.

Ordering Information

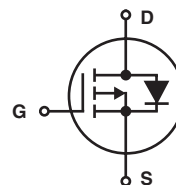
PART NUMBER	PACKAGE	BRAND
RFP8P10	TO-220AB	RFP8P10

NOTE: When ordering, include the entire part number.

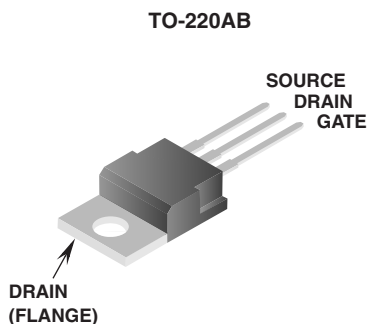
Features

- 8A, 100V
- $r_{DS(ON)} = 0.400\Omega$
- Related Literature
 - TB334 "Guidelines for Soldering Surface Mount Components to PC Boards"

Symbol



Packaging



RFP8P10

Absolute Maximum Ratings $T_C = 25^\circ\text{C}$, Unless Otherwise Specified

	RFP8P10	UNITS
Drain to Source Voltage (Note 1)	V_{DS}	-100 V
Drain to Gate Voltage ($R_{GS} = 20\text{k}\Omega$) (Note 1)	V_{DGR}	-100 V
Continuous Drain Current	I_D	8 A
Pulsed Drain Current (Note 3)	I_{DM}	20 A
Gate to Source Voltage	V_{GS}	± 20 V
Maximum Power Dissipation		75 W
Linear Derating Factor		0.6 W/ $^\circ\text{C}$
Operating and Storage Temperature	T_J, T_{STG}	-55 to 150 $^\circ\text{C}$
Maximum Temperature for Soldering		
Leads at 0.063in (1.6mm) from Case for 10s.	T_L	300 $^\circ\text{C}$
Package Body for 10s, See Techbrief 334	T_{pkg}	260 $^\circ\text{C}$

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTE:

1. $T_J = 25^\circ\text{C}$ to 125°C .

Electrical Specifications $T_C = 25^\circ\text{C}$, Unless Otherwise Specified

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Drain to Source Breakdown Voltage	BV_{DSS}	$I_D = -250\mu\text{A}$, $V_{GS} = 0$	-100			V
Gate Threshold Voltage	$V_{GS(TH)}$	$V_{GS} = V_{DS}$, $I_D = -250\mu\text{A}$	-2	-	-4	V
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS} = \text{Rated } BV_{DSS}$, $V_{GS} = 0\text{V}$	-	-	1	μA
		$V_{DS} = 0.8 \times \text{Rated } BV_{DSS}$, $V_{GS} = 0\text{V}$, $T_J = 125^\circ\text{C}$	-	-	25	μA
Gate to Source Leakage Current	I_{GSS}	$V_{GS} = \pm 20\text{V}$, $V_{DS} = 0$	-	-	± 100	nA
Drain to Source On Resistance (Note 2)	$r_{DS(ON)}$	$I_D = 8\text{A}$, $V_{GS} = -10\text{V}$ (Figures 6, 7)	-	-	0.400	Ω
Drain to Source On Voltage (Note 2)	$V_{DS(ON)}$	$I_D = 8\text{A}$, $V_{GS} = -10\text{V}$	-	-	3.2	V
Turn-On Delay Time	$t_{d(ON)}$	$I_D \approx 4\text{A}$, $V_{DD} = 50\text{V}$, $R_G = 50\Omega$, $V_{GS} = -10\text{V}$ $R_L = 12\Omega$, (Figure 10)	-	18	60	ns
Rise Time	t_r		-	70	150	ns
Turn-Off Delay Time	$t_{d(OFF)}$		-	166	275	ns
Fall Time	t_f		-	94	175	ns
Input Capacitance	C_{ISS}	$V_{GS} = 0\text{V}$, $V_{DS} = 25\text{V}$, $f = 1\text{MHz}$ (Figure 9)	-	-	1500	pF
Output Capacitance	C_{OSS}		-	-	700	pF
Reverse Transfer Capacitance	C_{RSS}		-	-	300	pF
Thermal Resistance, Junction to Case	$R_{\theta JC}$	RFP8P10	-	-	1.67	$^\circ\text{C/W}$

Source to Drain Diode Specifications

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Source to Drain Diode Voltage (Note 2)	V_{SD}	$I_{SD} = -4\text{A}$	-	-	-1.4	V
Diode Reverse Recovery Time	t_{rr}	$I_{SD} = -4\text{A}$, $dI_{SD}/dt = -100\text{A}/\mu\text{s}$	-	200	-	ns

NOTES:

2. Pulse Test: Pulse Width $\leq 300\mu\text{s}$, Duty Cycle $\leq 2\%$
3. Repetitive rating: pulse width is limited by maximum junction temperature.

Typical Performance Curves

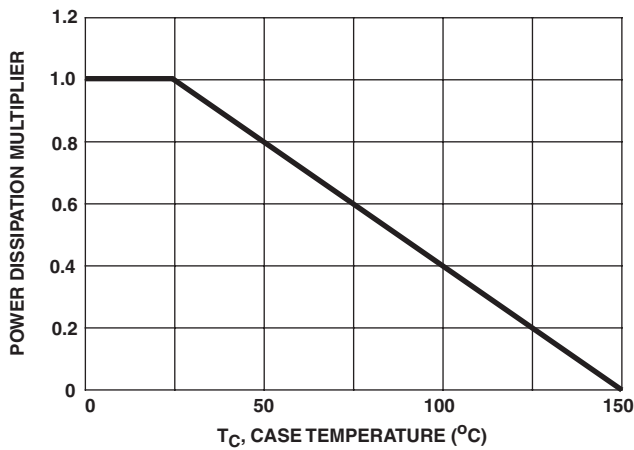


FIGURE 1. NORMALIZED POWER DISSIPATION vs CASE TEMPERATURE

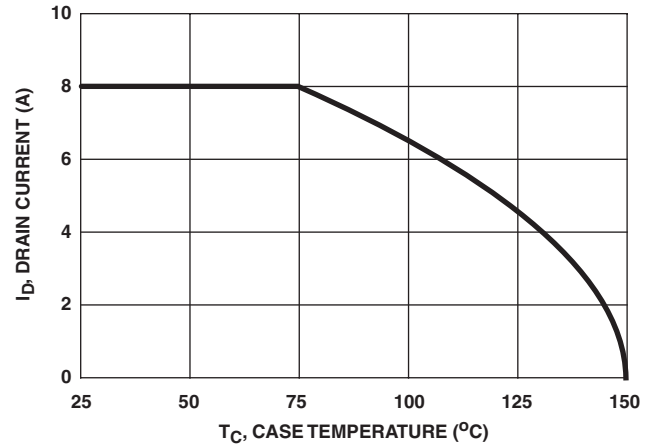


FIGURE 2. MAXIMUM CONTINUOUS DRAIN CURRENT vs CASE TEMPERATURE

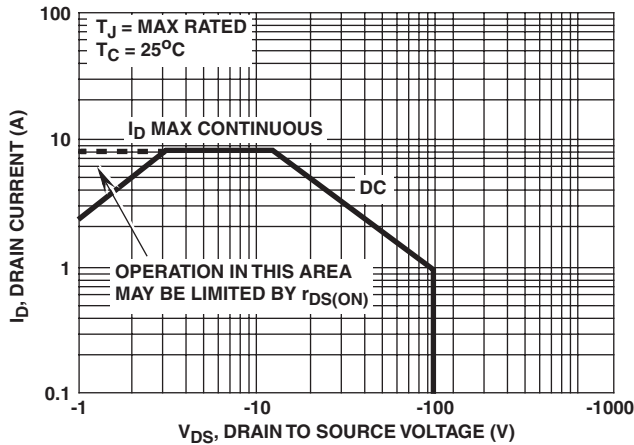


FIGURE 3. FORWARD BIAS SAFE OPERATING AREA

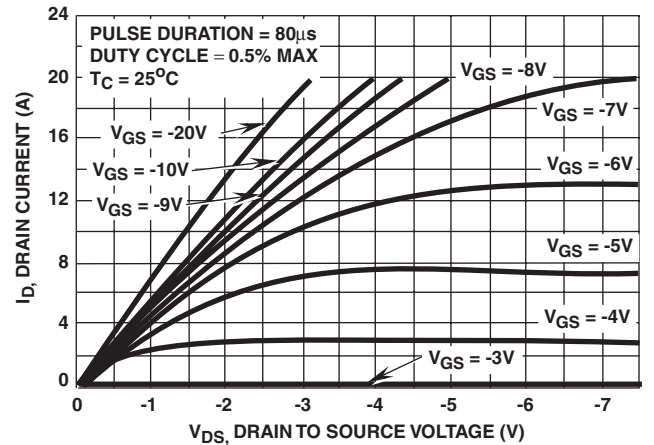


FIGURE 4. SATURATION CHARACTERISTICS

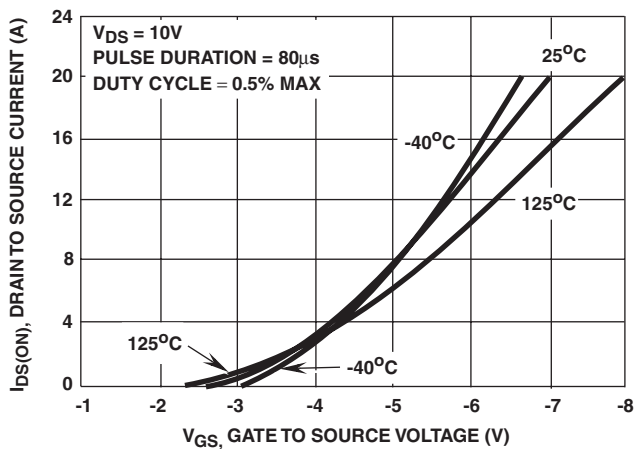


FIGURE 5. TRANSFER CHARACTERISTICS

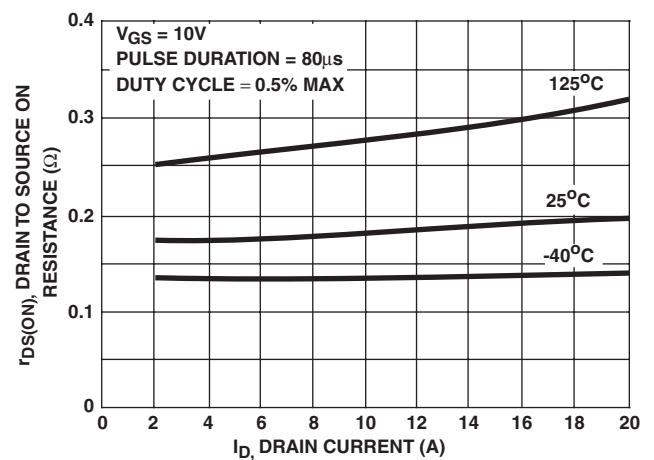


FIGURE 6. DRAIN TO SOURCE ON RESISTANCE vs DRAIN CURRENT

Typical Performance Curves (Continued)

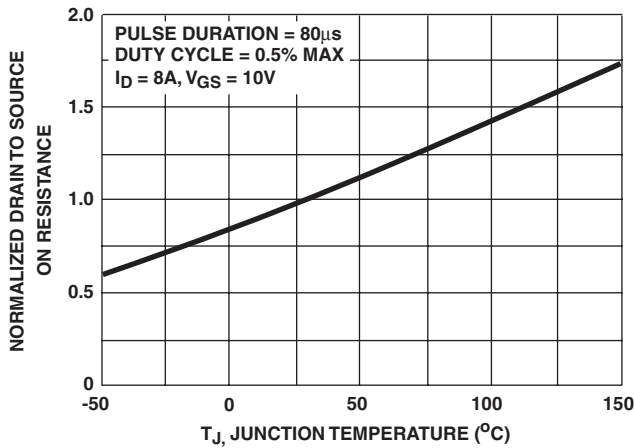


FIGURE 7. NORMALIZED DRAIN TO SOURCE ON RESISTANCE vs JUNCTION TEMPERATURE

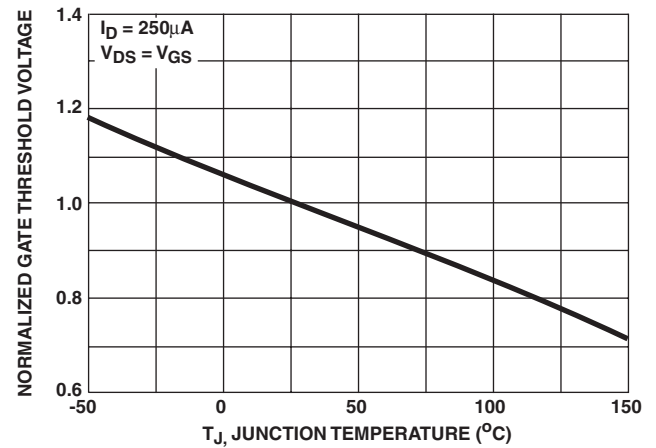


FIGURE 8. NORMALIZED GATE THRESHOLD VOLTAGE vs JUNCTION TEMPERATURE

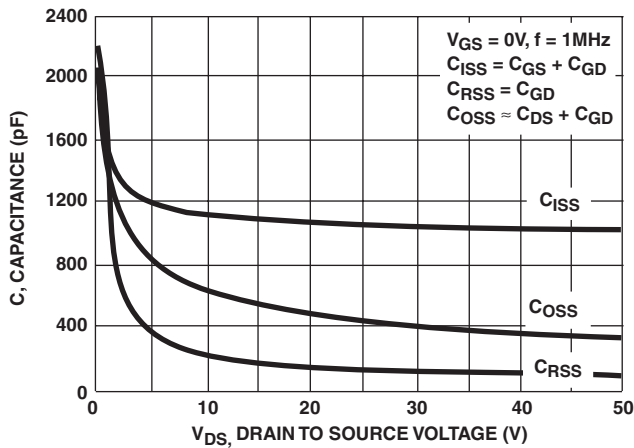
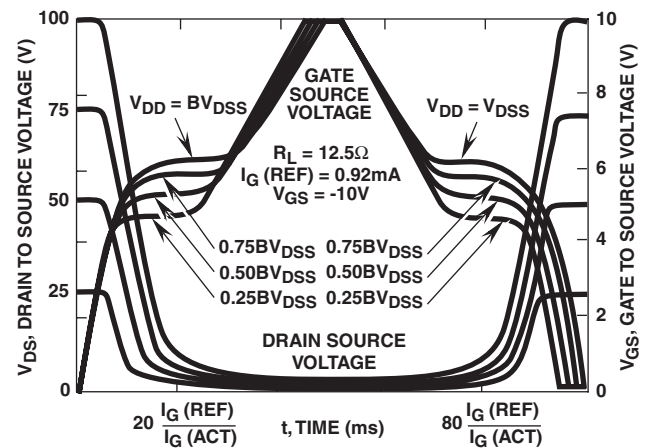


FIGURE 9. CAPACITANCE vs DRAIN TO SOURCE VOLTAGE



NOTE: Refer to Fairchild Applications Notes AN7254 and AN7260

FIGURE 10. NORMALIZED SWITCHING WAVEFORMS FOR CONSTANT GATE CURRENT

Test Circuits and Waveforms

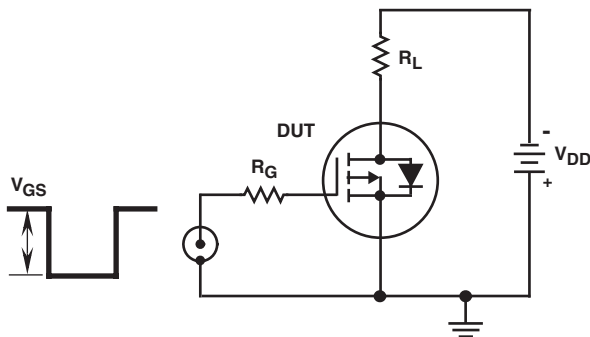


FIGURE 11. SWITCHING TIME TEST CIRCUIT

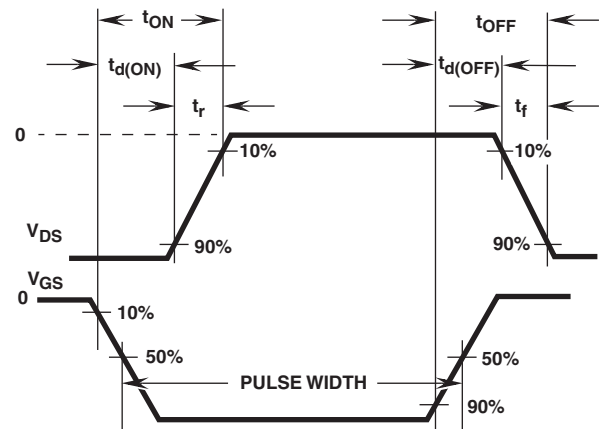


FIGURE 12. RESISTIVE SWITCHING WAVEFORMS

Test Circuits and Waveforms (Continued)

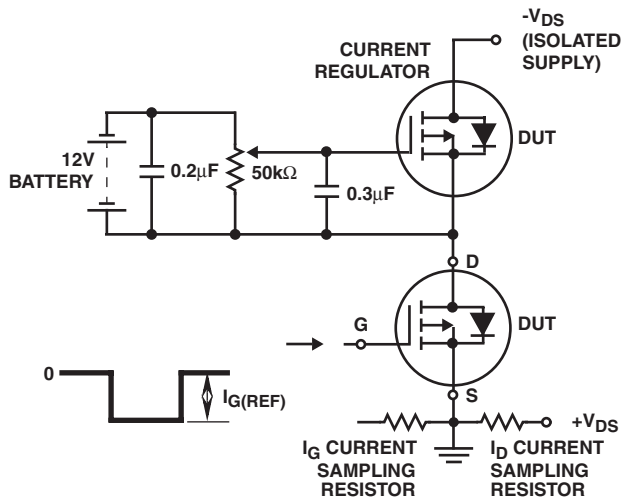


FIGURE 13. GATE CHARGE TEST CIRCUIT

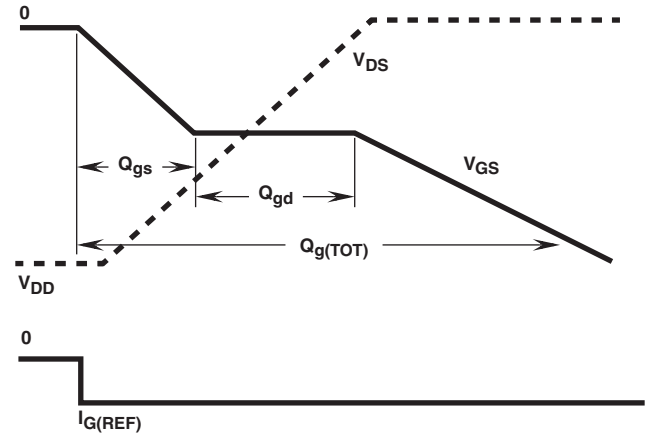


FIGURE 14. GATE CHARGE WAVEFORMS

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