

FDMC007N30D

MOSFET, Dual N-Channel, POWERTRENCH[®]

Q1: 30 V, 11.6 mΩ; Q2: 30 V, 6.4 mΩ

General Description

This device includes two specialized N-Channel MOSFETs in a dual Power33 (3mm × 3mm MLP) package. The switch node has been internally connected to enable easy placement and routing of synchronous buck converters. The control MOSFET (Q1) and synchronous MOSFET (Q2) have been designed to provide optimal power efficiency.

Features

Q1: N-Channel

- Max $r_{DS(on)}$ = 11.6 mΩ at $V_{GS} = 10$ V, $I_D = 10$ A
- Max $r_{DS(on)}$ = 13.3 mΩ at $V_{GS} = 4.5$ V, $I_D = 9$ A

Q2: N-Channel

- Max $r_{DS(on)}$ = 6.4 mΩ at $V_{GS} = 10$ V, $I_D = 16$ A
- Max $r_{DS(on)}$ = 7.0 mΩ at $V_{GS} = 4.5$ V, $I_D = 15$ A
- RoHS Compliant

Applications

- Mobile Computing
- Mobile Internet Devices
- General Purpose Point of Load

MOSFET MAXIMUM RATINGS ($T_C = 25^\circ\text{C}$ unless otherwise noted)

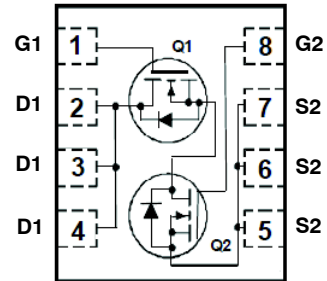
Symbol	Parameter	Q1	Q2	Unit
V_{DS}	Drain to Source Voltage	30	30	V
V_{GS}	Gate to Source Voltage (Note 4)	± 12	± 12	V
I_D	Drain Current: – Continuous, $T_C = 25^\circ\text{C}$ (Note 6) – Continuous, $T_C = 100^\circ\text{C}$ (Note 6) – Continuous, $T_A = 25^\circ\text{C}$ (Note 1a) – Pulsed (Note 5)	29 18 10 113 (Note 1a)	46 29 16 302 (Note 1b)	A
E_{AS}	Single Pulse Avalanche Energy (Note 3)	24	54	mJ
P_D	Power Dissipation for Single Operation: $T_A = 25^\circ\text{C}$ $T_A = 25^\circ\text{C}$	1.9 (Note 1a) 0.7 (Note 1c)	2.5 (Note 1b) 1.0 (Note 1d)	W
T_J, T_{STG}	Operating and Storage Junction Temperature Range	–55 to +150		$^\circ\text{C}$

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.



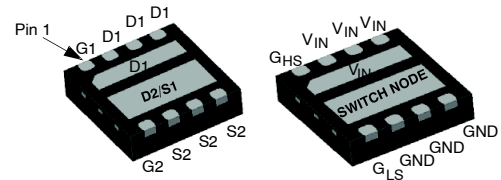
ON Semiconductor[®]

www.onsemi.com



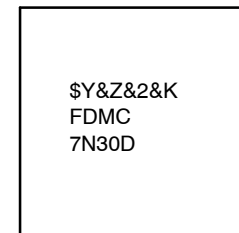
Dual N-Channel MOSFET

Bottom



WDFN8 3x3
CASE 511DE

MARKING DIAGRAM



\$Y = ON Semiconductor Logo
&Z = Assembly Plant Code
&2 = Data Code (Year & Week)
&K = Lot
FDMC7N30D = Specific Device Code

ORDERING INFORMATION

See detailed ordering and shipping information on page 2 of this data sheet.

FDMC007N30D

PACKAGE MARKING AND ORDERING INFORMATION

Device Marking	Device	Package	Quantity
FDMC7N30D	FDMC007N30D	WDFN-8 (Power 33)	3000/Tape&Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

THERMAL CHARACTERISTICS

Symbol	Parameter	Q1	Q2	Unit
$R_{\theta JC}$	Thermal Resistance, Junction to Case	8.2	6.1	°C/W
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient	65 (Note 1a)	50 (Note 1b)	
		180 (Note 1c)	125 (Note 1d)	

ELECTRICAL CHARACTERISTICS ($T_J = 25^\circ\text{C}$ unless otherwise noted)

Symbol	Parameter	Test Condition	Type	Min	Typ	Max	Unit
--------	-----------	----------------	------	-----	-----	-----	------

OFF CHARACTERISTICS

BV_{DSS}	Drain to Source Breakdown Voltage	$I_D = 250\ \mu\text{A}$, $V_{GS} = 0\ \text{V}$ $I_D = 250\ \mu\text{A}$, $V_{GS} = 0\ \text{V}$	Q1 Q2	30 30			V
$\Delta BV_{DSS} / \Delta T_J$	Breakdown Voltage Temperature Coefficient	$I_D = 250\ \mu\text{A}$, referenced to 25°C $I_D = 250\ \mu\text{A}$, referenced to 25°C	Q1 Q2		15 16		mV/°C
I_{DSS}	Zero Gate Voltage Drain Current	$V_{DS} = 24\ \text{V}$, $V_{GS} = 0\ \text{V}$	Q1 Q2			1 1	μA
I_{GSS}	Gate to Source Leakage Current, Forward	$V_{GS} = \pm 12\ \text{V}$, $V_{DS} = 0\ \text{V}$	Q1 Q2			± 100 ± 100	nA

ON CHARACTERISTICS

$V_{GS(th)}$	Gate to Source Threshold Voltage	$V_{GS} = V_{DS}$, $I_D = 250\ \mu\text{A}$ $V_{GS} = V_{DS}$, $I_D = 250\ \mu\text{A}$	Q1 Q2	1.0 1.0	1.3 1.8	3.0 3.0	V
$\Delta V_{GS(th)} / \Delta T_J$	Gate to Source Threshold Voltage Temperature Coefficient	$I_D = 250\ \mu\text{A}$, referenced to 25°C $I_D = 250\ \mu\text{A}$, referenced to 25°C	Q1 Q2		-4 -4		mV/°C
$r_{DS(on)}$	Static Drain to Source On Resistance	$V_{GS} = 10\ \text{V}$, $I_D = 10\ \text{A}$ $V_{GS} = 4.5\ \text{V}$, $I_D = 9\ \text{A}$ $V_{GS} = 10\ \text{V}$, $I_D = 10\ \text{A}$, $T_J = 125^\circ\text{C}$	Q1		7.7 8.9 10.8	11.6 13.3 16.3	m Ω
$r_{DS(on)}$	Static Drain to Source On Resistance	$V_{GS} = 10\ \text{V}$, $I_D = 16\ \text{A}$ $V_{GS} = 4.5\ \text{V}$, $I_D = 15\ \text{A}$ $V_{GS} = 10\ \text{V}$, $I_D = 16\ \text{A}$, $T_J = 125^\circ\text{C}$	Q2		4.4 5.4 6.2	6.4 7.0 9.0	m Ω
g_{FS}	Forward Transconductance	$V_{DD} = 5\ \text{V}$, $I_D = 10\ \text{A}$ $V_{DD} = 5\ \text{V}$, $I_D = 16\ \text{A}$	Q1 Q2		46 70		S

DYNAMIC CHARACTERISTICS

C_{iss}	Input Capacitance	$V_{DS} = 15\ \text{V}$, $V_{GS} = 0\ \text{V}$, $f = 1\ \text{MHz}$	Q1 Q2		792 1685	1110 2360	pF
C_{oss}	Output Capacitance		Q1 Q2		230 467	325 655	pF
C_{rss}	Reverse Transfer Capacitance		Q1 Q2		20 36	30 50	pF
R_g	Gate Resistance		Q1 Q2	0.1 0.1	2.0 1.2	4.0 2.4	Ω

FDMC007N30D

ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise noted) (continued)

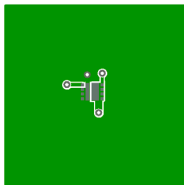
Symbol	Parameter	Test Condition	Type	Min	Typ	Max	Unit
SWITCHING CHARACTERISTICS							
t _{d(on)}	Turn-On Delay Time	Q1 V _{DD} = 15 V, I _D = 10 A, V _{GS} = 10 V, R _{GEN} = 6 Ω	Q1		7	14	ns
t _r	Rise Time		Q2		10	20	ns
t _{d(off)}	Turn-Off Delay Time	Q2 V _{DD} = 15 V, I _D = 16 A, V _{GS} = 10 V, R _{GEN} = 6 Ω	Q1		2	10	ns
t _f	Fall Time		Q2		3	10	ns
Q _{g(TOT)}	Total Gate Charge	V _{GS} = 0 V to 10 V Q1 V _{DD} = 15 V, V _{GS} = 0 V to 4.5 V I _D = 10 A Q2 V _{DD} = 15 V, I _D = 16 A	Q1		12	17	nC
			Q2		24	34	nC
Q _{gs}	Gate to Source Charge		Q1		5.5	7.7	nC
			Q2		11	16	nC
Q _{gd}	Gate to Drain "Miller" Charge		Q1		1.7		nC
			Q2		4.4		nC
			Q1		1.3		nC
			Q2		2.7		nC

DRAIN-SOURCE DIODE CHARACTERISTICS

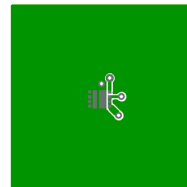
V _{SD}	Source-Drain Diode Forward Voltage	V _{GS} = 0 V, I _S = 10 A (Note 2) V _{GS} = 0 V, I _S = 1.5 A (Note 2) V _{GS} = 0 V, I _S = 16 A (Note 2) V _{GS} = 0 V, I _S = 2 A (Note 2)	Q1 Q1 Q2 Q2		0.85 0.75 0.83 0.73	1.2 1.2 1.2 1.2	V
t _{rr}	Reverse Recovery Time	Q1 I _F = 10 A, di/dt = 100 A/μs	Q1 Q2		17 27	31 42	ns
Q _{rr}	Reverse Recovery Charge	Q2 I _F = 16 A, di/dt = 100 A/μs	Q1 Q2		5 10	10 20	nC

NOTES:

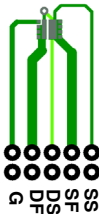
1. R_{θJA} is determined with the device mounted on a 1 in² pad 2 oz copper pad on a 1.5 × 1.5 in. board of FR-4 material. R_{θCA} is determined by the user's board design.



a. 65 °C/W when mounted on a 1 in² pad of 2 oz copper.



b. 50 °C/W when mounted on a 1 in² pad of 2 oz copper.



c. 180 °C/W when mounted on a minimum pad of 2 oz copper.



d. 125 °C/W when mounted on a minimum pad of 2 oz copper.

2. Pulse Test: Pulse Width < 300 μs, Duty cycle < 2.0%.
3. Q1: E_{AS} of 24 mJ is based on starting T_J = 25°C, L = 3 mH, I_{AS} = 4 A, V_{DD} = 30 V, V_{GS} = 10 V. 100% tested at L = 0.1 mH, I_{AS} = 13 A. Q2: E_{AS} of 54 mJ is based on starting T_J = 25°C, L = 3 mH, I_{AS} = 6 A, V_{DD} = 30 V, V_{GS} = 10 V. 100% tested at L = 0.1 mH, I_{AS} = 22 A.
4. As an N-ch device, the negative V_{gs} rating is for low duty cycle pulse occurrence only. No continuous rating is implied.
5. Pulsed I_d please refer to Figure 11 and Figure. 24 SOA graph for more details.
6. Computed continuous current limited to Max Junction Temperature only, actual continuous current will be limited by thermal & electro-mechanical application board design.

TYPICAL CHARACTERISTICS (Q1 N-CHANNEL)

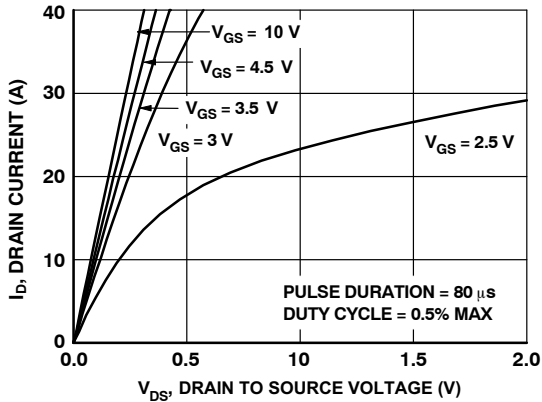
(T_J = 25°C unless otherwise noted)

Figure 1. On Region Characteristics

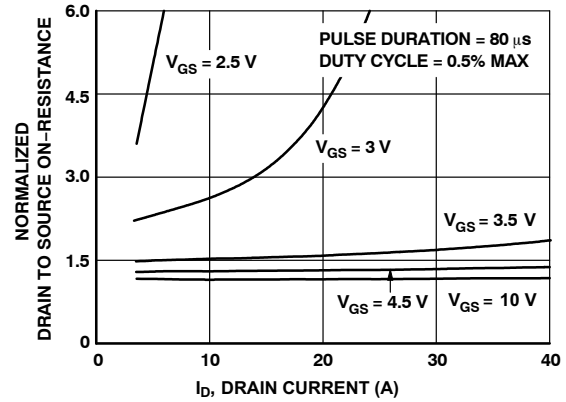


Figure 2. Normalized On-Resistance vs. Drain Current and Gate Voltage

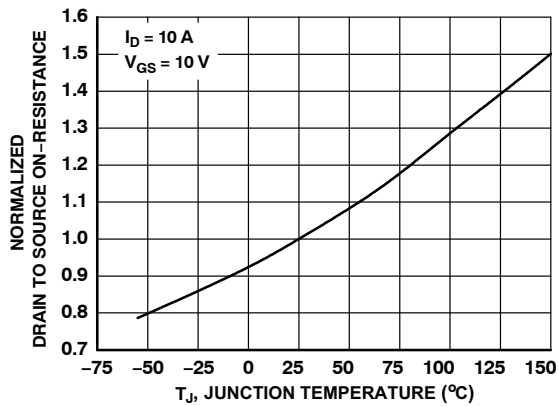


Figure 3. Normalized On Resistance vs. Junction Temperature

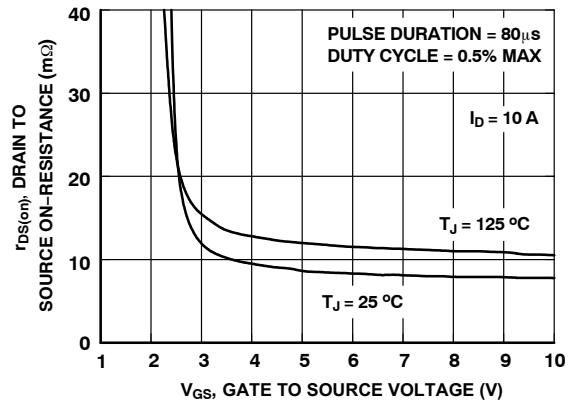


Figure 4. On-Resistance vs. Gate to Source Voltage

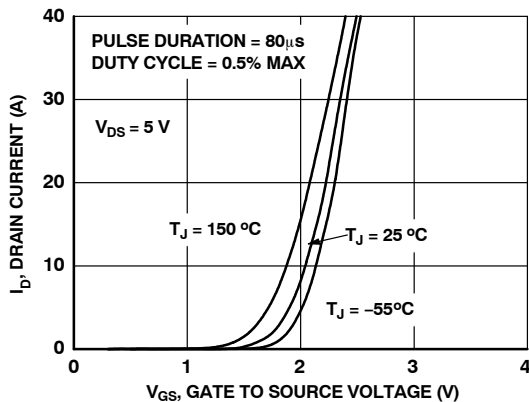


Figure 5. Transfer Characteristics

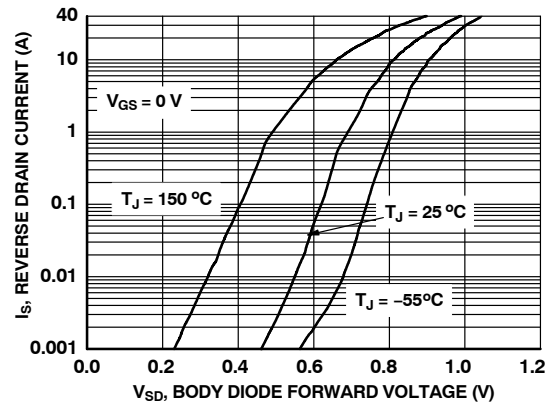


Figure 6. Source to Drain Diode Forward Voltage vs. Source Current

TYPICAL CHARACTERISTICS (Q1 N-CHANNEL) (continued)

($T_J = 25^\circ\text{C}$ unless otherwise noted)

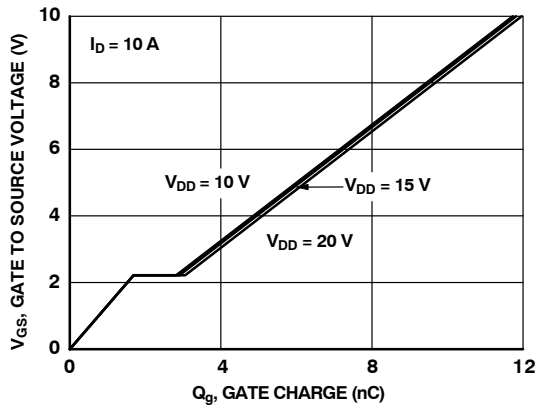


Figure 7. Gate Charge Characteristics

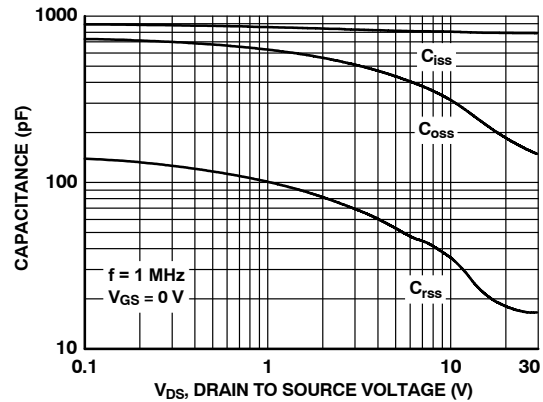


Figure 8. Capacitance vs. Drain to Source Voltage

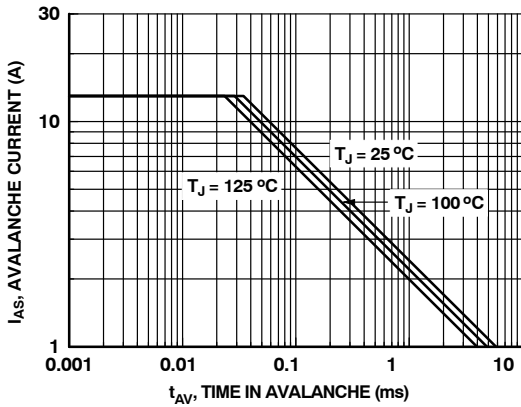


Figure 9. Unclamped Inductive Switching Capability

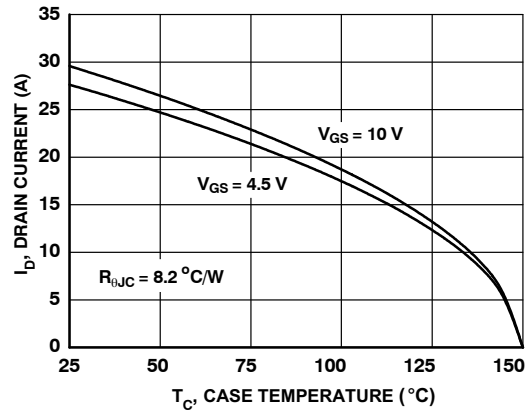


Figure 10. Maximum Continuous Drain Current vs. Case Temperature

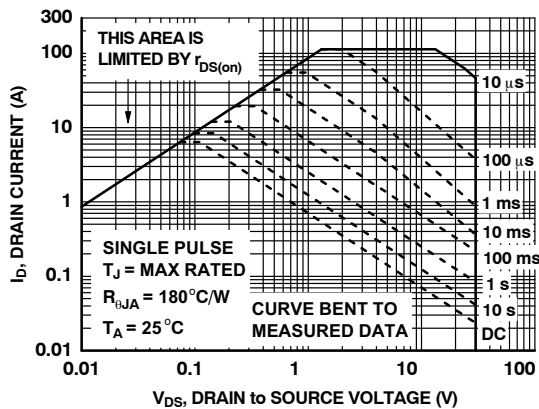


Figure 11. Forward Bias Safe Operating Area

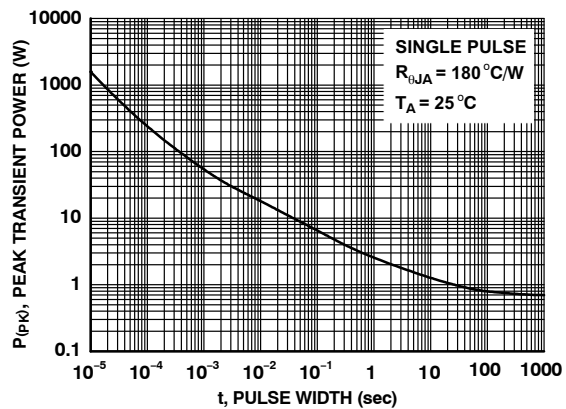


Figure 12. Single Pulse Maximum Power Dissipation

TYPICAL CHARACTERISTICS (Q1 N-CHANNEL) (continued)

($T_J = 25^\circ\text{C}$ unless otherwise noted)

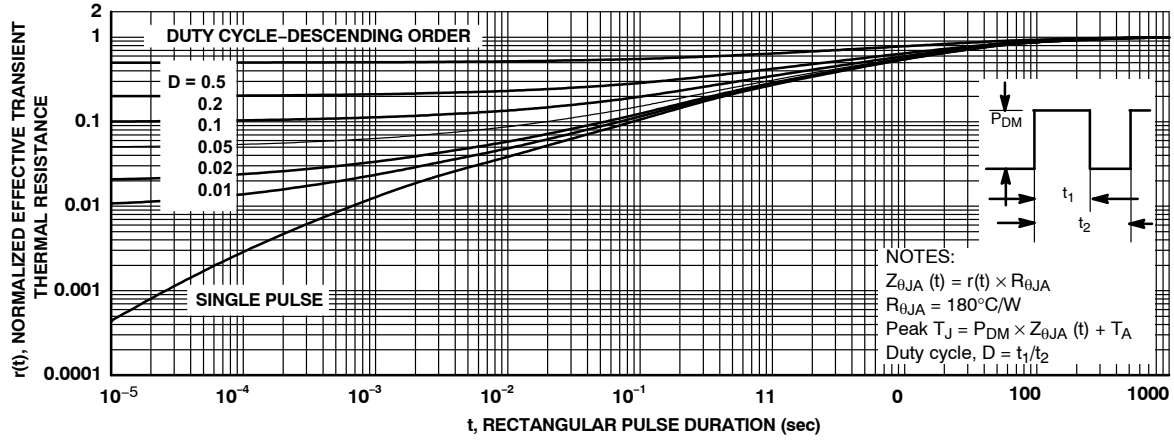


Figure 13. Junction-to-Ambient Transient Thermal Response Curve

TYPICAL CHARACTERISTICS (Q2 N-CHANNEL)

($T_J = 25^\circ\text{C}$ unless otherwise noted)

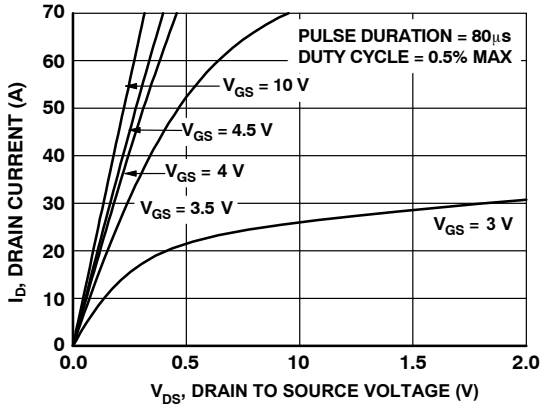


Figure 14. On Region Characteristics

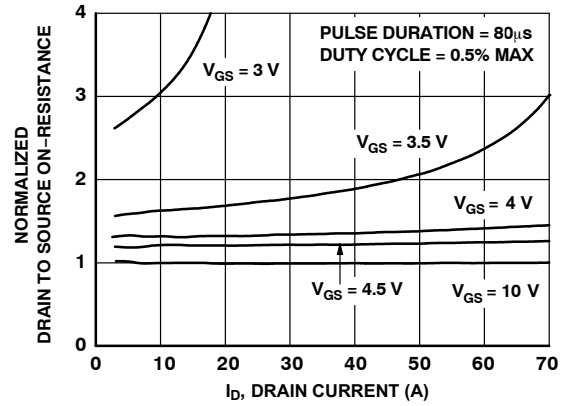


Figure 15. Normalized On-Resistance vs. Drain Current and Gate Voltage

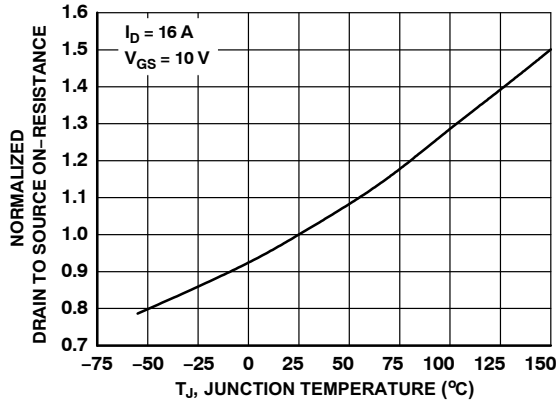


Figure 16. Normalized On Resistance vs. Junction Temperature

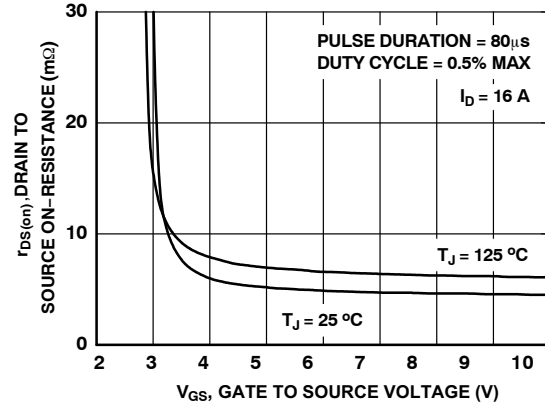


Figure 17. On-Resistance vs. Gate to Source Voltage

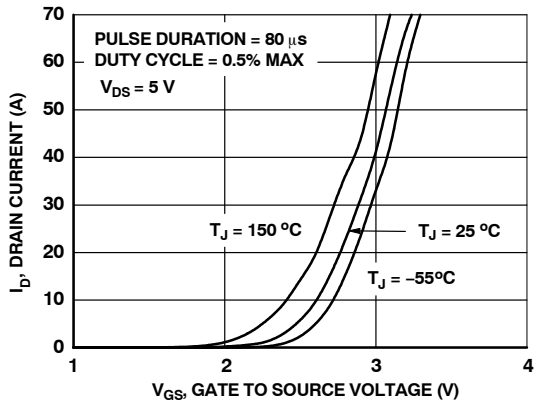


Figure 18. Transfer Characteristics

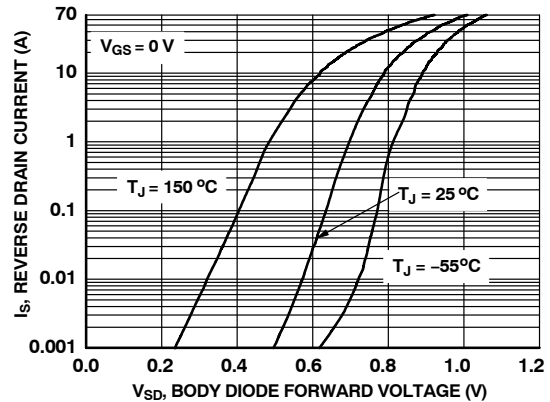


Figure 19. Source to Drain Diode Forward Voltage vs. Source Current

TYPICAL CHARACTERISTICS (Q2 N-CHANNEL) (continued)

($T_J = 25^\circ\text{C}$ unless otherwise noted)

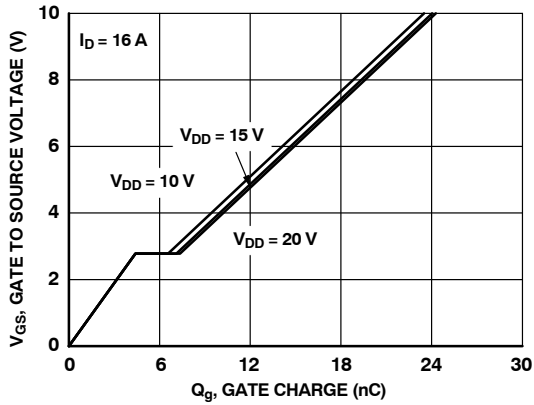


Figure 20. Gate Charge Characteristics

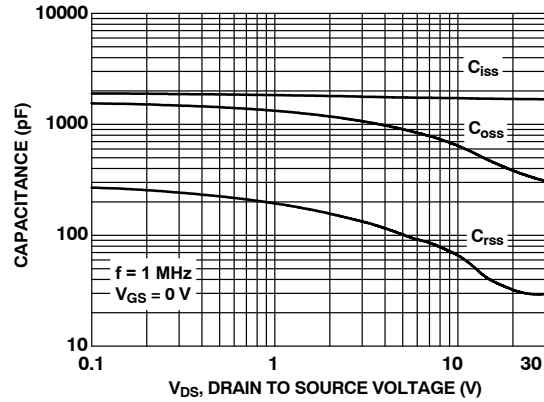


Figure 21. Capacitance vs. Drain to Source Voltage

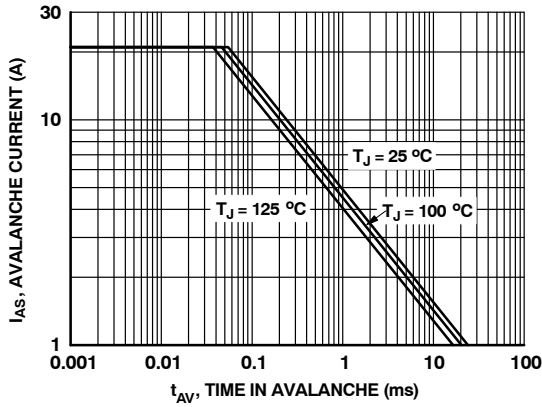


Figure 22. Unclamped Inductive Switching Capability

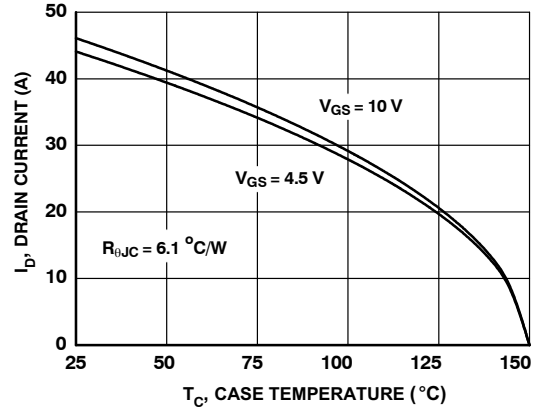


Figure 23. Maximum Continuous Drain Current vs. Case Temperature

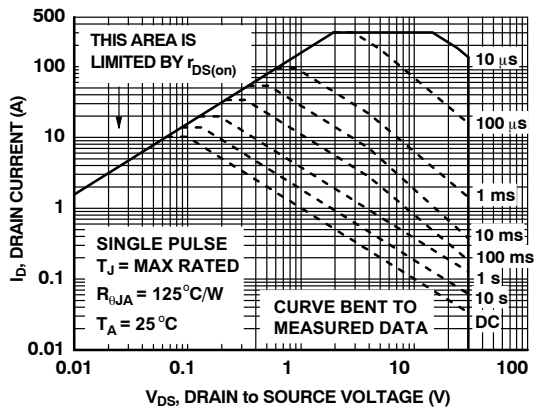


Figure 24. Forward Bias Safe Operating Area

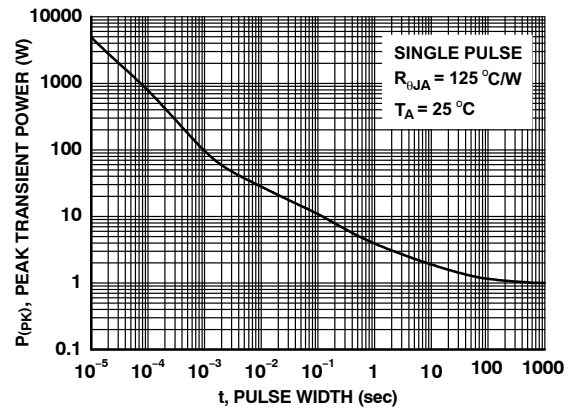


Figure 25. Single Pulse Maximum Power Dissipation

TYPICAL CHARACTERISTICS (Q2 N-CHANNEL) (continued)

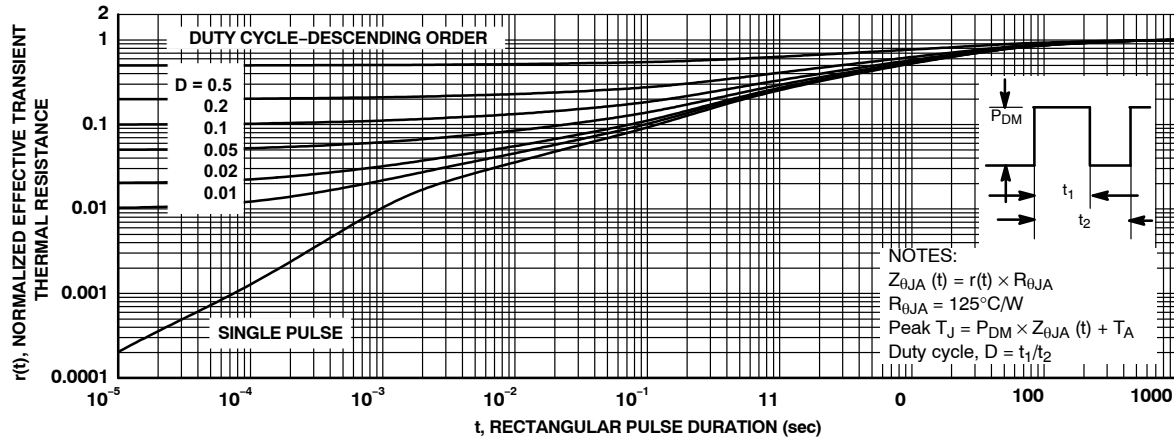
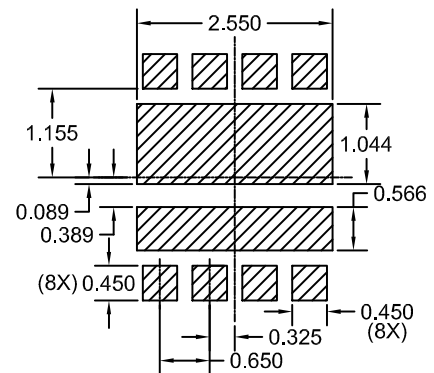
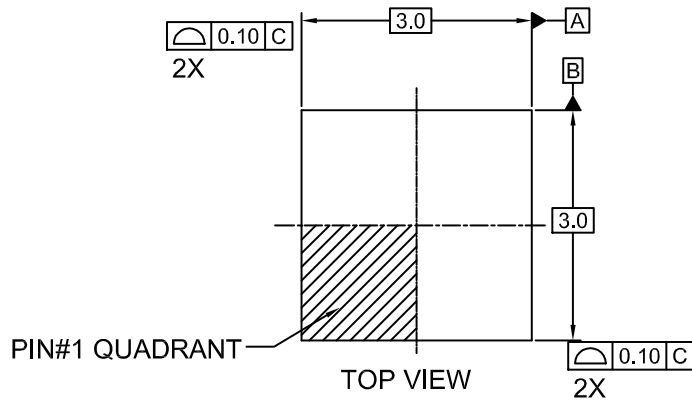
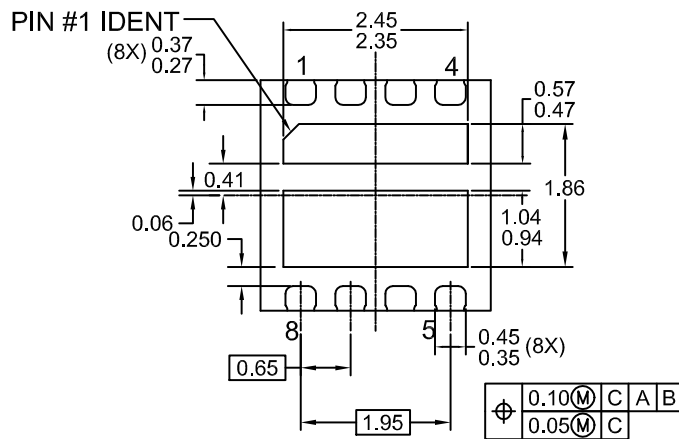
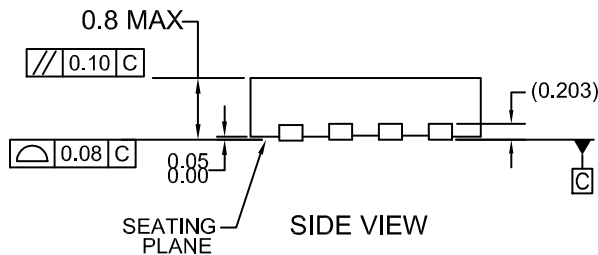
(T_J = 25°C unless otherwise noted)

Figure 26. Junction-to-Ambient Transient Thermal Response Curve

DATE 31 AUG 2016



RECOMMENDED LAND PATTERN



BOTTOM VIEW

NOTES:

- A. DOES NOT CONFORM TO JEDEC
REGISTRATION MO-229
- B. DIMENSIONS ARE IN MILLIMETERS.
- C. DIMENSIONS AND TOLERANCES PER
ASME Y14.5M, 1994

DOCUMENT NUMBER:	98AON13621G	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped "CONTROLLED COPY" in red.
DESCRIPTION:	WDFN8 3X3, 0.65P	PAGE 1 OF 1

ON Semiconductor and  are trademarks of Semiconductor Components Industries, LLC dba ON Semiconductor or its subsidiaries in the United States and/or other countries. ON Semiconductor reserves the right to make changes without further notice to any products herein. ON Semiconductor makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does ON Semiconductor assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. ON Semiconductor does not convey any license under its patent rights nor the rights of others.

onsemi, **Onsemi**, and other names, marks, and brands are registered and/or common law trademarks of Semiconductor Components Industries, LLC dba "**onsemi**" or its affiliates and/or subsidiaries in the United States and/or other countries. **onsemi** owns the rights to a number of patents, trademarks, copyrights, trade secrets, and other intellectual property. A listing of **onsemi**'s product/patent coverage may be accessed at www.onsemi.com/site/pdf/Patent-Marking.pdf. **onsemi** reserves the right to make changes at any time to any products or information herein, without notice. The information herein is provided "as-is" and **onsemi** makes no warranty, representation or guarantee regarding the accuracy of the information, product features, availability, functionality, or suitability of its products for any particular purpose, nor does **onsemi** assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. Buyer is responsible for its products and applications using **onsemi** products, including compliance with all laws, regulations and safety requirements or standards, regardless of any support or applications information provided by **onsemi**. "Typical" parameters which may be provided in **onsemi** data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals" must be validated for each customer application by customer's technical experts. **onsemi** does not convey any license under any of its intellectual property rights nor the rights of others. **onsemi** products are not designed, intended, or authorized for use as a critical component in life support systems or any FDA Class 3 medical devices or medical devices with a same or similar classification in a foreign jurisdiction or any devices intended for implantation in the human body. Should Buyer purchase or use **onsemi** products for any such unintended or unauthorized application, Buyer shall indemnify and hold **onsemi** and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that **onsemi** was negligent regarding the design or manufacture of the part. **onsemi** is an Equal Opportunity/Affirmative Action Employer. This literature is subject to all applicable copyright laws and is not for resale in any manner.

PUBLICATION ORDERING INFORMATION

LITERATURE FULFILLMENT:

Email Requests to: orderlit@onsemi.com

onsemi Website: www.onsemi.com

TECHNICAL SUPPORT

North American Technical Support:

Voice Mail: 1 800-282-9855 Toll Free USA/Canada

Phone: 011 421 33 790 2910

Europe, Middle East and Africa Technical Support:

Phone: 00421 33 790 2910

For additional information, please contact your local Sales Representative