

Automotive N-Channel 20 V (D-S) 175 °C MOSFET

PRODUCT SUMMARY

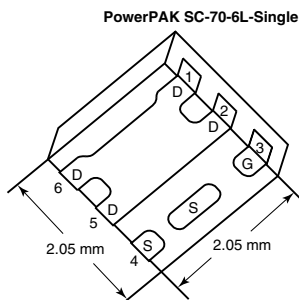
V _{DS} (V)	20
R _{DS(on)} (Ω) at V _{GS} = 4.5 V	0.028
R _{DS(on)} (Ω) at V _{GS} = 2.5 V	0.034
R _{DS(on)} (Ω) at V _{GS} = 1.8 V	0.038
I _D (A)	7.8
Configuration	Single

FEATURES

- Halogen-free According to IEC 61249-2-21 Definition
- TrenchFET® Power MOSFET
- AEC-Q101 Qualified ^d
- 100 % R_g and UIS Tested
- Compliant to RoHS Directive 2002/95/EC

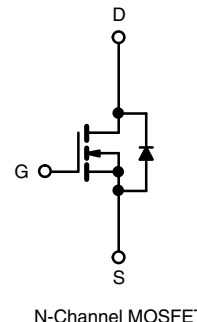
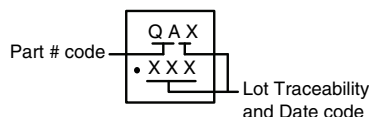


RoHS
COMPLIANT
HALOGEN
FREE



Ordering Information: SQA410EJ-T1-GE3 (Lead (Pb)-free and Halogen-free)

Marking Code



ORDERING INFORMATION

Package	PowerPAK SC-70
Lead (Pb)-free and Halogen-free	SQA410EJ-T1-GE3

ABSOLUTE MAXIMUM RATINGS (T_C = 25 °C, unless otherwise noted)

PARAMETER	SYMBOL	LIMIT	UNIT
Drain-Source Voltage	V _{DS}	20	V
Gate-Source Voltage	V _{GS}	± 8	V
Continuous Drain Current ^a	I _D	T _C = 25 °C	7.8
		T _C = 125 °C	7.8
Continuous Source Current (Diode Conduction) ^a	I _S	7.8	A
Pulsed Drain Current ^a	I _{DM}	24	A
Single Pulse Avalanche Current	I _{AS}	10	A
Single Pulse Avalanche Energy	E _{AS}	5	mJ
Maximum Power Dissipation ^b	P _D	T _C = 25 °C	13.6
		T _C = 125 °C	4.5
Operating Junction and Storage Temperature Range	T _J , T _{stg}	- 55 to + 175	°C
Soldering Recommendations (Peak Temperature) ^{e, f}		260	°C

THERMAL RESISTANCE RATINGS

PARAMETER	SYMBOL	LIMIT	UNIT
Junction-to-Ambient	R _{thJA}	90	°C/W
Junction-to-Case (Drain)	R _{thJC}	11	°C/W

Notes

- Package limited.
- Pulse test; pulse width ≤ 300 μs, duty cycle ≤ 2 %.
- When mounted on 1" square PCB (FR-4 material).
- Parametric verification ongoing.
- See solder profile (www.vishay.com/doc?73257). The PowerPAK SC-70 is a leadless package. The end of the lead terminal is exposed copper (not plated) as a result of the singulation process in manufacturing. A solder fillet at the exposed copper tip cannot be guaranteed and is not required to ensure adequate bottom side solder interconnection.
- Rework conditions: manual soldering with a soldering iron is not recommended for leadless components.

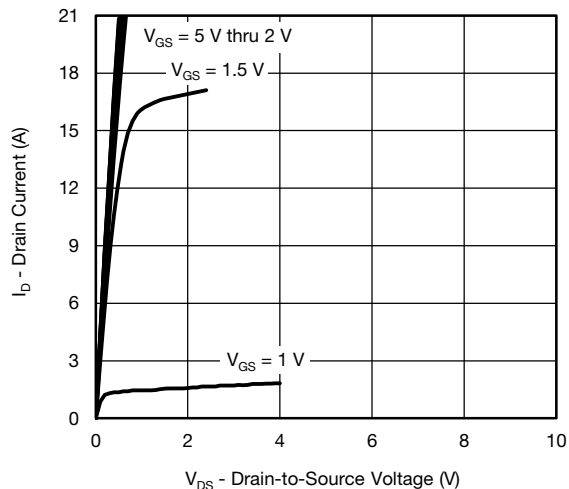
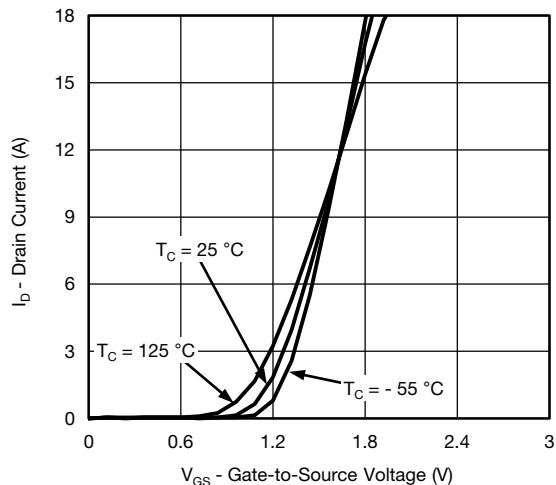
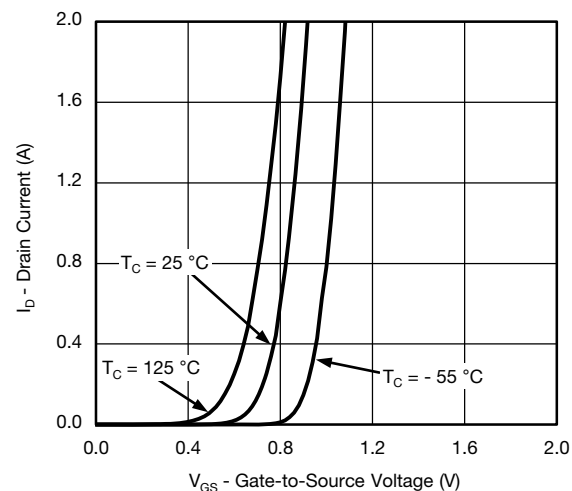
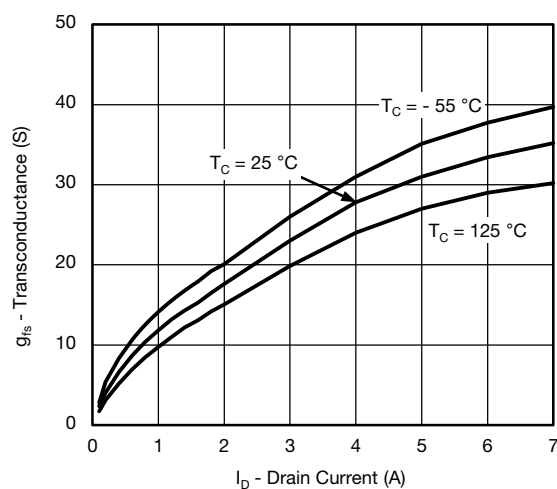
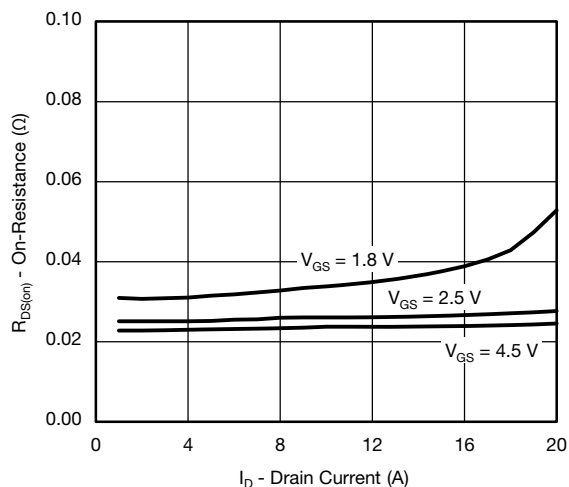
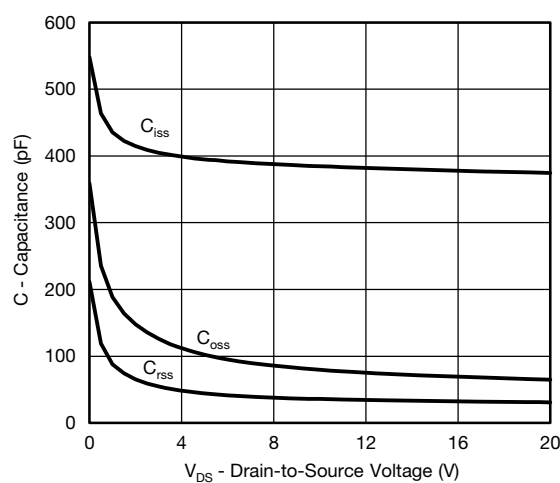


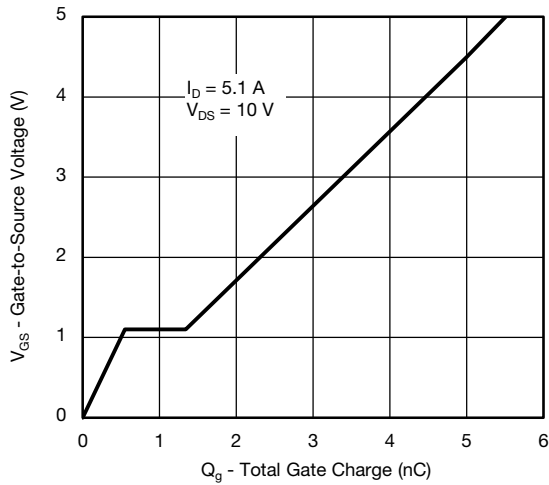
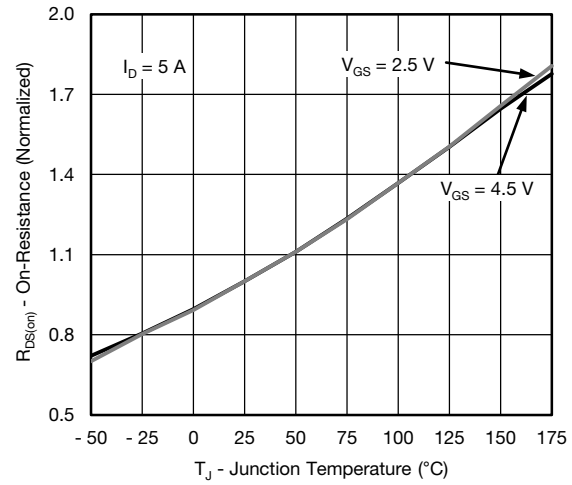
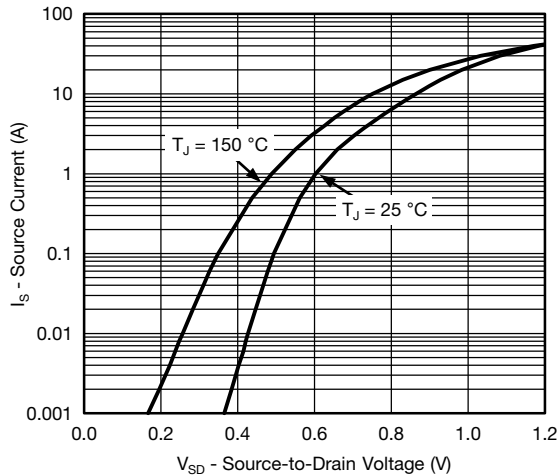
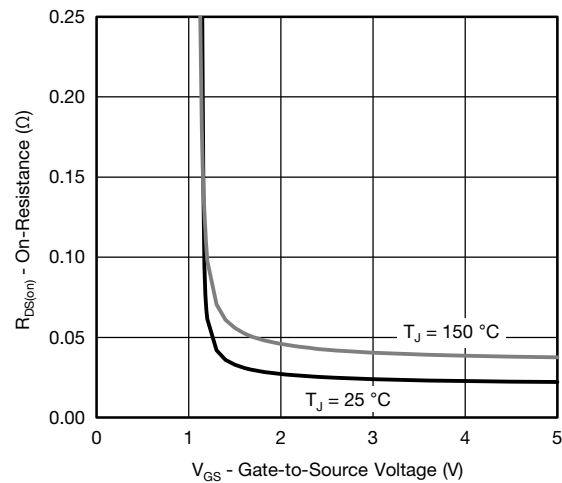
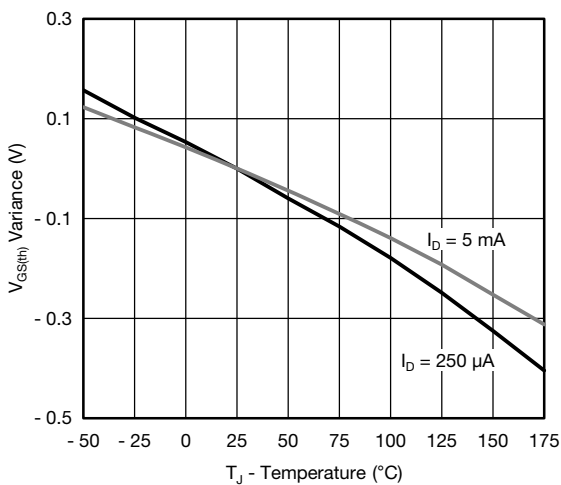
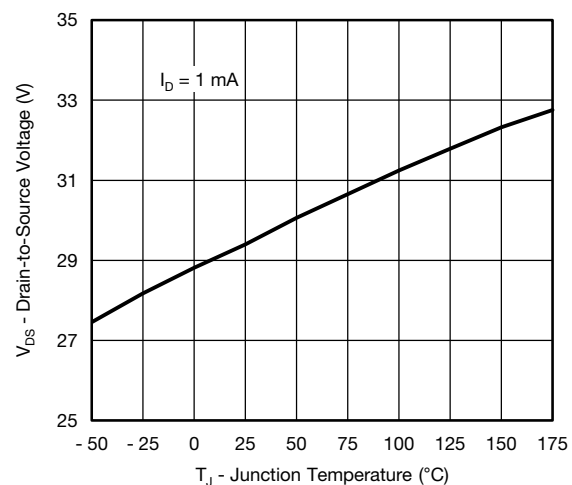
SPECIFICATIONS (T _C = 25 °C, unless otherwise noted)							
PARAMETER	SYMBOL	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT
Static							
Drain-Source Breakdown Voltage	V _{DS}	V _{GS} = 0 V, I _D = 250 μA		20	-	-	V
Gate-Source Threshold Voltage	V _{GS(th)}	V _{DS} = V _{GS} , I _D = 250 μA		0.45	0.6	1.1	
Gate-Source Leakage	I _{GSS}	V _{DS} = 0 V, V _{GS} = ± 8 V		-	-	± 100	nA
Zero Gate Voltage Drain Current	I _{DSS}	V _{GS} = 0 V	V _{DS} = 20 V	-	-	1	μA
		V _{GS} = 0 V	V _{DS} = 20 V, T _J = 125 °C	-	-	50	
		V _{GS} = 0 V	V _{DS} = 20 V, T _J = 175 °C	-	-	250	
On-State Drain Current ^a	I _{D(on)}	V _{GS} = 4.5 V	V _{DS} ≥ 5 V	10	-	-	A
Drain-Source On-State Resistance ^a	R _{DS(on)}	V _{GS} = 4.5 V	I _D = 5 A	-	0.023	0.028	Ω
		V _{GS} = 4.5 V	I _D = 5 A, T _J = 125 °C	-	-	0.042	
		V _{GS} = 4.5 V	I _D = 5 A, T _J = 175 °C	-	-	0.050	
		V _{GS} = 2.5 V	I _D = 4 A	-	0.026	0.034	
		V _{GS} = 1.8 V	I _D = 3 A	-	0.031	0.038	
Forward Transconductance ^b	g _{fs}	V _{DS} = 15 V, I _D = 5 A		-	31	-	S
Dynamic ^b							
Input Capacitance	C _{iss}	V _{GS} = 0 V	V _{DS} = 10 V, f = 1 MHz	-	388	485	pF
Output Capacitance	C _{oss}			-	80	100	
Reverse Transfer Capacitance	C _{rss}			-	36	45	
Total Gate Charge ^c	Q _g	V _{GS} = 4.5 V	V _{DS} = 10 V, I _D = 5.1 A	-	5	8	nC
Gate-Source Charge ^c	Q _{gs}			-	0.55	-	
Gate-Drain Charge ^c	Q _{gd}			-	0.79	-	
Gate Resistance	R _g	f = 1 MHz		6	11.89	18	Ω
Turn-On Delay Time ^c	t _{d(on)}	V _{DD} = 10 V, R _L = 10 Ω I _D ≅ 1 A, V _{GEN} = 4.5 V, R _g = 1 Ω		-	8	12	ns
Rise Time ^c	t _r			-	8	12	
Turn-Off Delay Time ^c	t _{d(off)}			-	21	32	
Fall Time ^c	t _f			-	8	12	
Source-Drain Diode Ratings and Characteristics ^b							
Pulsed Current ^a	I _{SM}			-	-	24	A
Forward Voltage	V _{SD}	I _F = 4.5 A, V _{GS} = 0 V		-	0.75	1.2	V

Notes

- a. Pulse test; pulse width $\leq 300\text{ }\mu\text{s}$, duty cycle $\leq 2\%$.
b. Guaranteed by design, not subject to production testing.
c. Independent of operating temperature.

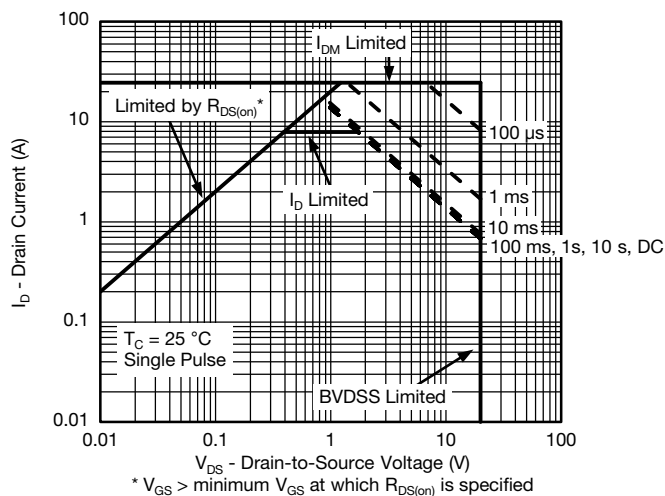
Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

TYPICAL CHARACTERISTICS ($T_A = 25\text{ }^{\circ}\text{C}$, unless otherwise noted)

Output Characteristics

Transfer Characteristics

Transfer Characteristics

Transconductance

On-Resistance vs. Drain Current

Capacitance

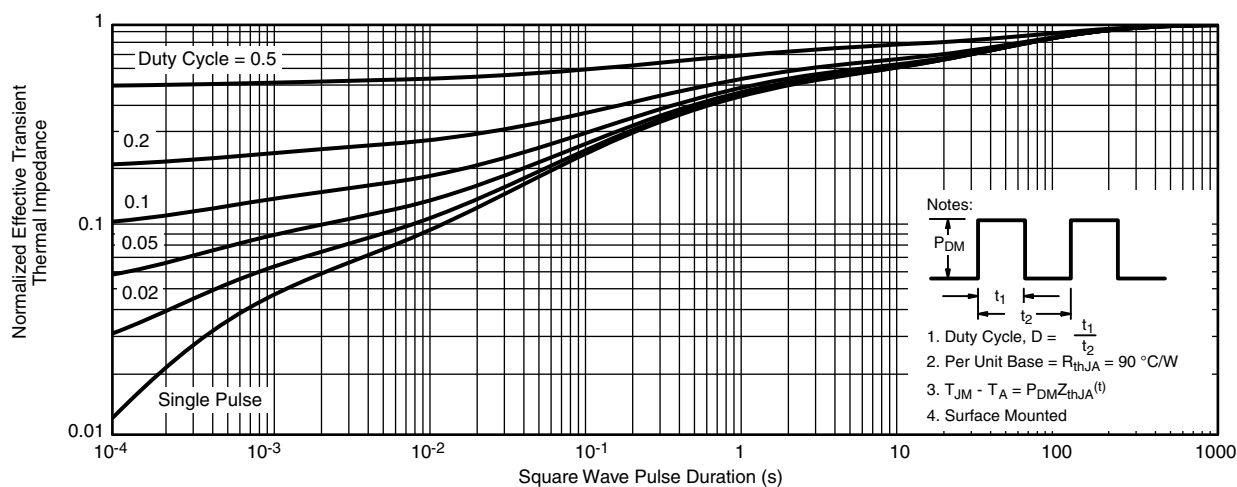
TYPICAL CHARACTERISTICS ($T_A = 25\text{ }^{\circ}\text{C}$, unless otherwise noted)

Gate Charge

On-Resistance vs. Junction Temperature

Source Drain Diode Forward Voltage

On-Resistance vs. Gate-to-Source Voltage

Threshold Voltage

Drain Source Breakdown vs. Junction Temperature



THERMAL RATINGS ($T_A = 25\text{ }^{\circ}\text{C}$, unless otherwise noted)



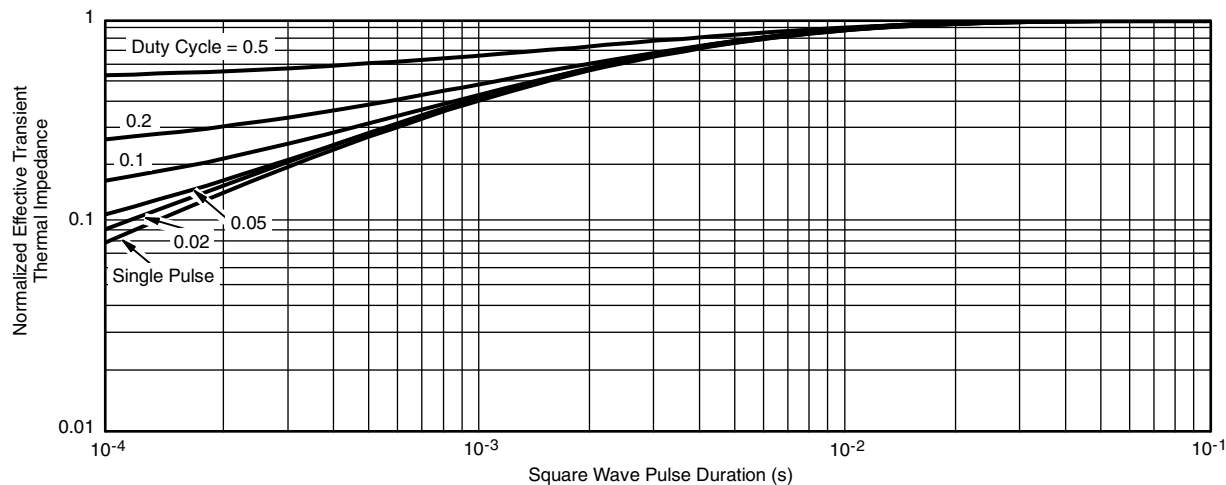
Safe Operating Area



Normalized Thermal Transient Impedance, Junction-to-Ambient



THERMAL RATINGS ($T_A = 25\text{ }^{\circ}\text{C}$, unless otherwise noted)



Normalized Thermal Transient Impedance, Junction-to-Case

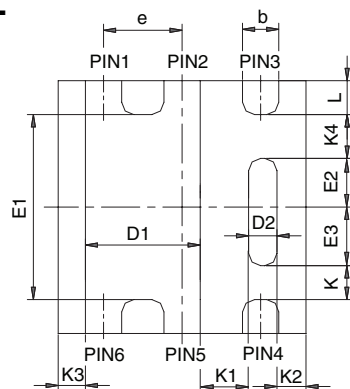
Note

- The characteristics shown in the two graphs
 - Normalized Transient Thermal Impedance Junction-to-Ambient ($25\text{ }^{\circ}\text{C}$)
 - Normalized Transient Thermal Impedance Junction-to-Case ($25\text{ }^{\circ}\text{C}$)are given for general guidelines only to enable the user to get a “ball park” indication of part capabilities. The data are extracted from single pulse transient thermal impedance characteristics which are developed from empirical measurements. The latter is valid for the part mounted on printed circuit board - FR4, size 1" x 1" x 0.062", double sided with 2 oz. copper, 100 % on both sides. The part capabilities can widely vary depending on actual application parameters and operating conditions.

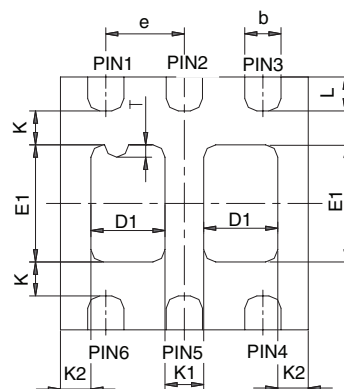
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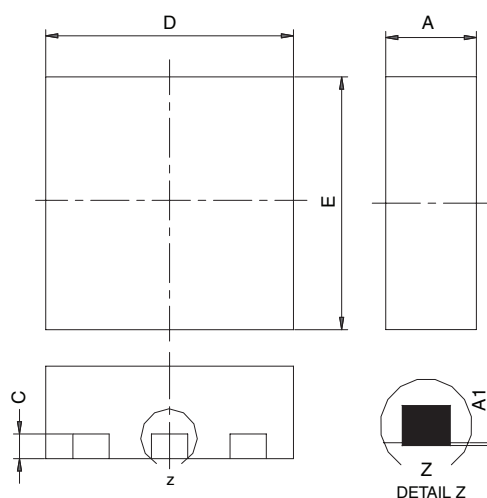
PowerPAK® SC70-6L



BACKSIDE VIEW OF SINGLE



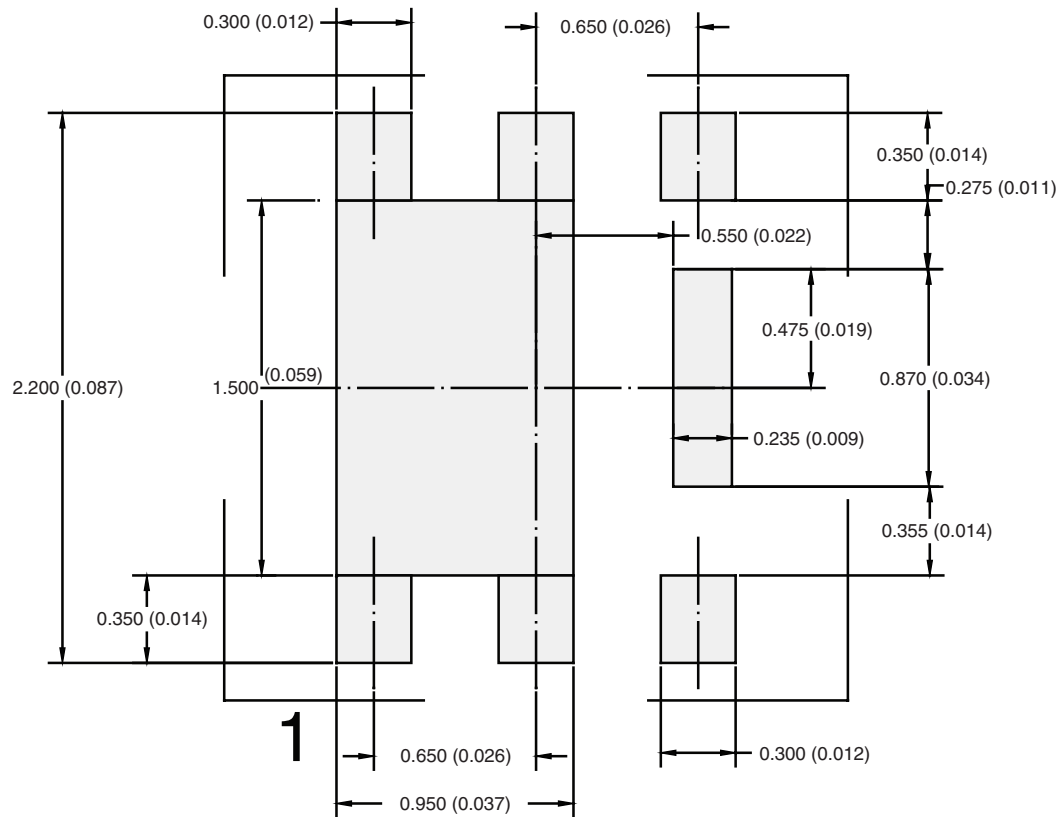
BACKSIDE VIEW OF DUAL



- Notes:
1. All dimensions are in millimeters
 2. Package outline exclusive of mold flash and metal burr
 3. Package outline inclusive of plating

DIM	SINGLE PAD						DUAL PAD					
	MILLIMETERS			INCHES			MILLIMETERS			INCHES		
	Min	Nom	Max	Min	Nom	Max	Min	Nom	Max	Min	Nom	Max
A	0.675	0.75	0.80	0.027	0.030	0.032	0.675	0.75	0.80	0.027	0.030	0.032
A1	0	-	0.05	0	-	0.002	0	-	0.05	0	-	0.002
b	0.23	0.30	0.38	0.009	0.012	0.015	0.23	0.30	0.38	0.009	0.012	0.015
C	0.15	0.20	0.25	0.006	0.008	0.010	0.15	0.20	0.25	0.006	0.008	0.010
D	1.98	2.05	2.15	0.078	0.081	0.085	1.98	2.05	2.15	0.078	0.081	0.085
D1	0.85	0.95	1.05	0.033	0.037	0.041	0.513	0.613	0.713	0.020	0.024	0.028
D2	0.135	0.235	0.335	0.005	0.009	0.013						
E	1.98	2.05	2.15	0.078	0.081	0.085	1.98	2.05	2.15	0.078	0.081	0.085
E1	1.40	1.50	1.60	0.055	0.059	0.063	0.85	0.95	1.05	0.033	0.037	0.041
E2	0.345	0.395	0.445	0.014	0.016	0.018						
E3	0.425	0.475	0.525	0.017	0.019	0.021						
e	0.65 BSC			0.026 BSC			0.65 BSC			0.026 BSC		
K	0.275 TYP			0.011 TYP			0.275 TYP			0.011 TYP		
K1	0.400 TYP			0.016 TYP			0.320 TYP			0.013 TYP		
K2	0.240 TYP			0.009 TYP			0.252 TYP			0.010 TYP		
K3	0.225 TYP			0.009 TYP								
K4	0.355 TYP			0.014 TYP								
L	0.175	0.275	0.375	0.007	0.011	0.015	0.175	0.275	0.375	0.007	0.011	0.015
T							0.05	0.10	0.15	0.002	0.004	0.006
ECN: C-07431 – Rev. C, 06-Aug-07												
DWG: 5934												

RECOMMENDED PAD LAYOUT FOR PowerPAK® SC70-6L Single



Dimensions in mm/(Inches)

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