

128K x 8 Static RAM

Features

- Pin and function compatible with CY7C1019BV33
- High speed
 - $t_{AA} = 8, 10, 12, 15 \text{ ns}$
- CMOS for optimum speed/power
- Data retention at 2.0V
- Center power/ground pinout
- Automatic power-down when deselected
- Easy memory expansion with $\overline{CE}$ and $\overline{OE}$ options
- Available in 48-ball VFBGA, 32-pin TSOP II and 400-mil SOJ package
- Also available in lead-free 48-ball VFBGA and 32-pin TSOP II packages

Functional Description

The CY7C1019CV33 is a high-performance CMOS static RAM organized as 131,072 words by 8 bits. Easy memory

expansion is provided by an active LOW Chip Enable ($\overline{CE}$), an active LOW Output Enable ($\overline{OE}$), and three-state drivers. This device has an automatic power-down feature that significantly reduces power consumption when deselected.

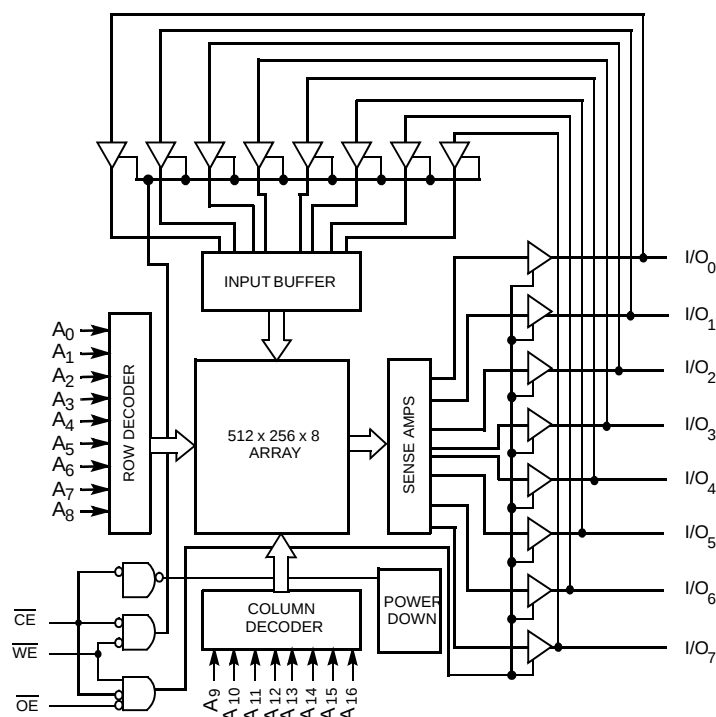
Writing to the device is accomplished by taking Chip Enable ($\overline{CE}$) and Write Enable ($\overline{WE}$) inputs LOW. Data on the eight I/O pins (I/O_0 through I/O_7) is then written into the location specified on the address pins (A_0 through A_{16}).

Reading from the device is accomplished by taking Chip Enable ($\overline{CE}$) and Output Enable ($\overline{OE}$) LOW while forcing Write Enable ($\overline{WE}$) HIGH. Under these conditions, the contents of the memory location specified by the address pins will appear on the I/O pins.

The eight input/output pins (I/O_0 through I/O_7) are placed in a high-impedance state when the device is deselected ($\overline{CE}$ HIGH), the outputs are disabled ($\overline{OE}$ HIGH), or during a write operation ($\overline{CE}$ LOW, and $\overline{WE}$ LOW).

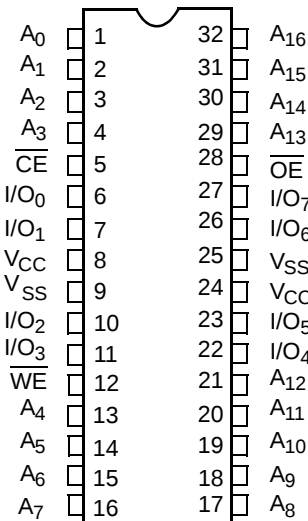
The CY7C1019CV33 is available in Standard 48-ball FBGA, 32-pin TSOP II and 400-mil-wide SOJ packages.

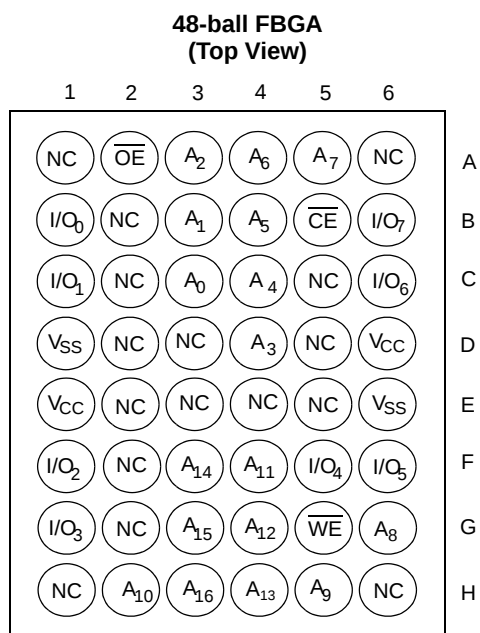
Logic Block Diagram



Pin Configuration

SOJ/TSOP II Top View



Pin Configuration (continued)

Selection Guide

	7C1019CV33-8	7C1019CV33-10	7C1019CV33-12	7C1019CV33-15	Unit
Maximum Access Time	8	10	12	15	ns
Maximum Operating Current	85	80	75	70	mA
Maximum Standby Current	5	5	5	5	mA

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature -65°C to +150°C

Ambient Temperature with
Power Applied -55°C to +125°C

Supply Voltage on V_{CC} to Relative GND^[1] ... -0.5V to + 4.6V

DC Voltage Applied to Outputs
in High-Z State^[1] -0.5V to $V_{CC} + 0.5V$

DC Input Voltage^[1] -0.5V to $V_{CC} + 0.5V$

Current into Outputs (LOW) 20 mA

Static Discharge Voltage >2001V
(per MIL-STD-883, Method 3015)

Latch-up Current >200 mA

Operating Range

Range	Ambient Temperature	V_{CC}
Commercial	0°C to +70°C	3.3V ± 10%
Industrial	-40°C to +85°C	3.3V ± 10%

Electrical Characteristics Over the Operating Range

Parameter	Description	Test Conditions	7C1019CV33 -8		7C1019CV33 -10		7C1019CV33 -12		7C1019CV33 -15		Unit
			Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
V_{OH}	Output HIGH Voltage	$V_{CC} = \text{Min.}, I_{OH} = -4.0 \text{ mA}$	2.4		2.4		2.4		2.4		V
V_{OL}	Output LOW Voltage	$V_{CC} = \text{Min.}, I_{OL} = 8.0 \text{ mA}$		0.4		0.4		0.4		0.4	V
V_{IH}	Input HIGH Voltage		2.0	$V_{CC} + 0.3$	2.0	$V_{CC} + 0.3$	2.0	$V_{CC} + 0.3$	2.0	$V_{CC} + 0.3$	V
V_{IL}	Input LOW Voltage ^[1]		-0.3	0.8	-0.3	0.8	-0.3	0.8	-0.3	0.8	V
I_{IX}	Input Load Current	$GND \leq V_I \leq V_{CC}$	-1	+1	-1	+1	-1	+1	-1	+1	μA
I_{OZ}	Output Leakage Current	$GND \leq V_I \leq V_{CC},$ Output Disabled	-1	+1	-1	+1	-1	+1	-1	+1	μA
$I_{OS}^{[2]}$	Output Short Circuit Current	$V_{CC} = \text{Max.}, V_{OUT} = GND$		-300		-300		-300		-300	mA
I_{CC}	V_{CC} Operating Supply Current	$V_{CC} = \text{Max.}, I_{OUT} = 0 \text{ mA},$ $f = f_{MAX} = 1/t_{RC}$		85		80		75		70	mA
I_{SB1}	Automatic CE Power-down Current — TTL Inputs	Max. $V_{CC}, \overline{CE} \geq V_{IH}$ $V_{IN} \geq V_{IH}$ or $V_{IN} \leq V_{IL}, f = f_{MAX}$		15		15		15		15	mA
I_{SB2}	Automatic CE Power-down Current — CMOS Inputs	Max. $V_{CC}, \overline{CE} \geq V_{CC} - 0.3V,$ $V_{IN} \geq V_{CC} - 0.3V,$ or $V_{IN} \leq 0.3V, f = 0$		5		5		5		5	mA

Capacitance^[3]

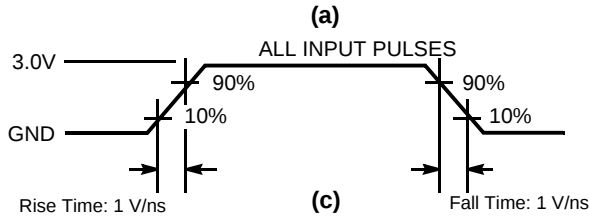
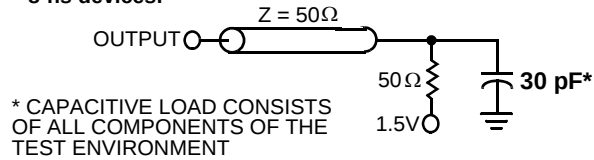
Parameter	Description	Test Conditions	Max.	Unit
C_{IN}	Input Capacitance	$T_A = 25^\circ\text{C}, f = 1 \text{ MHz},$ $V_{CC} = 5.0V$	8	pF
C_{OUT}	Output Capacitance		8	pF

Notes:

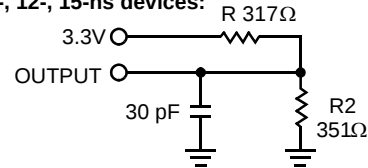
- $V_{IL} (\text{min.}) = -2.0V$ for pulse durations of less than 20 ns.
- Not more than one output should be shorted at one time. Duration of the short circuit should not exceed 30 seconds.
- Tested initially and after any design or process changes that may affect these parameters.

AC Test Loads and Waveforms^[4]

8-ns devices:

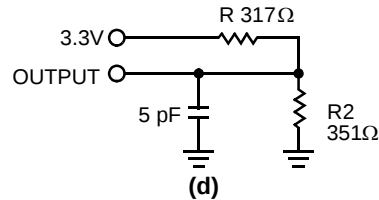


10-, 12-, 15-ns devices:



(b)

High-Z characteristics:



Switching Characteristics^[5] Over the Operating Range

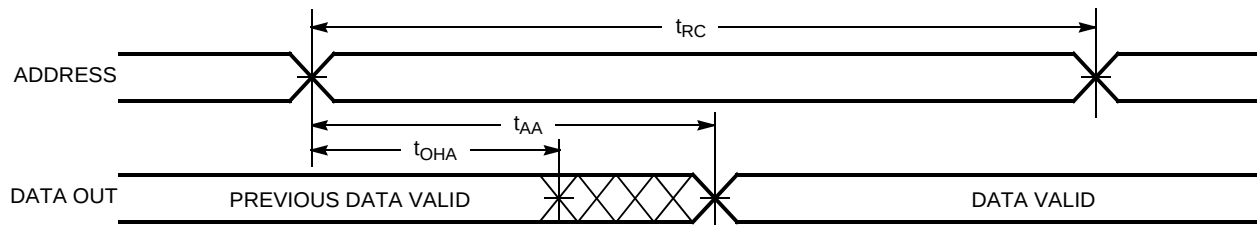
Parameter	Description	7C1019CV33-8		7C1019CV33-10		7C1019CV33-12		7C1019CV33-15		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Read Cycle										
t _{RC}	Read Cycle Time	8		10		12		15		ns
t _{AA}	Address to Data Valid		8		10		12		15	ns
t _{OHA}	Data Hold from Address Change	3		3		3		3		ns
t _{ACE}	$\overline{\text{CE}}$ LOW to Data Valid		8		10		12		15	ns
t _{DOE}	$\overline{\text{OE}}$ LOW to Data Valid		5		5		6		7	ns
t _{LZOE}	$\overline{\text{OE}}$ LOW to Low Z	0		0		0		0		ns
t _{HZOE}	$\overline{\text{OE}}$ HIGH to High Z ^[6, 7]		4		5		6		7	ns
t _{LZCE}	$\overline{\text{CE}}$ LOW to Low Z ^[7]	3		3		3		3		ns
t _{HZCE}	$\overline{\text{CE}}$ HIGH to High Z ^[6, 7]		4		5		6		7	ns
t _{PU} ^[8]	$\overline{\text{CE}}$ LOW to Power-Up	0		0		0		0		ns
t _{PD} ^[8]	$\overline{\text{CE}}$ HIGH to Power-Down		8		10		12		15	ns
Write Cycle ^[9, 10]										
t _{WC}	Write Cycle Time	8		10		12		15		ns
t _{SCE}	$\overline{\text{CE}}$ LOW to Write End	7		8		9		10		ns
t _{AW}	Address Set-Up to Write End	7		8		9		10		ns
t _{HA}	Address Hold from Write End	0		0		0		0		ns
t _{SA}	Address Set-Up to Write Start	0		0		0		0		ns
t _{PWE}	$\overline{\text{WE}}$ Pulse Width	6		7		8		10		ns
t _{SD}	Data Set-Up to Write End	5		5		6		8		ns
t _{HD}	Data Hold from Write End	0		0		0		0		ns
t _{LZWE}	$\overline{\text{WE}}$ HIGH to Low Z ^[7]	3		3		3		3		ns
t _{HZWE}	$\overline{\text{WE}}$ LOW to High Z ^[6, 7]		4		5		6		7	ns

Notes:

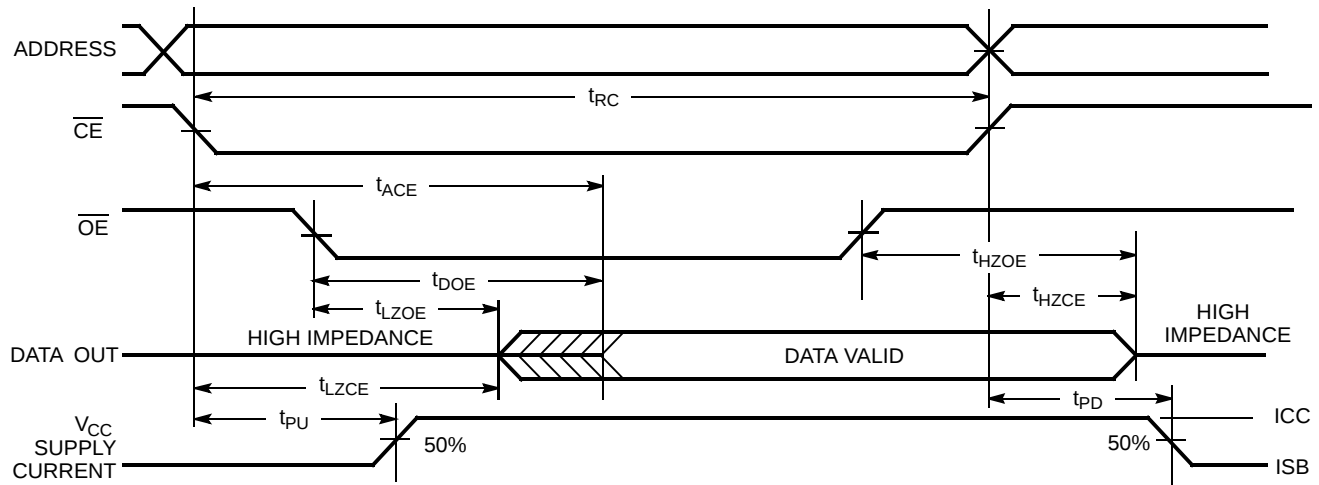
- AC characteristics (except High-Z) for all 8-ns parts are tested using the load conditions shown in Figure (a). All other speeds are tested using the Thevenin load shown in Figure (b). High-Z characteristics are tested for all speeds using the test load shown in Figure (d).
- Test conditions assume signal transition time of 3 ns or less, timing reference levels of 1.5V, input pulse levels of 0 to 3.0V.
- t_{HZOE} , t_{HZCE} , and t_{HZWE} are specified with a load capacitance of 5 pF as in part (d) of AC Test Loads. Transition is measured ± 500 mV from steady-state voltage.
- At any given temperature and voltage condition, t_{HZCE} is less than t_{LZCE} , t_{HZOE} is less than t_{LZOE} , and t_{HZWE} is less than t_{LZWE} for any given device.
- This parameter is guaranteed by design and is not tested.
- The internal write time of the memory is defined by the overlap of $\overline{CE}$ LOW and $\overline{WE}$ LOW. $\overline{CE}$ and $\overline{WE}$ must be LOW to initiate a write, and the transition of any of these signals can terminate the write. The input data set-up and hold timing should be referenced to the leading edge of the signal that terminates the write.
- The minimum write cycle time for Write Cycle no. 3 ($\overline{WE}$ controlled, $\overline{OE}$ LOW) is the sum of t_{HZWE} and t_{SD} .

Switching Waveforms

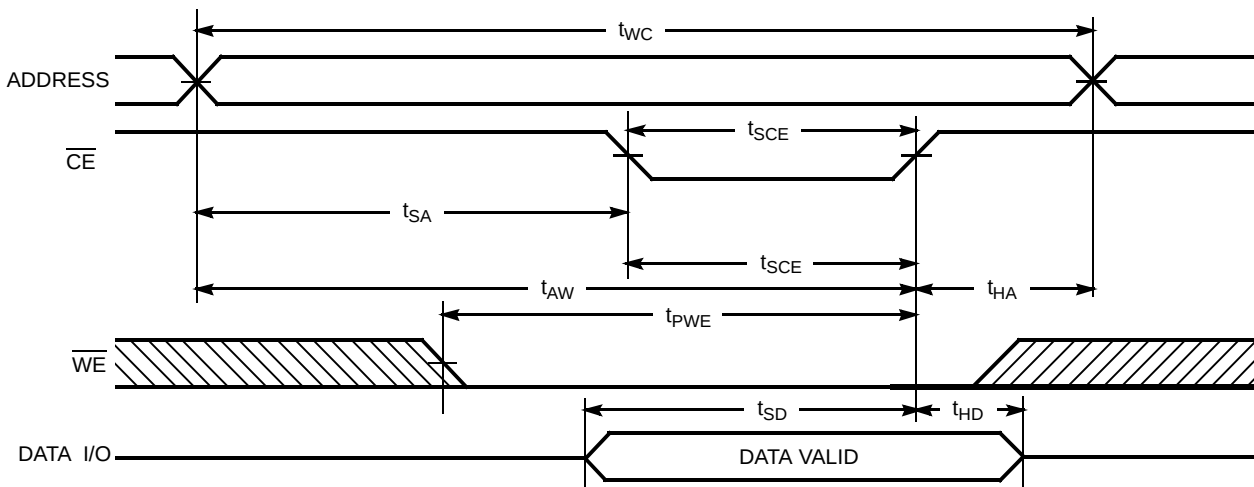
Read Cycle No. 1^[11, 12]



Read Cycle No. 2 ($\overline{OE}$ Controlled)^[12, 13]

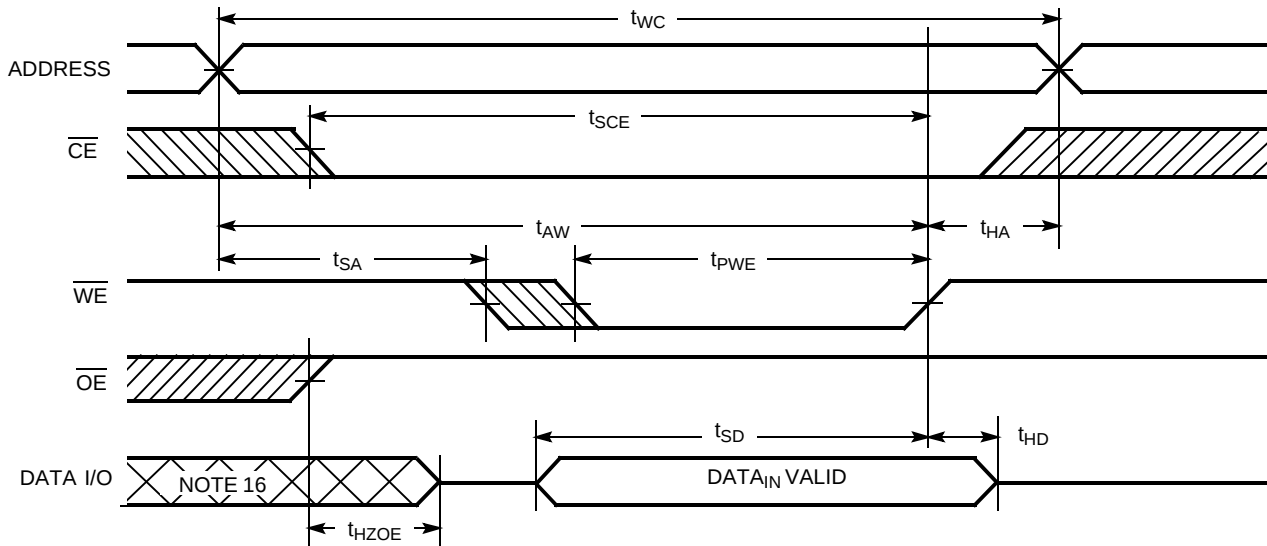
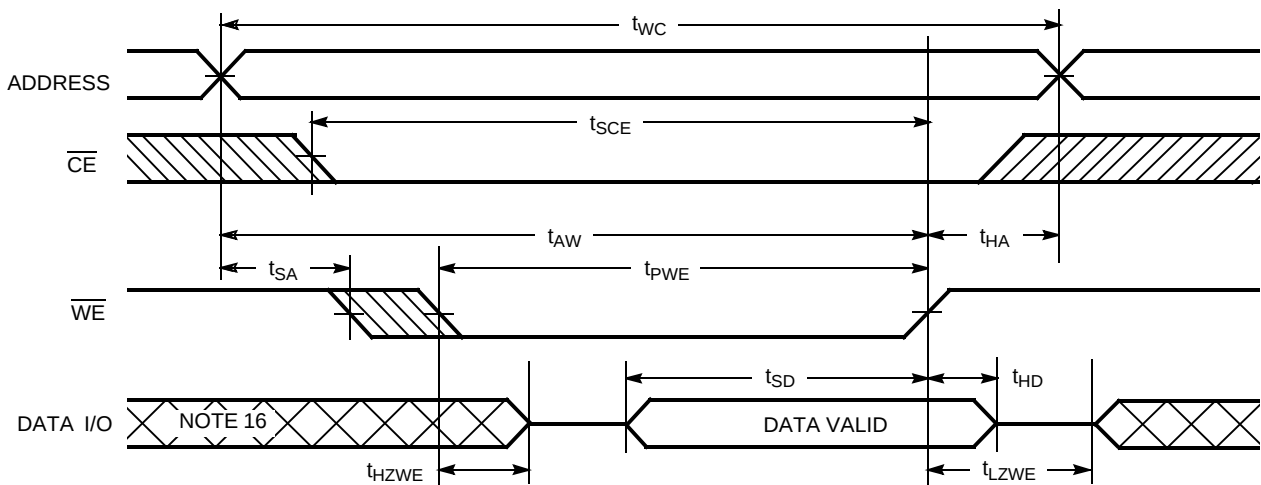


Write Cycle No. 1 ($\overline{CE}$ Controlled)^[14, 15]



Notes:

11. Device is continuously selected. $\overline{OE}$, $\overline{CE} = V_{IL}$.
12. WE is HIGH for read cycle.
13. Address valid prior to or coincident with $\overline{CE}$ transition LOW.
14. Data I/O is high impedance if $\overline{OE} = V_{IL}$.
15. If CE goes HIGH simultaneously with WE going HIGH, the output remains in a high-impedance state.

Switching Waveforms (continued)
Write Cycle No. 2 ($\overline{\text{WE}}$ Controlled, $\overline{\text{OE}}$ HIGH During Write)^[14, 15]

Write Cycle No. 3 ($\overline{\text{WE}}$ Controlled, $\overline{\text{OE}}$ LOW)^[15]

Truth Table

$\overline{\text{CE}}$	$\overline{\text{OE}}$	$\overline{\text{WE}}$	I/O ₀ -I/O ₇	Mode	Power
H	X	X	High Z	Power-Down	Standby (I_{SB})
L	L	H	Data Out	Read	Active (I_{CC})
L	X	L	Data In	Write	Active (I_{CC})
L	H	H	High Z	Selected, Outputs Disabled	Active (I_{CC})

Note:

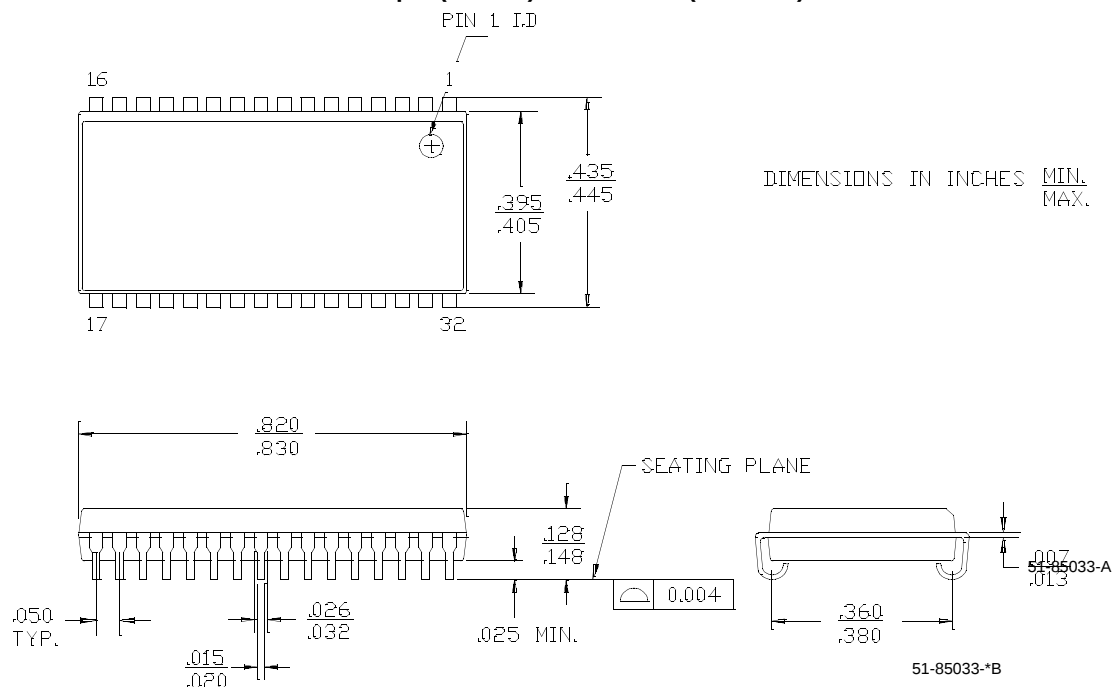
16. During this period the I/Os are in the output state and input signals should not be applied.

Ordering Information

Speed (ns)	Ordering Code	Package Diagram	Package Type	Operating Range
8	CY7C1019CV33-8VC	51-85033	32-pin 400-Mil Molded SOJ	Commercial
	CY7C1019CV33-8VI	51-85033	32-pin 400-Mil Molded SOJ	Industrial
10	CY7C1019CV33-10VC	51-85033	32-pin 400-Mil Molded SOJ	Commercial
	CY7C1019CV33-10ZC	51-85095	32-pin TSOP II	
	CY7C1019CV33-10ZXC	51-85095	32-pin TSOP II (Pb-Free)	
	CY7C1019CV33-10VI	51-85033	32-pin 400-Mil Molded SOJ	Industrial
	CY7C1019CV33-10ZI	51-85095	32-pin TSOP II	
	CY7C1019CV33-10ZXI	51-85095	32-pin TSOP II (Pb-Free)	
12	CY7C1019CV33-12VC	51-85033	32-pin 400-Mil Molded SOJ	Commercial
	CY7C1019CV33-12ZC	51-85095	32-pin TSOP II	
	CY7C1019CV33-12ZXC	51-85095	32-pin TSOP II (Pb-Free)	
	CY7C1019CV33-12VI	51-85033	32-pin 400-Mil Molded SOJ	Industrial
	CY7C1019CV33-12ZI	51-85095	32-pin TSOP II	
	CY7C1019CV33-12BVI	51-85150	48-ball VFBGA	
	CY7C1019CV33-12BVXI	51-85150	48-ball VFBGA (Pb-Free)	
15	CY7C1019CV33-15VC	51-85033	32-pin 400-Mil Molded SOJ	Commercial
	CY7C1019CV33-15ZC	51-85095	32-pin TSOP II	
	CY7C1019CV33-15ZXC	51-85095	32-pin TSOP II (Pb-Free)	
	CY7C1019CV33-15VI	51-85033	32-pin 400-Mil Molded SOJ	Industrial
	CY7C1019CV33-15ZI	51-85095	32-pin TSOP II	
	CY7C1019CV33-15ZXI	51-85095	32-pin TSOP II (Pb-Free)	

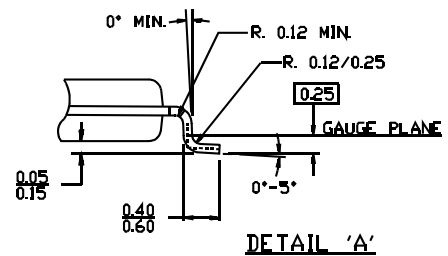
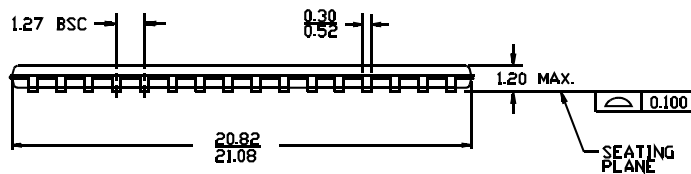
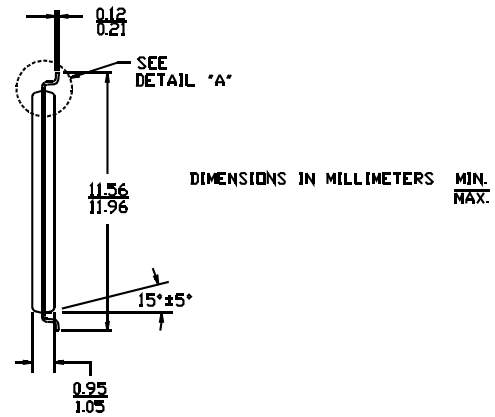
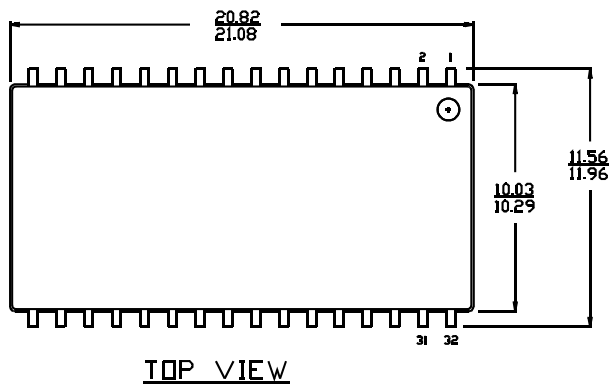
Package Diagrams

32-pin (400-Mil) Molded SOJ (51-85033)

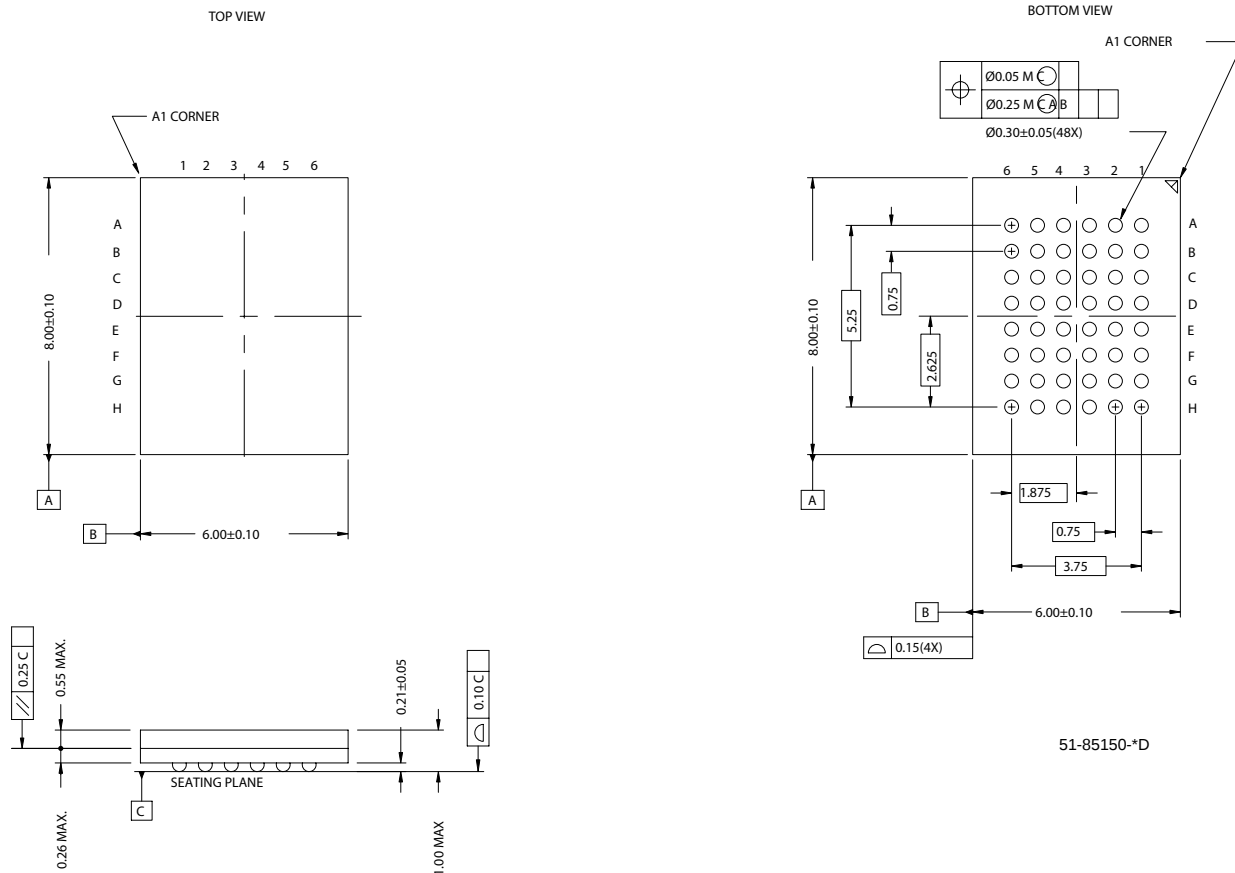


Package Diagrams (continued)

32-pin TSOP II ZS32 (51-85095)



51-85095-**

Package Diagrams (continued)
48-ball VFBGA (6 x 8 x 1 mm) (51-85150)


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Document History Page

Document Title: CY7C1019CV33 128K x 8 Static RAM Document Number: 38-05130				
REV.	ECN NO.	Issue Date	Orig. of Change	Description of Change
**	109245	12/16/01	HGK	New Data Sheet
*A	113431	04/10/02	NSL	AC Test Loads split based on speed.
*B	115047	08/01/02	HGK	Added TSOP II Package and I Temp. Improved I _{CC} limits.
*C	119796	10/11/02	DFP	Updated standby current from 5 nA to 5 mA.
*D	123030	12/17/02	DFP	Updated Truth Table to reflect single Chip Enable option.
*E	419983	See ECN	NXR	Added 48-ball VFBGA Package Added lead-free parts in Ordering Information Table Replaced Package Name column with Package Diagram in the Ordering Information table.