

SN54LS640 THRU SN54LS642, SN54LS644, SN54LS645 SN74LS640 THRU SN74LS642, SN74LS644, SN74LS645 OCTAL BUS TRANSCEIVERS

SDLS189 – APRIL 1979 – REVISED MARCH 1988

- **SN74LS64X-1 Versions Rated at I_{OL} of 48 mA**
- **Bi-directional Bus Transceivers in High-Density 20-Pin Packages**
- **Hysteresis at Bus Inputs Improves Noise Margins**
- **Choice of True or Inverting Logic**
- **Choice of 3-State or Open-Collector Outputs**

DEVICE	OUTPUT	LOGIC
'LS640	3-State	Inverting
'LS641	Open-Collector	True
'LS642	Open-Collector	Inverting
'LS644	Open-Collector	True and inverting
'LS645	3-State	True

description

These octal bus transceivers are designed for asynchronous two-way communication between data buses. The devices transmit data from the A bus to the B bus or from the B bus to the A bus depending upon the level at the direction control (DIR) input. The enable input ($\bar{G}$) can be used to disable the device so the buses are effectively isolated.

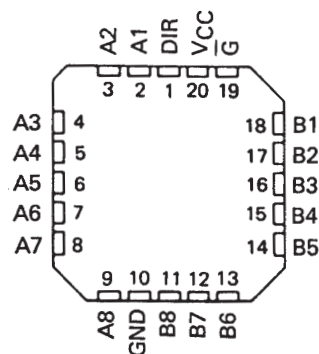
The -1 versions of the SN74LS640 thru SN74LS642, SN74LS644, and SN74LS645 are identical to the standard versions except that the recommended maximum I_{OL} is increased to 48 milliamperes. There are no -1 versions of the SN54LS640 thru SN54LS642, SN54LS644, and SN54LS645.

The SN54LS640 thru SN54LS642, SN54LS644, and SN54LS645 are characterized for operation over the full military temperature range of -55°C to 125°C . The SN74LS640 thru SN74LS642, SN74LS644, and SN74LS645 are characterized for operation from 0°C to 70°C .

SN54LS' . . . J PACKAGE
SN74LS' . . . DW OR N PACKAGE
(TOP VIEW)



SN54LS' . . . FK PACKAGE
(TOP VIEW)



FUNCTION TABLE

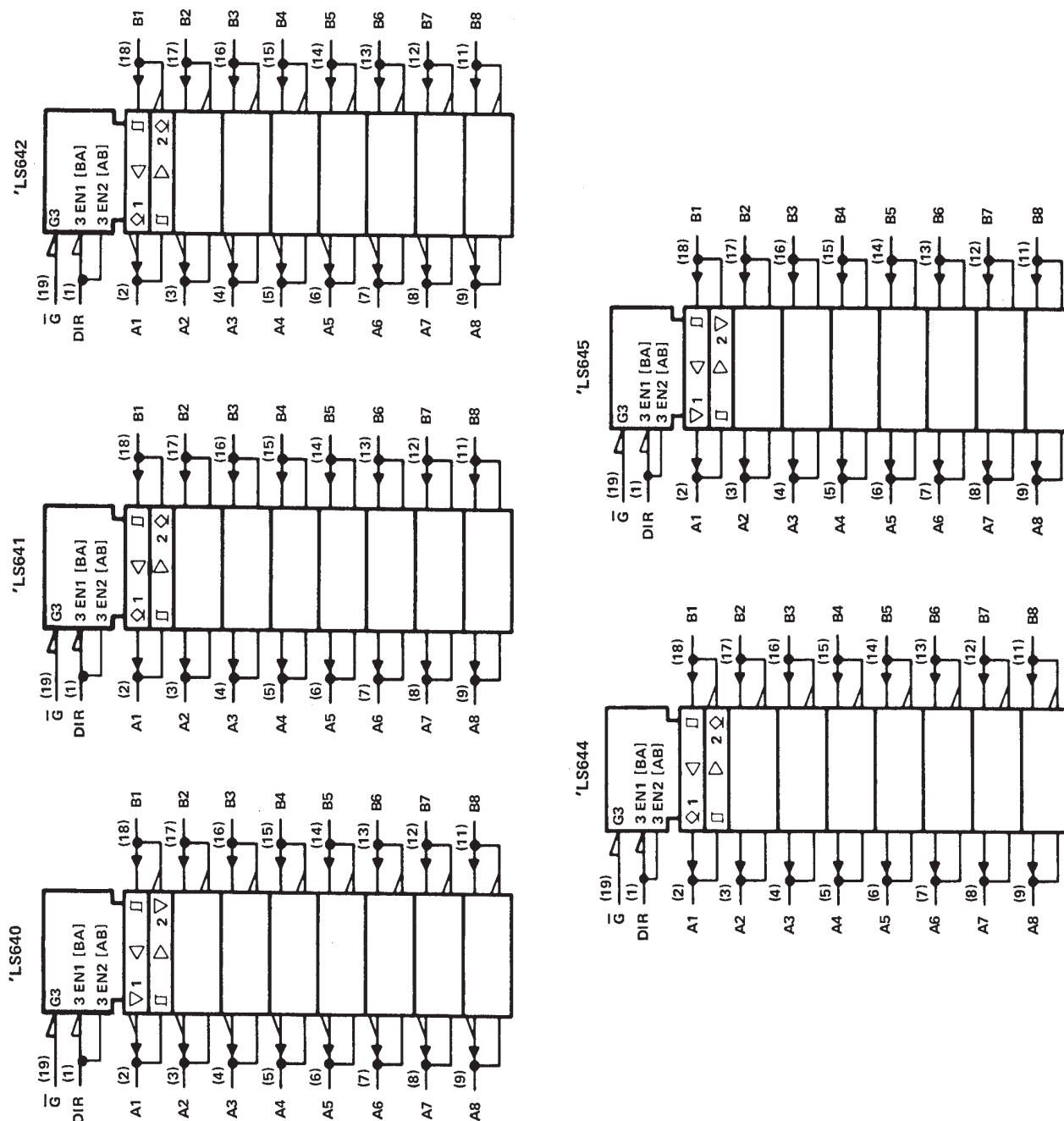
CONTROL INPUTS		OPERATION		
$\bar{G}$	DIR	'LS640 'LS642	'LS641 'LS645	'LS644
L	L	B data to A bus	B data to A bus	B data to A bus
L	H	A data to B bus	A data to B bus	$\bar{A}$ data to B bus
H	X	Isolation	Isolation	Isolation

H = high level, L = low level, X = irrelevant

SN54LS640 THRU SN54LS642, SN54LS644, SN54LS645 SN74LS640 THRU SN74LS642, SN74LS644, SN74LS645 OCTAL BUS TRANSCEIVERS

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logic symbols†

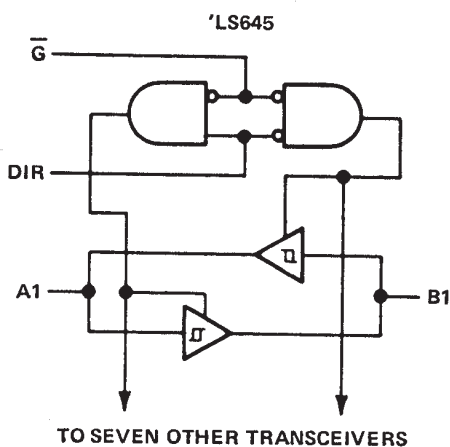
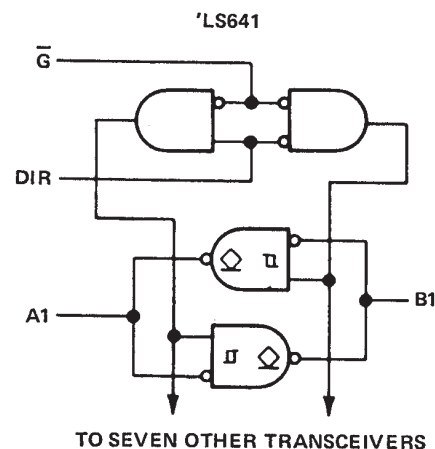
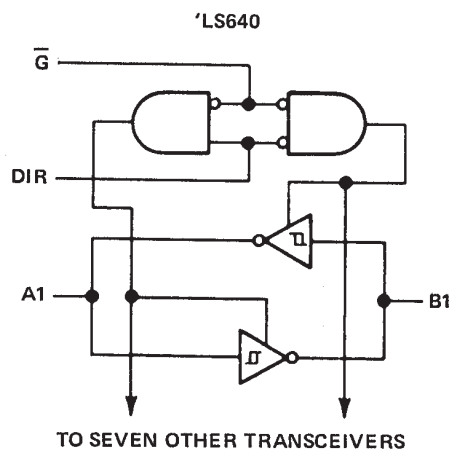


† These symbols are in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for DW, J, and N packages.

SN54LS640 THRU SN54LS642, SN54LS644, SN54LS645
 SN74LS640 THRU SN74LS642, SN74LS644, SN74LS645
 OCTAL BUS TRANSCEIVERS

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logic diagrams (positive logic)



SN54LS640, SN54LS645
SN74LS640, SN74LS645
OCTAL BUS TRANSCEIVERS WITH 3-STATE OUTPUTS

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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1)	7 V
Input voltage: All inputs	7 V
I/O ports	5.5 V
Operating free-air temperature range: SN54LS640, SN54LS645	– 55 °C to 125 °C
SN74LS640, SN74LS645	0 °C to 70 °C
Storage temperature range	– 65 °C to 150 °C

NOTE 1: Voltage values are with respect to network ground terminal.

recommended operating conditions

PARAMETER	SN54LS640 SN54LS645			SN74LS640 SN74LS645			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC} Supply voltage	4.5	5	5.5	4.75	5	5.25	V
V_{IH} High-level input voltage	2			2			V
V_{IL} Low-level input voltage			0.5			0.6	V
I_{OH} High-level output current			– 12			– 15	mA
I_{OL} Low-level output current			12			24	mA
						48†	
T_A Operating free-air temperature	– 55		125	0		70	°C

†The 48-mA limit applies for the SN74LS640-1 and SN74LS645-1 only.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS†		SN54LS640 SN54LS645		SN74LS640 SN74LS645		UNIT
				MIN	TYP‡	MAX	MIN	
V _{IK}		V _{CC} = MIN, I _I = – 18 mA				– 1.5		V
Hysteresis (V _{T+} – V _{T–})		V _{CC} = MIN,	A or B input	0.1	0.4		0.2 0.4	V
V _{OH}		V _{CC} = MIN, V _{IH} = 2 V, V _{IL} = MAX	I _{OH} = – 3 mA	2.4	3.4		2.4 3.4	
			I _{OH} = MAX	2		2		
V _{OL}		V _{CC} = MIN, V _{IH} = 2 V, V _{IL} = MAX	I _{OL} = 12 mA	0.25 0.4		0.25 0.4		V
			I _{OL} = 24 mA			0.35 0.5		
			I _{OL} = 48 mA#			0.4 0.5		
I _{OZH}		V _{CC} = MAX, $\bar{G}$ at 2 V, V _O = 2.7 V		20		20		μA
I _{OZL}		V _{CC} = MAX, $\bar{G}$ at 2 V, V _O = 0.4 V		– 0.4		– 0.4		mA
I _I	A or B	V _{CC} = MAX	V _I = 5.5 V	0.1		0.1		mA
	DIR or $\bar{G}$		V _I = 7 V	0.1		0.1		
I _{IH}		V _{CC} = MAX, V _{IH} = 2.7 V		20		20		μA
I _{IL}		V _{CC} = MAX, V _{IL} = 0.4 V		– 0.4		– 0.4		mA
I _{OS} †		V _{CC} = MAX		– 40	– 225	– 40	– 225	mA
I _{CC}	Outputs high	V _{CC} = MAX, Outputs open		48	70	48	70	mA
	Outputs low			62	90	62	90	
	Outputs at Hi-Z			64	95	64	95	

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

‡All typical values are at $V_{CC} = 5 \text{ V}, T_A = 25^\circ\text{C}$.

†Not more than one output should be shorted at a time, and duration of the short-circuit should not exceed one second.

‡The 48-mA condition applies for the SN74LS640-1 and SN74LS645-1 only.

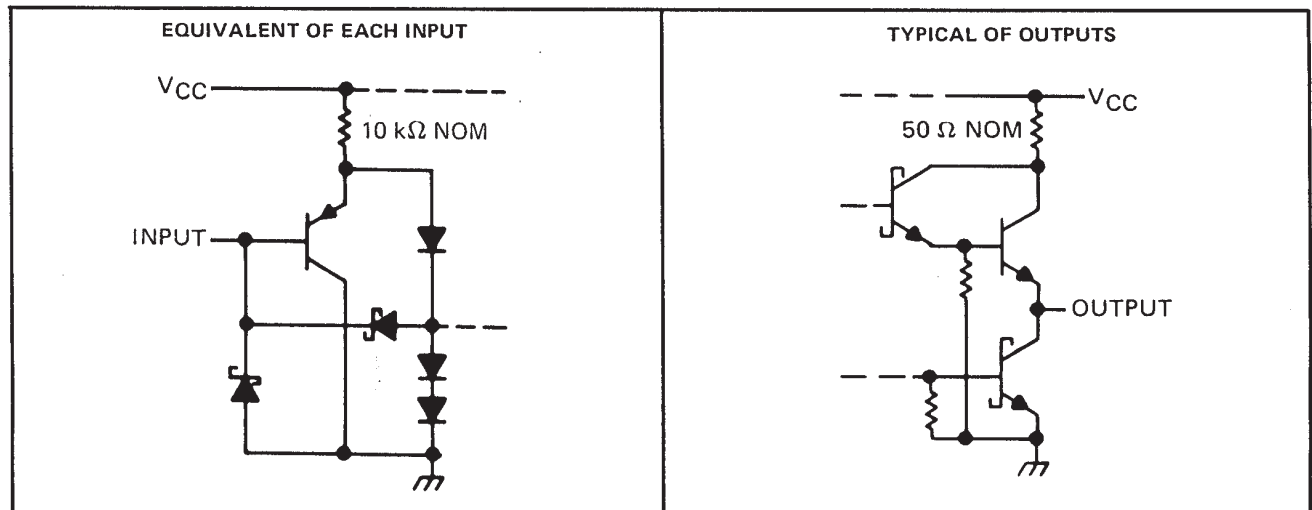


switching characteristics, $V_{CC} = 5\text{ V}$, $T_A = 25^\circ\text{C}$

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	'LS640, 'LS640-1			'LS645, 'LS645-1			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
t_{PLH} Propagation delay time, low-to-high-level output	A	B	$C_L = 45\text{ pF}$, $R_L = 667\ \Omega$, See Note 2		6	10		8	15	ns
	B	A			6	10		8	15	
t_{PHL} Propagation delay time, high-to-low-level output	A	B			8	15		11	15	ns
	B	A			8	15		11	15	
t_{PZL} Output enable time to low level	$\overline{G}$	A			31	40		31	40	ns
	$\overline{G}$	B			31	40		31	40	
t_{PZH} Output enable time to high level	$\overline{G}$	A			23	40		26	40	ns
	$\overline{G}$	B			23	40		26	40	
t_{PLZ} Output disable time from low level	$\overline{G}$	A	$C_L = 5\text{ pF}$, $R_L = 667\ \Omega$, See Note 2		15	25		15	25	ns
	$\overline{G}$	B			15	25		15	25	
t_{PHZ} Output disable time from high level	$\overline{G}$	A			15	25		15	25	ns
	$\overline{G}$	B			15	25		15	25	

NOTE 2: Load circuits and voltage waveforms are shown in Section 1.

schematics of inputs and outputs



SN54LS640, SN54LS645
SN74LS640, SN74LS645
OCTAL BUS TRANSCEIVERS WITH 3-STATE OUTPUTS

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TYPICAL CHARACTERISTICS

SN54LS'
INVERTING OUTPUT VOLTAGE
 vs
INPUT VOLTAGE

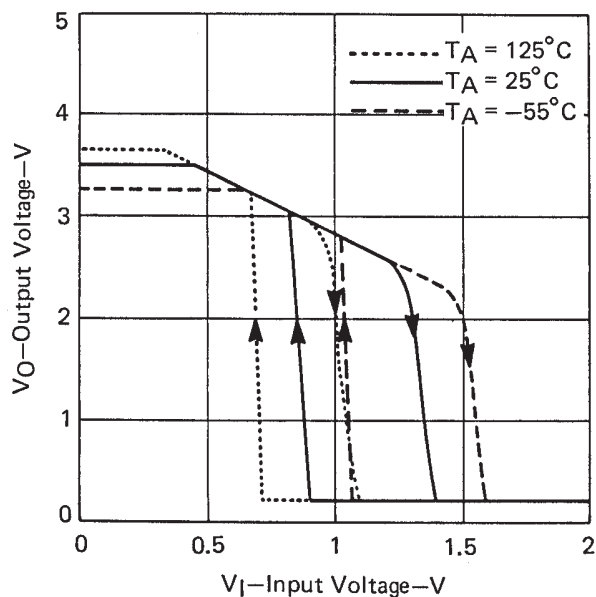


FIGURE 1

SN74LS'
INVERTING OUTPUT VOLTAGE
 vs
INPUT VOLTAGE

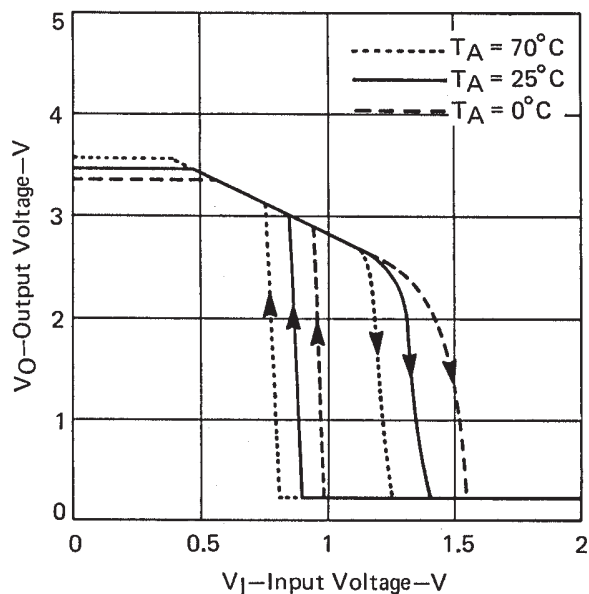


FIGURE 2

SN54LS'
NONINVERTING OUTPUT VOLTAGE
 vs
INPUT VOLTAGE



FIGURE 3

SN74LS'
NONINVERTING OUTPUT VOLTAGE
 vs
INPUT VOLTAGE



FIGURE 4

SN54LS641, SN54LS642, SN54LS644
SN74LS641, SN74LS642, SN74LS644
OCTAL BUS TRANSCEIVERS WITH OPEN-COLLECTOR OUTPUTS
SDLS189 – APRIL 1979 – REVISED MARCH 1988

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1)	7 V
Input voltage: All inputs and I/O ports	7 V
Operating free-air temperature range: SN54LS641, SN54LS642, SN54LS644	– 55° C to 125° C
SN74LS641, SN74LS642, SN74LS644	0° C to 70° C
Storage temperature range	– 65° C to 150° C

NOTE 1: Voltage values are with respect to network ground terminal.

recommended operating conditions

PARAMETER	SN54LS641 SN54LS642 SN54LS644			SN74LS641 SN74LS642 SN74LS644			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC} Supply voltage	4.5	5	5.5	4.75	5	5.25	V
V_{IH} High-level input voltage	2			2			V
V_{IL} Low-level input voltage			0.5			0.6	V
V_{OH} High-level output voltage			5.5			5.5	V
I_{OL} Low-level output current			12			24	mA
						48 [§]	
T_A Operating free-air temperature	– 55		125	0		70	°C

[§]The 48 mA limit applies for the SN74LS641-1, SN74LS642-1, and SN74LS644-1 only.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS†		SN54LS641 SN54LS642 SN54LS644		SN74LS641 SN74LS642 SN74LS644		UNIT
				MIN	TYP‡	MAX	MIN	
VIK		VCC = MIN,	II = − 18 mA	− 1.5		− 1.5		V
Hysteresis (VT+ − VT−)		VCC = MIN,	A or B input	0.1	0.4	0.2	0.4	V
IOH		VCC = MIN, VIL = MAX,	VIH = 2 V, VOH = 5.5 V	0.1		0.1		mA
VOL		VCC = MIN, VIH = 2 V, VIL = MAX	IOL = 12 mA	0.25	0.4	0.25	0.4	V
			IOL = 24 mA			0.35	0.5	
			IOL = 48 mA§			0.4	0.5	
II	A or B	VCC = MAX	VI = 5.5 V	0.1		0.1		mA
	DIR or G		VI = 7 V	0.1		0.1		
IIH		VCC = MAX,	VI = 2.7 V	20		20		μA
IIL		VCC = MAX,	VI = 0.4 V	− 0.4		− 0.4		mA
ICC	Outputs high	VCC = MAX,	Outputs open	48	70	48	70	mA
	Outputs low			62	90	62	90	
	Outputs at Hi-Z			64	95	64	95	

[†] For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

[‡] All typical values are at $V_{CC} = 5 \text{ V}, T_A = 25^\circ\text{C}$.

[§]The 48 mA condition applies for the SN74LS641-1, SN74LS642-1, and SN74LS644-1 only.

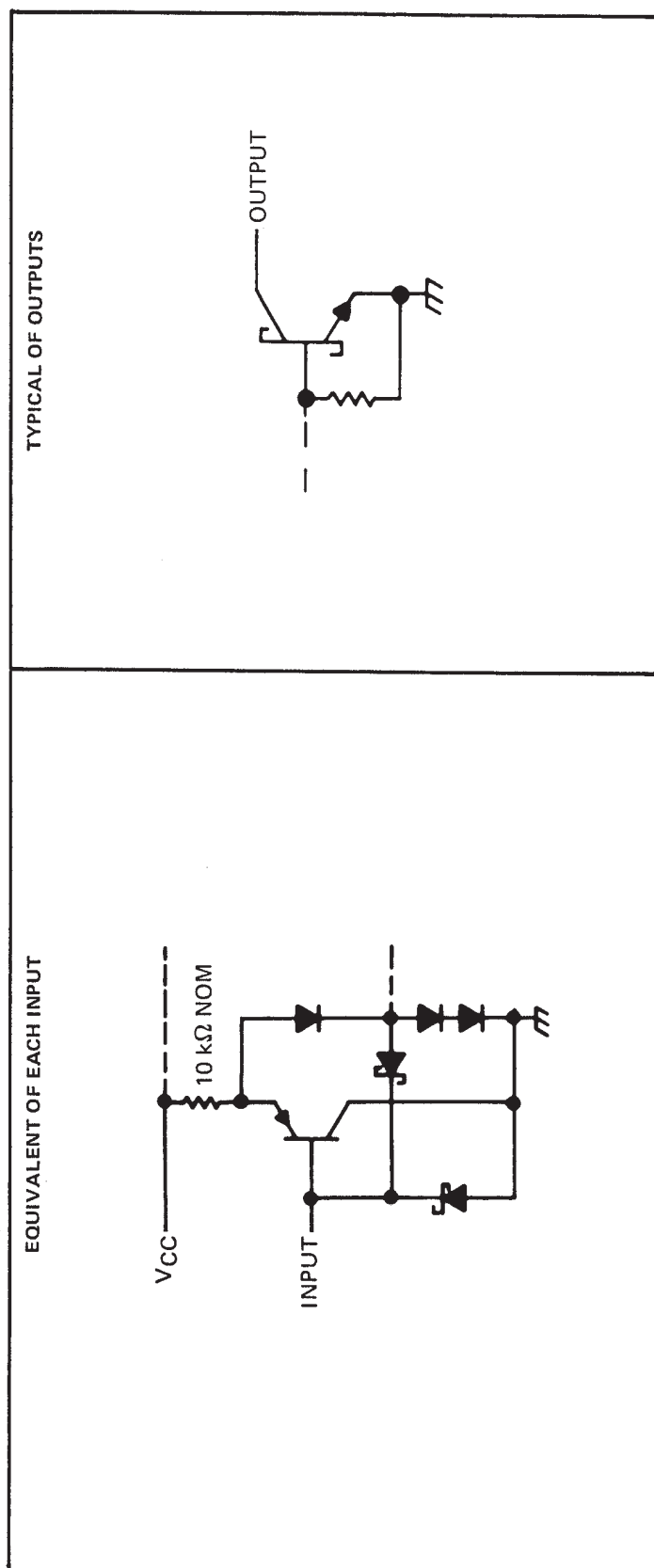
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switching characteristics at $V_{CC} = 5\text{ V}$, $T_A = 25^\circ\text{C}$

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	'LS641, 'LS641-1		'LS642, 'LS642-1		'LS644, 'LS644-1		UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
t _{PLH} Propagation delay time, low-to-high-level output	A	B	C _L = 45 pF, R _L = 667 Ω, See Note 2	17	25	19	25	17	25	ns
	B	A		17	25	19	25	19	25	
t _{PHL} Propagation delay time, high-to-low-level output	A	B		16	25	14	25	14	25	ns
	B	A		16	25	14	25	16	25	
t _{PLH} Output disable time from low level	$\bar{G}$, DIR	A	23	40	26	40	26	40	ns	
	$\bar{G}$, DIR	B	25	40	28	40	25	40		
t _{PHL} Output enable time from high level	$\bar{G}$, DIR	A	34	50	43	60	43	60	ns	
	$\bar{G}$, DIR	B	37	50	39	60	37	50		

NOTE 2: Load circuits and voltage waveforms are shown in Section 1.

schematics of inputs and outputs



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SN74LS641, Octal bus transceivers with open collector outputs

DEVICE STATUS: **ACTIVE**

PARAMETER NAME	SN74LS641	SN74LS641-1
Voltage Nodes (V)	5	5
Vcc range (V)	4.75 to 5.25	4.75 to 5.25
Input Level	TTL	TTL
Output Level	TTL	TTL
Output Drive (mA)	- /24	- /48
No. of Outputs	8	8
Logic	True	True
Static Current	80	80
tpd max (ns)	25	25

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- SN74LS64X-1 Versions Rated at I_{OL} of 48 mA
- Bi-directional Bus Transceivers in High-Density 20-Pin Packages
- Hysteresis at Bus Inputs Improves Noise Margins
- Choice of True or Inverting Logic
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DESCRIPTION

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These octal bus transceivers are designed for asynchronous two-way communication between data buses. The devices transmit data from the A bus to the B bus or from the B bus to the A bus depending upon the level at the direction control (DIR) input. The enable input (G_\) can be used to disable the device so the buses are effectively isolated.

The -1 versions of the SN74LS640 thru SN74LS642, SN74LS644, and SN74LS645 are identical to the standard versions except that the recommended maximum I_{OL} is increased to 48 milliamperes. There are no -1 versions of the SN54LS640 thru SN54LS642, SN54LS644, and SN54LS645.

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PRICING/AVAILABILITY/PKG							▲Back to Top			REPORTED DISTRIBUTOR INVENTORY		
DEVICE INFORMATION							TI INVENTORY STATUS			AS OF 3:00 PM GMT, 26 Sep 2002		
ORDERABLE DEVICE	STATUS	PACKAGE TYPE PINS	TEMP (°C)	PRODUCT CONTENT	BUDGETARY PRICING QTY \$US	STD PACK QTY	IN STOCK	IN PROGRESS QTY DATE	LEAD TIME	DISTRIBUTOR COMPANY REGION	IN STOCK	PURCHASE
SN74LS641-1DW	ACTIVE	SOP (DW) 20	0 TO 70	View Contents	1KU 2.10	25	N/A*		12 WKS			
SN74LS641-1DWR	ACTIVE	SOP (DW) 20	0 TO 70	View Contents	1KU 2.13	2000	N/A*		12 WKS			
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SN74LS641DWR	ACTIVE	SOP (DW) 20	0 TO 70	View Contents	1KU 1.06	2000	N/A*		12 WKS			
SN74LS641N	ACTIVE	PDIP (N) 20	0 TO 70	View Contents	1KU 0.95	20	N/A*		12 WKS			
SN74LS641N3	OBSOLETE	PDIP (N) 20	0 TO 70	View Contents	1KU		N/A*		Not Available			
SN74LS641NSR	ACTIVE	SOP (NS) 20		View Contents	1KU 0.95	2000	N/A*		12 WKS			

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SN74LS640-1, OCTAL BUS TRANSCEIVER / IOL = 48 mA 3-STATE

DEVICE STATUS: **ACTIVE**

PARAMETER NAME	SN74LS640-1
Voltage Nodes (V)	5
Vcc range (V)	4.75 to 5.25
Input Level	TTL
Output Level	TTL
Output Drive (mA)	-15/48
No. of Outputs	8
Logic	Inv
Static Current	80
tpd max (ns)	15

FEATURES

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ORDERABLE DEVICE	STATUS	PACKAGE TYPE PINS	TEMP (°C)	PRODUCT CONTENT	BUDGETARY PRICING QTY \$US	STD PACK QTY	IN STOCK	IN PROGRESS QTY DATE	LEAD TIME	DISTRIBUTOR COMPANY REGION	IN STOCK	PURCHASE
SN74LS640-1DW	ACTIVE	SOP (DW) 20	0 TO 70	View Contents	1KU 2.10	25	N/A*	125 03 Oct	4 WKS			
SN74LS640-1DWR	OBSOLETE	SOP (DW) 20	0 TO 70	View Contents	1KU		N/A*		Not Available			
SN74LS640-1N	ACTIVE	PDIP (N) 20	0 TO 70	View Contents	1KU 2.10	20	N/A*	2780 03 Oct	4 WKS	Avnet AMERICA	711	BUY NOW
SN74LS640-1NSR	ACTIVE	SOP (NS) 20		View Contents	1KU 2.10	2000	N/A*		12 WKS			

Table Data Updated on: 9/26/2002



PRODUCT FOLDER | PRODUCT INFO: [FEATURES](#) | [DESCRIPTION](#) | [DATASHEETS](#) | [PRICING/AVAILABILITY/PKG](#) | [APPLICATION NOTES](#) | [RELATED DOCUMENTS](#)

PRODUCT SUPPORT: [TRAINING](#)

SN74LS642, Octal bus transceivers with open collector outputs

DEVICE STATUS: **ACTIVE**

PARAMETER NAME	SN74LS642	SN74LS642-1
Voltage Nodes (V)	5	5
Vcc range (V)	4.75 to 5.25	4.75 to 5.25
Input Level	TTL	TTL
Output Level	TTL	TTL
Output Drive (mA)	- /24	- /48
No. of Outputs	8	8
Logic	Inv	Inv
Static Current	80	80
tpd max (ns)	25	25

FEATURES

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- SN74LS64X-1 Versions Rated at I_{OL} of 48 mA
- Bi-directional Bus Transceivers in High-Density 20-Pin Packages
- Hysteresis at Bus Inputs Improves Noise Margins
- Choice of True or Inverting Logic
- Choice of 3-State or Open-Collector Outputs

DESCRIPTION

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These octal bus transceivers are designed for asynchronous two-way communication between data buses. The devices transmit data from the A bus to the B bus or from the B bus to the A bus depending upon the level at the direction control (DIR) input. The enable input (G_\) can be used to disable the device so the buses are effectively isolated.

The -1 versions of the SN74LS640 thru SN74LS642, SN74LS644, and SN74LS645 are identical to the standard versions except that the recommended maximum I_{OL} is increased to 48 milliamperes. There are no -1 versions of the SN54LS640 thru SN54LS642, SN54LS644, and SN54LS645.

The SN54LS640 thru SN54LS642, SN54LS644, and SN54LS645 are characterized for operation over the full military temperature range of -55°C to 125°C. The SN74LS640 thru SN74LS642, SN74LS644, and SN74LS645 are characterized for operation from 0°C to 70°C.

TECHNICAL DOCUMENTS

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To view the following documents, [Acrobat Reader 4.0](#) is required.

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Full datasheet in Acrobat PDF: [sn74ls642.pdf](#) (336 KB) (Updated: 03/01/1988)

APPLICATION NOTES

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- [Designing With Logic \(Rev. C\)](#) (SDYA009C - Updated: 06/01/1997)
- [Designing with the SN54/74LS123 \(Rev. A\)](#) (SDLA006A - Updated: 03/01/1997)
- [Evaluation of Nickel/Palladium/Gold-Finished Surface-Mount Integrated Circuits](#) (SZZA026 - Updated: 06/20/2001)
- [Input and Output Characteristics of Digital Integrated Circuits](#) (SDYA010 - Updated: 10/01/1996)
- [LVT-to-LVTH Conversion](#) (SCEA010 - Updated: 12/08/1998)
- [Live Insertion](#) (SDYA012 - Updated: 10/01/1996)
- [Logic Solutions For IEEE Std 1284](#) (SCEA013 - Updated: 06/01/1999)

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- [Logic Selection Guide Second Half 2002 \(Rev. R\)](#) (SDYU001R, 4274 KB - Updated: 07/19/2002)
- [Military Semiconductors Selection Guide 2002 \(Rev. B\)](#) (SGYC003B, 1648 KB - Updated: 04/22/2002)

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ORDERABLE DEVICE	STATUS	PACKAGE TYPE PINS	TEMP (°C)	PRODUCT CONTENT	BUDGETARY PRICING QTY \$US	STD PACK QTY	IN STOCK	IN PROGRESS QTY DATE	LEAD TIME	DISTRIBUTOR COMPANY REGION	IN STOCK	PURCHASE
SN74LS642-1DW	ACTIVE	SOP (DW) 20	0 TO 70	View Contents	1KU 3.15	25	N/A*		12 WKS			
SN74LS642-1N	ACTIVE	PDIP (N) 20	0 TO 70	View Contents	1KU 3.15	20	N/A*		12 WKS			
SN74LS642DW	ACTIVE	SOP (DW) 20	0 TO 70	View Contents	1KU 1.86	25	N/A*		12 WKS	Avnet AMERICA	357	BUY NOW
SN74LS642N	ACTIVE	PDIP (N) 20	0 TO 70	View Contents	1KU 1.86	20	N/A*		12 WKS			
SN74LS642NSR	ACTIVE	SOP (NS) 20		View Contents	1KU 1.86	2000	N/A*		12 WKS			

Table Data Updated on: 9/26/2002



PRODUCT FOLDER | PRODUCT INFO: [FEATURES](#) | [DESCRIPTION](#) | [DATASHEETS](#) | [PRICING/AVAILABILITY/PKG](#) | [APPLICATION NOTES](#) | [RELATED DOCUMENTS](#)

PRODUCT SUPPORT: [TRAINING](#)

SN74LS645, Octal bus transceivers

DEVICE STATUS: **ACTIVE**

PARAMETER NAME	SN54LS645	SN74LS645
Voltage Nodes (V)	5	5
Vcc range (V)	4.5 to 5.5	4.75 to 5.25
Input Level	TTL	TTL
Output Level	TTL	TTL
Output Drive (mA)		-15/24
No. of Outputs	8	8
Logic	True	True
Static Current		80
tpd max (ns)		15

FEATURES

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- SN74LS64X-1 Versions Rated at I_{OL} of 48 mA
- Bi-directional Bus Transceivers in High-Density 20-Pin Packages
- Hysteresis at Bus Inputs Improves Noise Margins
- Choice of True or Inverting Logic
- Choice of 3-State or Open-Collector Outputs

DESCRIPTION

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These octal bus transceivers are designed for asynchronous two-way communication between data buses. The devices transmit data from the A bus to the B bus or from the B bus to the A bus depending upon the level at the direction control (DIR) input. The enable input (G\) can be used to disable the device so the buses are effectively isolated.

The -1 versions of the SN74LS640 thru SN74LS642, SN74LS644, and SN74LS645 are identical to the standard versions except that the recommended maximum I_{OL} is increased to 48 milliamperes. There are no -1 versions of the SN54LS640 thru SN54LS642, SN54LS644, and SN54LS645.

The SN54LS640 thru SN54LS642, SN54LS644, and SN54LS645 are characterized for operation over the full military temperature range of -55°C to 125°C. The SN74LS640 thru SN74LS642, SN74LS644, and SN74LS645 are characterized for operation from 0°C to 70°C.

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- [Evaluation of Nickel/Palladium/Gold-Finished Surface-Mount Integrated Circuits](#) (SZZA026 - Updated: 06/20/2001)
- [Input and Output Characteristics of Digital Integrated Circuits](#) (SDYA010 - Updated: 10/01/1996)
- [LVT-to-LVTH Conversion](#) (SCEA010 - Updated: 12/08/1998)
- [Live Insertion](#) (SDYA012 - Updated: 10/01/1996)
- [Logic Solutions For IEEE Std 1284](#) (SCEA013 - Updated: 06/01/1999)

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- [Logic Selection Guide Second Half 2002 \(Rev. R\)](#) (SDYU001R, 4274 KB - Updated: 07/19/2002)
- [Military Semiconductors Selection Guide 2002 \(Rev. B\)](#) (SGYC003B, 1648 KB - Updated: 04/22/2002)

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TI INVENTORY STATUS
OF 3:00 PM GMT, 26 Sep 2002

IN STOCK	IN PROGRESS QTY DATE	LEAD TIME
<u>N/A*</u>	250 24 Sep	4 WKS
	4170 07 Oct	
	> 10k 14 Oct	
	871 21 Oct	
<u>N/A*</u>		Not Available
<u>N/A*</u>	4406 07 Oct	4 WKS
	> 10k 14 Oct	
	> 10k 21 Oct	
	720 02 Dec	
	200 04 Dec	
<u>N/A*</u>		Not Available

**REPORTED DISTRIBUTOR INVENTORY
AS OF 3:00 PM GMT, 26 Sep 2002**

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SN74LS645NSR	ACTIVE	SOP (NS) 20		View Contents	1KU 0.64	2000	N/A*	> 10k 14 Oct	4 WKS			
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Table Data Updated on: 9/26/2002



PRODUCT FOLDER | PRODUCT INFO: [FEATURES](#) | [DESCRIPTION](#) | [DATASHEETS](#) | [PRICING/AVAILABILITY/PKG](#) | [APPLICATION NOTES](#) | [RELATED DOCUMENTS](#)

PRODUCT SUPPORT: [TRAINING](#)

SN74LS645-1, OCTAL BUS TRANSCEIVER / IOL = 48 mA 3-STATE

DEVICE STATUS: **ACTIVE**

PARAMETER NAME	SN74LS645-1
Voltage Nodes (V)	5
Vcc range (V)	4.75 to 5.25
Input Level	TTL
Output Level	TTL
Output Drive (mA)	-15/48
No. of Outputs	8
Logic	True
Static Current	80
tpd max (ns)	15

FEATURES

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- SN74LS64X-1 Versions Rated at I_{OL} of 48 mA
- Bi-directional Bus Transceivers in High-Density 20-Pin Packages
- Hysteresis at Bus Inputs Improves Noise Margins
- Choice of True or Inverting Logic
- Choice of 3-State or Open-Collector Outputs

DESCRIPTION

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These octal bus transceivers are designed for asynchronous two-way communication between data buses. The devices transmit data from the A bus to the B bus or from the B bus to the A bus depending upon the level at the direction control (DIR) input. The enable input (G_\) can be used to disable the device so the buses are effectively isolated.

The -1 versions of the SN74LS640 thru SN74LS642, SN74LS644, and SN74LS645 are identical to the standard versions except that the recommended maximum I_{OL} is increased to 48 milliamperes. There are no -1 versions of the SN54LS640 thru SN54LS642, SN54LS644, and SN54LS645.

The SN54LS640 thru SN54LS642, SN54LS644, and SN54LS645 are characterized for operation over the full military temperature range of -55°C to 125°C. The SN74LS640 thru SN74LS642, SN74LS644, and SN74LS645 are characterized for operation from 0°C to 70°C.

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- [Evaluation of Nickel/Palladium/Gold-Finished Surface-Mount Integrated Circuits](#) (SZZA026 - Updated: 06/20/2001)
- [Input and Output Characteristics of Digital Integrated Circuits](#) (SDYA010 - Updated: 10/01/1996)
- [LVT-to-LVTH Conversion](#) (SCEA010 - Updated: 12/08/1998)
- [Live Insertion](#) (SDYA012 - Updated: 10/01/1996)
- [Logic Solutions For IEEE Std 1284](#) (SCEA013 - Updated: 06/01/1999)

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- [Logic Selection Guide Second Half 2002 \(Rev. R\)](#) (SDYU001R, 4274 KB - Updated: 07/19/2002)
- [Military Semiconductors Selection Guide 2002 \(Rev. B\)](#) (SGYC003B, 1648 KB - Updated: 04/22/2002)

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DEVICE INFORMATION							TI INVENTORY STATUS			AS OF 3:00 PM GMT, 26 Sep 2002		
ORDERABLE DEVICE	STATUS	PACKAGE TYPE PINS	TEMP (°C)	PRODUCT CONTENT	BUDGETARY PRICING QTY \$US	STD PACK QTY	IN STOCK	IN PROGRESS QTY DATE	LEAD TIME	DISTRIBUTOR COMPANY REGION	IN STOCK	PURCHASE
SN74LS645-1DW	ACTIVE	SOP (DW) 20	0 TO 70	View Contents	1KU 2.10	25	N/A*	800 03 Oct	4 WKS			
								4420 07 Oct				
								>10k 14 Oct				
								871 21 Oct				
SN74LS645-1DWR	ACTIVE	SOP (DW) 20	0 TO 70	View Contents	1KU 2.13	2000	N/A*	4405 07 Oct	4 WKS			
								>10k 14 Oct				
SN74LS645-1N	ACTIVE	PDIP (N) 20	0 TO 70	View Contents	1KU 2.10	20	N/A*	622 24 Sep	4 WKS	Avnet AMERICA	>1k	BUY NOW
								3606 07 Oct				
								>10k 14 Oct				
								178 15 Oct				
								>10k 21 Oct				
SN74LS645-1N3	OBSOLETE	PDIP (N) 20	0 TO 70	View Contents	1KU		N/A*		Not Available			

SN74LS645-1NSR	ACTIVE	SOP (NS) 20		View Contents	1KU 2.10	2000	N/A*	1416 23 Sep	4 WKS			
								>10k 14 Oct				

Table Data Updated on: 9/26/2002



PRODUCT FOLDER | PRODUCT INFO: [FEATURES](#) | [DESCRIPTION](#) | [DATASHEETS](#) | [PRICING/AVAILABILITY/PKG](#) | [APPLICATION NOTES](#) | [RELATED DOCUMENTS](#)

PRODUCT SUPPORT: [TRAINING](#)

SN74LS640, Octal bus transceivers

DEVICE STATUS: **ACTIVE**

PARAMETER NAME	SN54LS640	SN74LS640
Voltage Nodes (V)	5	5
Vcc range (V)	4.5 to 5.5	4.75 to 5.25
Input Level	TTL	TTL
Output Level	TTL	TTL
Output Drive (mA)		-15/24
No. of Outputs	8	8
Logic	Inv	Inv
Static Current		80
tpd max (ns)		15

FEATURES

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- SN74LS64X-1 Versions Rated at I_{OL} of 48 mA
- Bi-directional Bus Transceivers in High-Density 20-Pin Packages
- Hysteresis at Bus Inputs Improves Noise Margins
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DESCRIPTION

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The SN54LS640 thru SN54LS642, SN54LS644, and SN54LS645 are characterized for operation over the full military temperature range of -55°C to 125°C. The SN74LS640 thru SN74LS642, SN74LS644, and SN74LS645 are characterized for operation from 0°C to 70°C.

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- [Designing with the SN54/74LS123 \(Rev. A\)](#) (SDLA006A - Updated: 03/01/1997)
- [Evaluation of Nickel/Palladium/Gold-Finished Surface-Mount Integrated Circuits](#) (SZZA026 - Updated: 06/20/2001)
- [Input and Output Characteristics of Digital Integrated Circuits](#) (SDYA010 - Updated: 10/01/1996)
- [LVT-to-LVTH Conversion](#) (SCEA010 - Updated: 12/08/1998)
- [Live Insertion](#) (SDYA012 - Updated: 10/01/1996)
- [Logic Solutions For IEEE Std 1284](#) (SCEA013 - Updated: 06/01/1999)

- [Logic Reference Guide](#) (SCYB004, 1032 KB - Updated: 10/23/2001)
- [Logic Selection Guide Second Half 2002 \(Rev. R\)](#) (SDYU001R, 4274 KB - Updated: 07/19/2002)
- [Military Semiconductors Selection Guide 2002 \(Rev. B\)](#) (SGYC003B, 1648 KB - Updated: 04/22/2002)

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ORDERABLE DEVICE	STATUS	PACKAGE TYPE PINS	TEMP (°C)	PRODUCT CONTENT	BUDGETARY PRICING QTY \$US	STD PACK QTY	IN STOCK	IN PROGRESS QTY DATE	LEAD TIME	DISTRIBUTOR COMPANY REGION	IN STOCK	PURCHASE
SN74LS640DW	ACTIVE	SOP (DW) 20	0 TO 70	View Contents	1KU 0.99	25	N/A*	1813 24 Sep	4 WKS	Avnet AMERICA	130	BUY NOW
								1209 03 Oct				
SN74LS640DWR	ACTIVE	SOP (DW) 20	0 TO 70	View Contents	1KU 1.02	2000	N/A*		12 WKS			
SN74LS640N	ACTIVE	PDIP (N) 20	0 TO 70	View Contents	1KU 0.91	20	N/A*	220 03 Oct	12 WKS	Avnet AMERICA	> 1k	BUY NOW
SN74LS640N3	OBSOLETE	PDIP (N) 20	0 TO 70	View Contents	1KU		N/A*		Not Available			
SN74LS640NSR	ACTIVE	SOP (NS) 20		View Contents	1KU 0.91	2000	N/A*		12 WKS			

Table Data Updated on: 9/26/2002