

## N-channel 600 V, 0.186 $\Omega$ typ., 18 A MDmesh™ M2 Power MOSFET in a PowerFLAT™ 8x8 HV package

Datasheet - production data

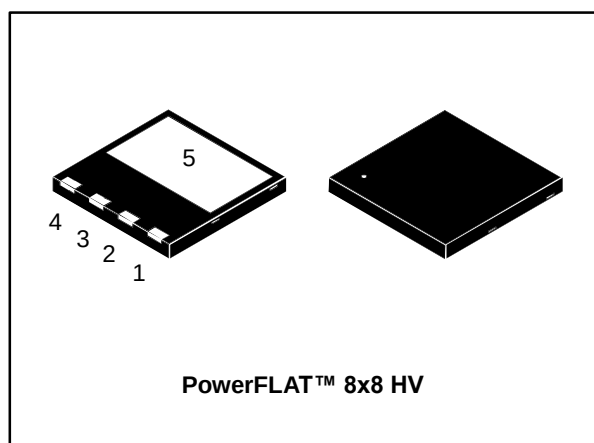
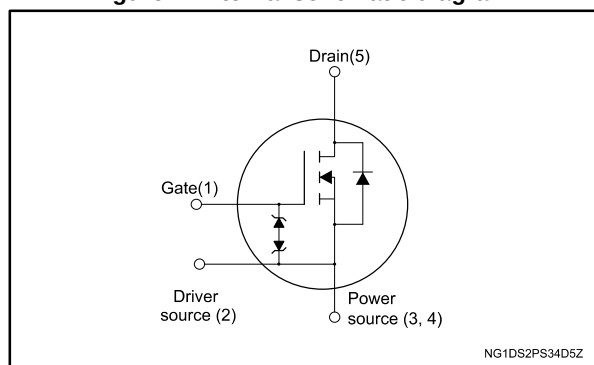


Figure 1: Internal schematic diagram



### Features

| Order code | V <sub>DS@T<sub>J</sub> max</sub> | R <sub>DS(on)</sub> max. | I <sub>D</sub> |
|------------|-----------------------------------|--------------------------|----------------|
| STL24N60M2 | 650 V                             | 0.210 $\Omega$           | 18 A           |

- Extremely low gate charge
- Excellent output capacitance (C<sub>oss</sub>) profile
- 100% avalanche tested
- Zener-protected

### Applications

- Switching applications

### Description

This device is an N-channel Power MOSFET developed using MDmesh™ M2 technology. Thanks to its strip layout and an improved vertical structure, the device exhibits low on-resistance and optimized switching characteristics, rendering it suitable for the most demanding high efficiency converters.

Table 1: Device summary

| Order code | Marking | Package           | Packing       |
|------------|---------|-------------------|---------------|
| STL24N60M2 | 24N60M2 | PowerFLAT™ 8x8 HV | Tape and reel |

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## Contents

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# 1 Electrical ratings

Table 2: Absolute maximum ratings

| Symbol            | Parameter                                                       | Value      | Unit             |
|-------------------|-----------------------------------------------------------------|------------|------------------|
| $V_{GS}$          | Gate-source voltage                                             | $\pm 25$   | V                |
| $I_D^{(1)}$       | Drain current (continuous) at $T_C = 25\text{ }^\circ\text{C}$  | 18         | A                |
| $I_D^{(1)}$       | Drain current (continuous) at $T_C = 100\text{ }^\circ\text{C}$ | 12         | A                |
| $I_{DM}^{(1)(2)}$ | Drain current (pulsed)                                          | 72         | A                |
| $P_{TOT}^{(1)}$   | Total dissipation at $T_C = 25\text{ }^\circ\text{C}$           | 125        | W                |
| $dv/dt^{(3)}$     | Peak diode recovery voltage slope                               | 15         | V/ns             |
| $dv/dt^{(4)}$     | MOSFET $dv/dt$ ruggedness                                       | 50         | V/ns             |
| $T_{stg}$         | Storage temperature range                                       | -55 to 150 | $^\circ\text{C}$ |
| $T_j$             | Operating junction temperature range                            |            |                  |

**Notes:**

<sup>(1)</sup>the value is limited by package

<sup>(2)</sup>Pulse width limited by safe operating area.

<sup>(3)</sup> $I_{SD} \leq 18\text{ A}$ ,  $di/dt \leq 400\text{ A}/\mu\text{s}$ ;  $V_{DS(peak)} < V_{(BR)DSS}$ ,  $V_{DD} = 400\text{ V}$ .

<sup>(4)</sup> $V_{DS} \leq 480\text{ V}$

Table 3: Thermal data

| Symbol              | Parameter                            | Value | Unit                      |
|---------------------|--------------------------------------|-------|---------------------------|
| $R_{thj-case}$      | Thermal resistance junction-case max | 1     | $^\circ\text{C}/\text{W}$ |
| $R_{thj-pcb}^{(1)}$ | Thermal resistance junction-pcb max  | 45    | $^\circ\text{C}/\text{W}$ |

**Notes:**

<sup>(1)</sup>When mounted on FR-4 board of  $\text{inch}^2$ , 2oz Cu.

Table 4: Avalanche characteristics

| Symbol   | Parameter                                                                                                            | Value | Unit |
|----------|----------------------------------------------------------------------------------------------------------------------|-------|------|
| $I_{AR}$ | Avalanche current, repetitive or not repetitive (pulse width limited by $T_{Jmax}$ )                                 | 3.5   | A    |
| $E_{AS}$ | Single pulse avalanche energy (starting $T_j = 25\text{ }^\circ\text{C}$ , $I_D = I_{AR}$ ; $V_{DD} = 50\text{ V}$ ) | 180   | mJ   |

## 2 Electrical characteristics

$T_C = 25\text{ }^{\circ}\text{C}$  unless otherwise specified

**Table 5: On/off states**

| Symbol        | Parameter                         | Test conditions                                                                                         | Min. | Typ.  | Max.     | Unit          |
|---------------|-----------------------------------|---------------------------------------------------------------------------------------------------------|------|-------|----------|---------------|
| $V_{(BR)DSS}$ | Drain-source breakdown voltage    | $V_{GS} = 0\text{ V}$ , $I_D = 1\text{ mA}$                                                             | 600  |       |          | V             |
| $I_{DSS}$     | Zero gate voltage Drain current   | $V_{GS} = 0\text{ V}$ , $V_{DS} = 600\text{ V}$                                                         |      |       | 1        | $\mu\text{A}$ |
|               |                                   | $V_{GS} = 0\text{ V}$ , $V_{DS} = 600\text{ V}$ ,<br>$T_C = 125\text{ }^{\circ}\text{C}$ <sup>(1)</sup> |      |       | 100      | $\mu\text{A}$ |
| $I_{GSS}$     | Gate-body leakage current         | $V_{DS} = 0\text{ V}$ , $V_{GS} = \pm 25\text{ V}$                                                      |      |       | $\pm 10$ | $\mu\text{A}$ |
| $V_{GS(th)}$  | Gate threshold voltage            | $V_{DS} = V_{GS}$ , $I_D = 250\text{ }\mu\text{A}$                                                      | 2    | 3     | 4        | V             |
| $R_{DS(on)}$  | Static drain-source on-resistance | $V_{GS} = 10\text{ V}$ , $I_D = 9\text{ A}$                                                             |      | 0.186 | 0.210    | $\Omega$      |

**Notes:**

<sup>(1)</sup>Defined by design, not subject to production test.

**Table 6: Dynamic**

| Symbol                     | Parameter                     | Test conditions                                                                                                                        | Min. | Typ. | Max. | Unit     |
|----------------------------|-------------------------------|----------------------------------------------------------------------------------------------------------------------------------------|------|------|------|----------|
| $C_{iss}$                  | Input capacitance             | $V_{DS} = 100\text{ V}$ , $f = 1\text{ MHz}$ , $V_{GS} = 0\text{ V}$                                                                   | -    | 1060 | -    | pF       |
| $C_{oss}$                  | Output capacitance            |                                                                                                                                        | -    | 55   | -    | pF       |
| $C_{rss}$                  | Reverse transfer capacitance  |                                                                                                                                        | -    | 2.2  | -    | pF       |
| $C_{oss\text{ eq.}}^{(1)}$ | Equivalent output capacitance | $V_{DS} = 0\text{ to }480\text{ V}$ , $V_{GS} = 0\text{ V}$                                                                            | -    | 258  | -    | pF       |
| $R_G$                      | Intrinsic gate resistance     | $f = 1\text{ MHz}$ open drain                                                                                                          | -    | 7    | -    | $\Omega$ |
| $Q_g$                      | Total gate charge             | $V_{DD} = 480\text{ V}$ , $I_D = 18\text{ A}$ , $V_{GS} = 10\text{ V}$<br>(see <a href="#">Figure 15: "Gate charge test circuit"</a> ) | -    | 29   | -    | nC       |
| $Q_{gs}$                   | Gate-source charge            |                                                                                                                                        | -    | 6    | -    | nC       |
| $Q_{gd}$                   | Gate-drain charge             |                                                                                                                                        | -    | 12   | -    | nC       |

**Notes:**

<sup>(1)</sup> $C_{oss\text{ eq.}}$  is defined as a constant equivalent capacitance giving the same charging time as  $C_{oss}$  when  $V_{DS}$  increases from 0 to 80%  $V_{DSS}$

**Table 7: Switching times**

| Symbol       | Parameter           | Test conditions                                                                                                                                                                                                                                       | Min. | Typ. | Max. | Unit |
|--------------|---------------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|------|------|------|------|
| $t_{d(on)}$  | Turn-on delay time  | $V_{DD} = 300\text{ V}$ , $I_D = 9\text{ A}$ , $R_G = 4.7\text{ }\Omega$ ,<br>$V_{GS} = 10\text{ V}$ (see <a href="#">Figure 14: "Switching times test circuit for resistive load"</a> ) and ( <a href="#">Figure 19: "Switching time waveform"</a> ) | -    | 14   | -    | ns   |
| $t_r$        | Rise time           |                                                                                                                                                                                                                                                       | -    | 9    | -    | ns   |
| $t_{d(off)}$ | Turn-off delay time |                                                                                                                                                                                                                                                       | -    | 60   | -    | ns   |
| $t_f$        | Fall time           |                                                                                                                                                                                                                                                       | -    | 15   | -    | ns   |

Table 8: Source drain diode

| Symbol             | Parameter                     | Test conditions                                                                                                                                                                                                                       | Min. | Typ. | Max. | Unit          |
|--------------------|-------------------------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|------|------|------|---------------|
| $I_{SD}^{(1)}$     | Source-drain current          |                                                                                                                                                                                                                                       | -    |      | 18   | A             |
| $I_{SDM}^{(1)(2)}$ | Source-drain current (pulsed) |                                                                                                                                                                                                                                       | -    |      | 72   | A             |
| $V_{SD}^{(3)}$     | Forward on voltage            | $V_{GS} = 0\text{ V}$ , $I_{SD} = 18\text{ A}$                                                                                                                                                                                        | -    |      | 1.6  | V             |
| $t_{rr}$           | Reverse recovery time         | $I_{SD} = 18\text{ A}$ , $di/dt = 100\text{ A}/\mu\text{s}$ ,<br>$V_{DD} = 60\text{ V}$ (see <a href="#">Figure 16: "Test circuit for inductive load switching and diode recovery times"</a> )                                        | -    | 332  |      | ns            |
| $Q_{rr}$           | Reverse recovery charge       |                                                                                                                                                                                                                                       | -    | 4    |      | $\mu\text{C}$ |
| $I_{RRM}$          | Reverse recovery current      |                                                                                                                                                                                                                                       | -    | 24   |      | A             |
| $t_{rr}$           | Reverse recovery time         | $I_{SD} = 18\text{ A}$ , $di/dt = 100\text{ A}/\mu\text{s}$ ,<br>$V_{DD} = 60\text{ V}$ , $T_J = 150\text{ }^\circ\text{C}$<br>(see <a href="#">Figure 16: "Test circuit for inductive load switching and diode recovery times"</a> ) | -    | 450  |      | ns            |
| $Q_{rr}$           | Reverse recovery charge       |                                                                                                                                                                                                                                       | -    | 5.5  |      | $\mu\text{C}$ |
| $I_{RRM}$          | Reverse recovery current      |                                                                                                                                                                                                                                       | -    | 25   |      | A             |

**Notes:**

<sup>(1)</sup>The value is limited by package.

<sup>(2)</sup>Pulse width is limited by safe operating area

<sup>(3)</sup>Pulsed: pulse duration = 300  $\mu\text{s}$ , duty cycle 1.5%

## 2.1 Electrical characteristics (curves)

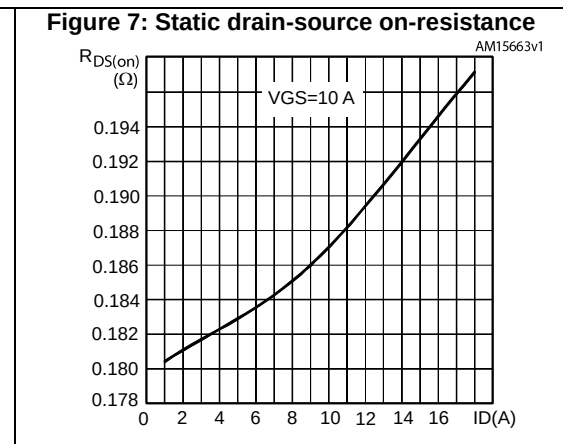
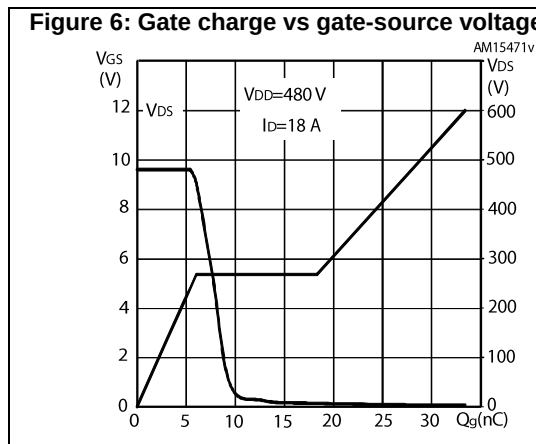
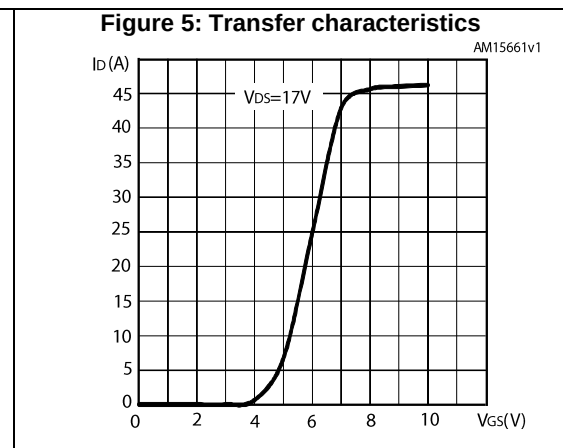
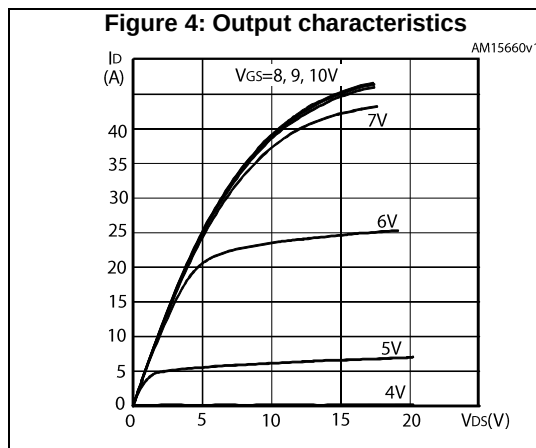
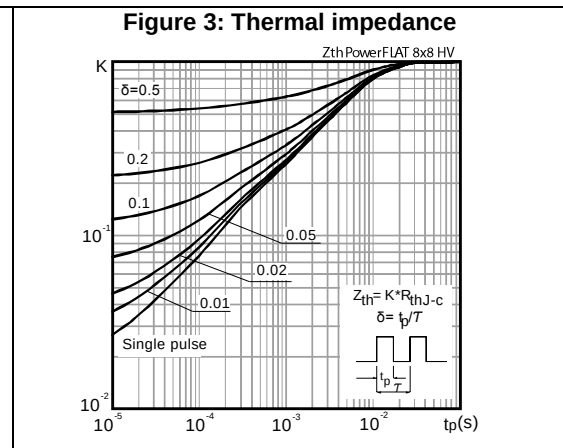
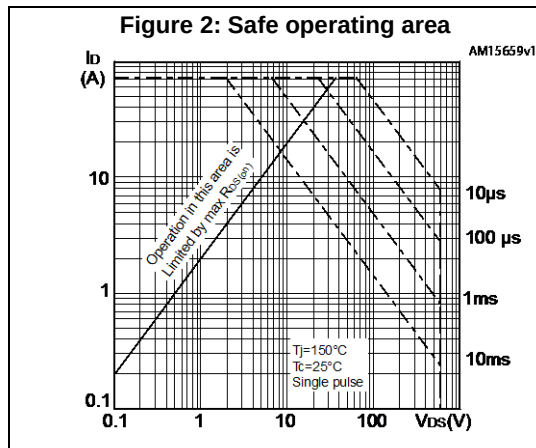


Figure 8: Capacitance variations

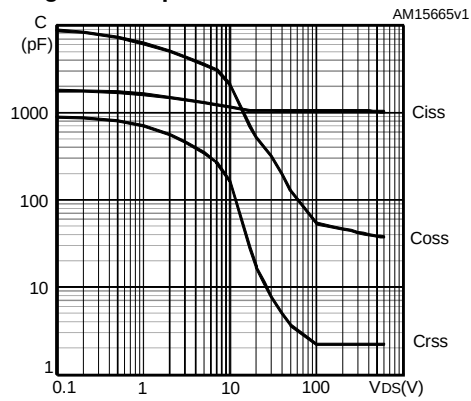


Figure 9: Normalized gate threshold voltage vs temperature

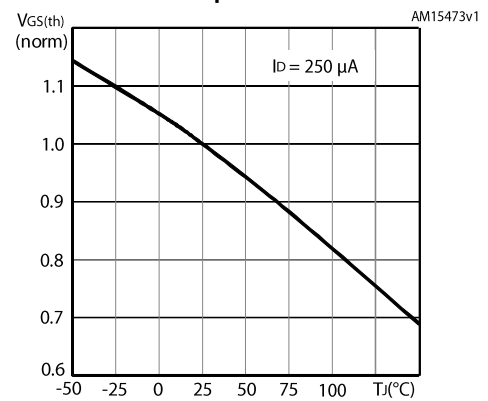


Figure 10: Normalized on-resistance vs temperature

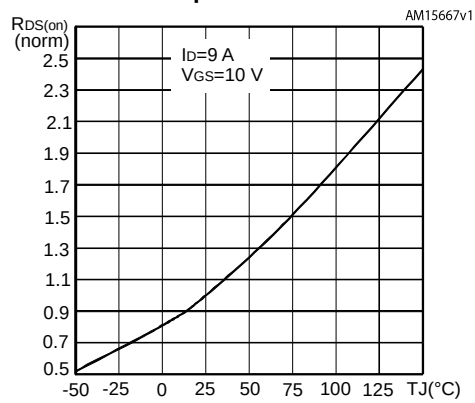


Figure 11: Normalized V(BR)DSS vs temperature

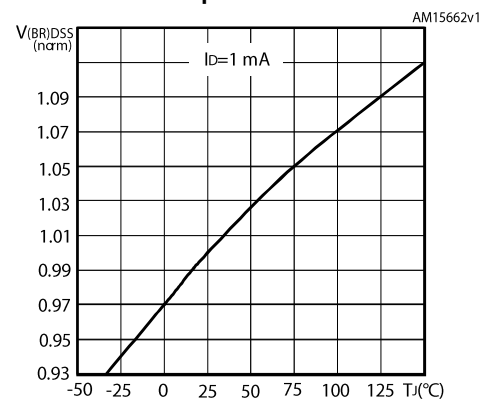


Figure 12: Output capacitance stored energy

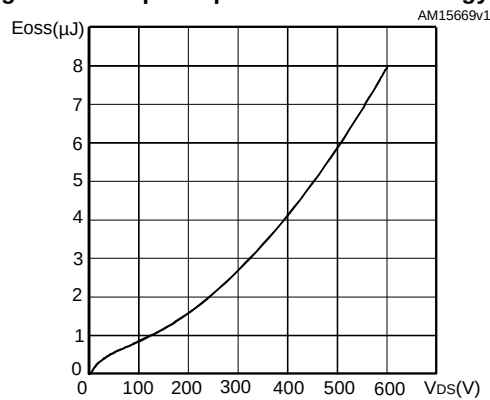
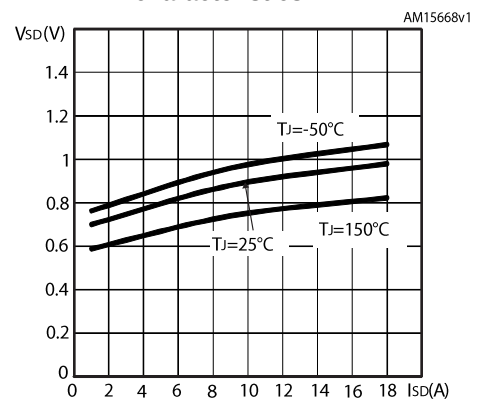
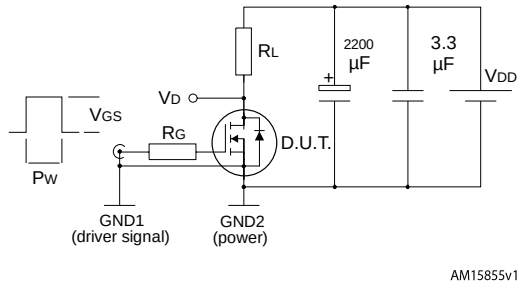


Figure 13: Source-drain diode forward characteristics

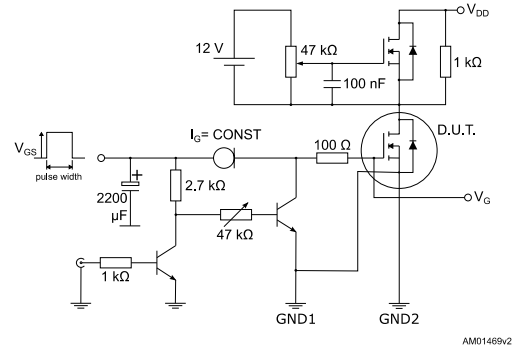


### 3 Test circuits

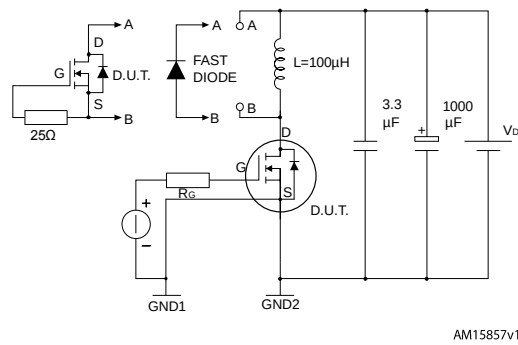
**Figure 14: Switching times test circuit for resistive load**



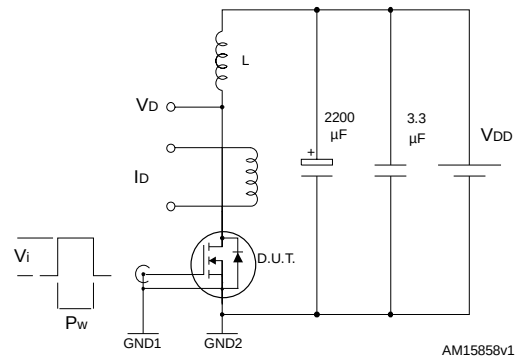
**Figure 15: Gate charge test circuit**



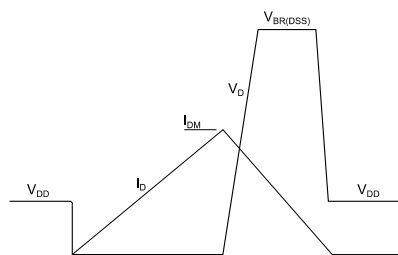
**Figure 16: Test circuit for inductive load switching and diode recovery times**



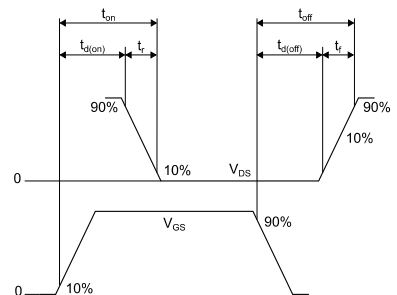
**Figure 17: Unclamped inductive load test circuit**



**Figure 18: Unclamped inductive waveform**



**Figure 19: Switching time waveform**





## 4 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: **[www.st.com](http://www.st.com)**. ECOPACK® is an ST trademark.

## 4.1 PowerFLAT™ 8x8 HV package information

Figure 20: PowerFLAT™ 8x8 HV package outline

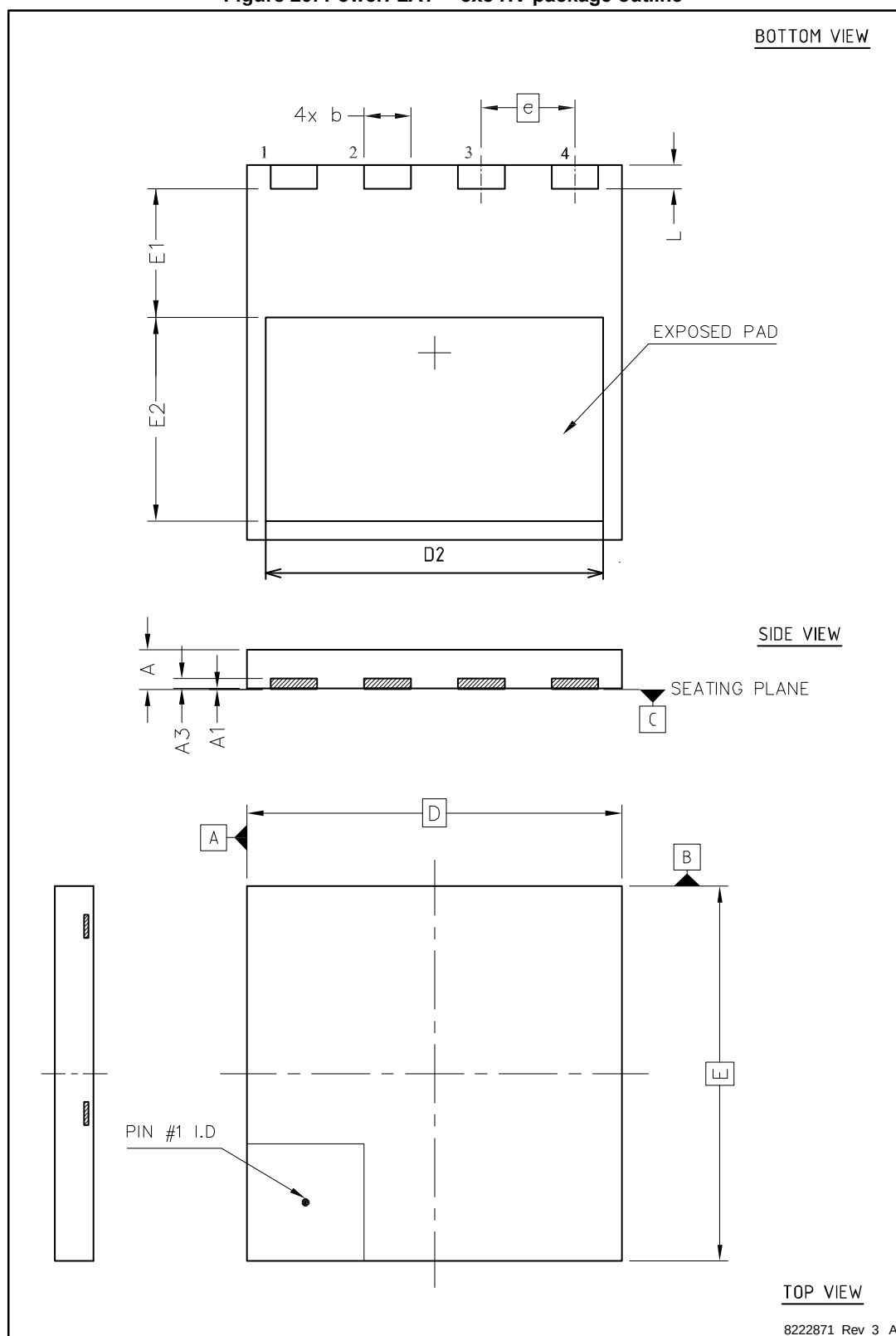
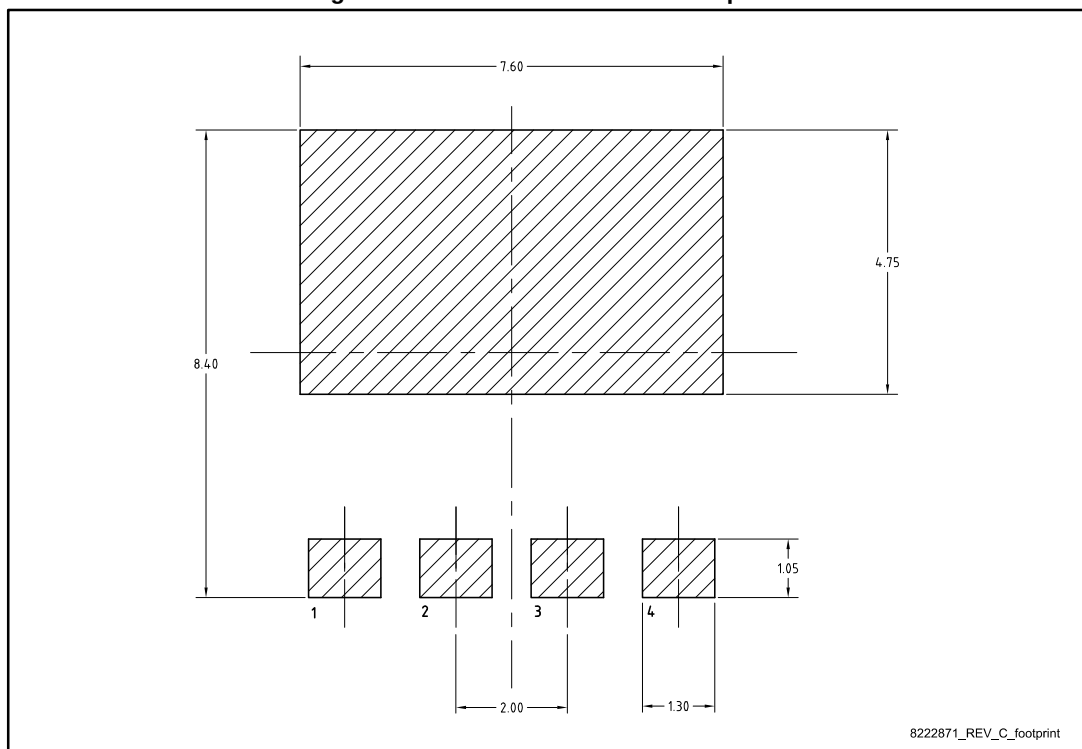


Table 9: PowerFLAT™ 8x8 HV mechanical data

| Dim. | mm   |      |      |
|------|------|------|------|
|      | Min. | Typ. | Max. |
| A    | 0.75 | 0.85 | 0.95 |
| A1   | 0.00 |      | 0.05 |
| A3   | 0.10 | 0.20 | 0.30 |
| b    | 0.90 | 1.00 | 1.10 |
| D    | 7.90 | 8.00 | 8.10 |
| E    | 7.90 | 8.00 | 8.10 |
| D2   | 7.10 | 7.20 | 7.30 |
| E1   | 2.65 | 2.75 | 2.85 |
| E2   | 4.25 | 4.35 | 4.45 |
| e    |      | 2.00 |      |
| L    | 0.40 | 0.50 | 0.60 |

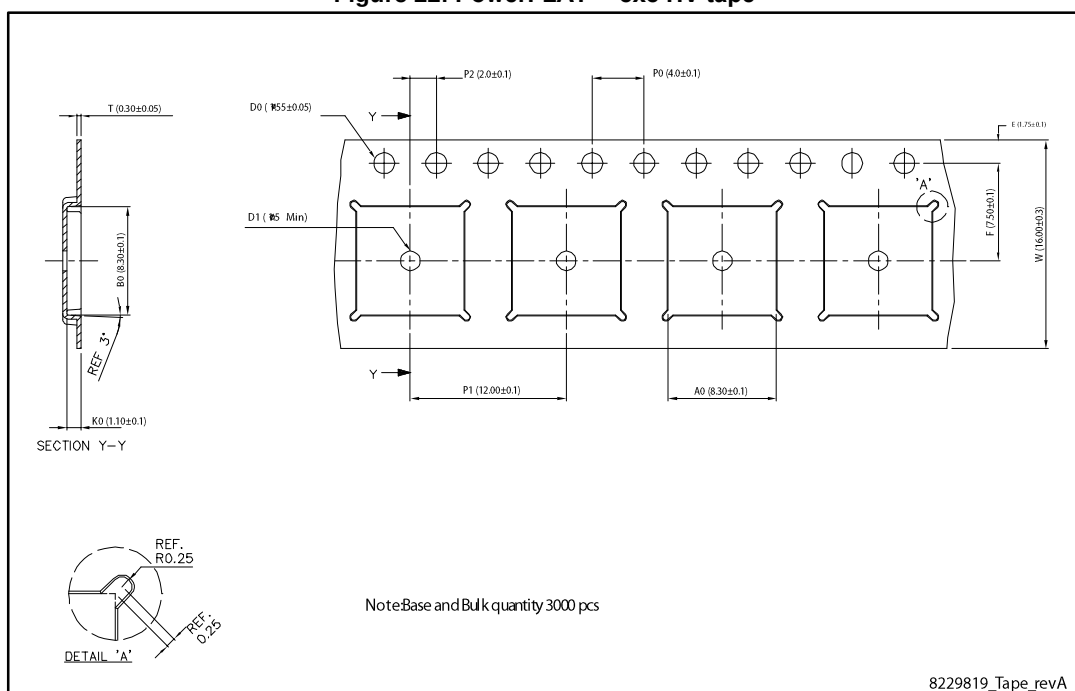
Figure 21: PowerFLAT™ 8x8 HV footprint



All dimensions are in millimeters.

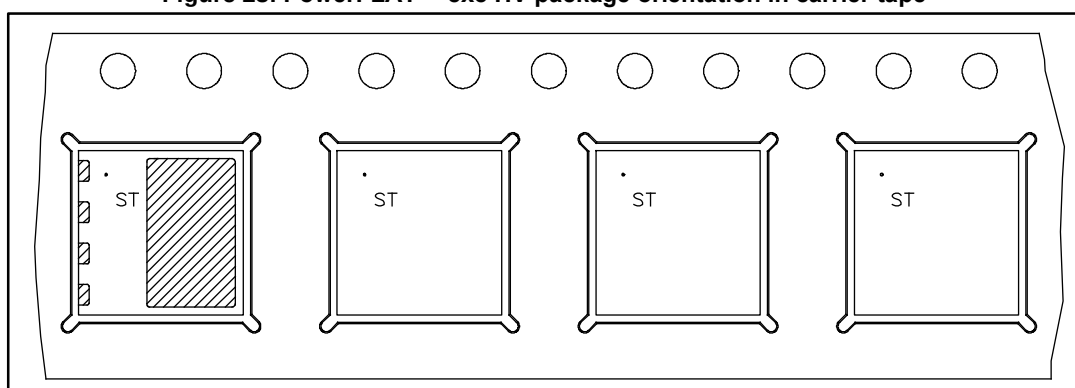
## 4.2 PowerFLAT™ 8x8 HV packing information

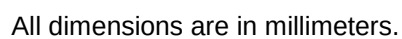
Figure 22: PowerFLAT™ 8x8 HV tape



All dimensions are in millimeters.

Figure 23: PowerFLAT™ 8x8 HV package orientation in carrier tape



[illegible]

## 5 Revision history

Table 10: Document revision history

| Date        | Revision | Changes                                                                                                                                                                                                                                                                                           |
|-------------|----------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 11-Jun-2013 | 1        | First release.                                                                                                                                                                                                                                                                                    |
| 28-Feb-2014 | 2        | Modified: $I_D$ (at $T_C = 100\text{ °C}$ ) value in Table 3.<br>Modified: $V_{SD}$ max value, figures 3 and 11.<br>Updated: Section 4: Package mechanical data – Minor text changes.                                                                                                             |
| 25-May-2016 | 3        | Updated features and description in cover page.<br>Updated package silhouette and <a href="#">Figure 1: "Internal schematic diagram"</a> .<br>Updated <a href="#">Section 4: "Test circuits"</a> and <a href="#">Section 5.1: "PowerFLAT™ 8x8 HV package information"</a> .<br>Minor text changes |

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