

Features

- High Speed
 - 25 ns
- CMOS for Optimum Speed and Power
- Low Active Power
 - 385 mW
- Low Standby Power
 - 110 mW
- TTL Compatible Inputs and Outputs
- Automatic Power Down when Deselected
- Available in Pb-free 22-Pin (300-Mil) Molded DIP

Functional Description

The CY7C187 is a high performance CMOS static RAM organized as 65,536 words x 1 bit. Easy memory expansion is provided by an active LOW Chip Enable ($\overline{CE}$) and tristate drivers. The CY7C187 has an automatic power down feature, reducing the power consumption by 56% when deselected.

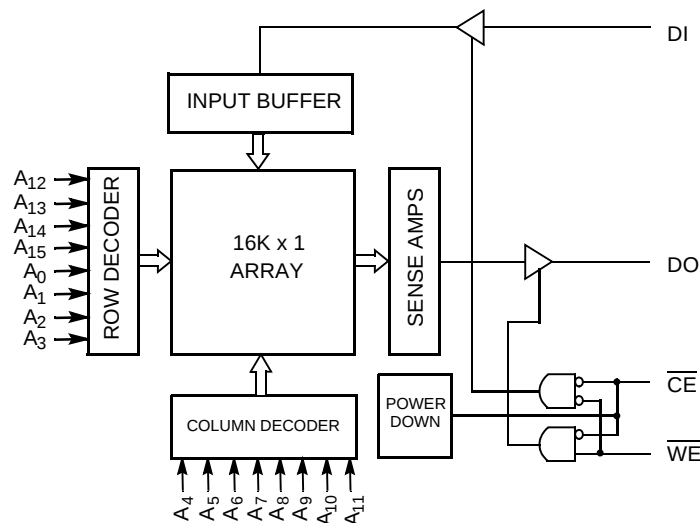
Writing to the device is possible when the Chip Enable ($\overline{CE}$) and Write Enable ($\overline{WE}$) inputs are both LOW. Data on the input pin (D_{IN}) is written into the memory location specified on the address pins (A_0 through A_{15}).

Reading the device is possible by taking the Chip Enable ($\overline{CE}$) LOW, while Write Enable ($\overline{WE}$) remains HIGH. Under these conditions, the contents of the memory location specified on the address pin appears on the data output (D_{OUT}) pin.

The output pin stays in high impedance state when $\overline{CE}$ is HIGH or $\overline{WE}$ is LOW.

The CY7C187 uses a die coat to insure alpha immunity.

Logic Block Diagram

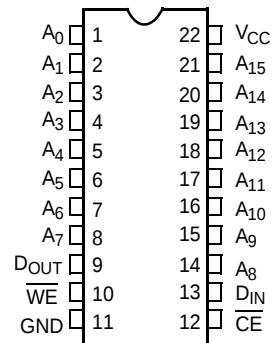


Selection Guide

Description	-25	-35
Maximum Access Time (ns)	25	35
Maximum Operating Current (mA)	70	70
Maximum CMOS Standby Current (mA)	20	20

Pin Configuration

Figure 1. Pin Diagram DIP - Top View



Maximum Ratings

Exceeding the maximum ratings may impair the useful life of the device. User guidelines are not tested.

Storage Temperature -65°C to $+150^{\circ}\text{C}$

Ambient Temperature with
Power Applied -55°C to $+125^{\circ}\text{C}$

Supply Voltage to Ground Potential
(Pin 22 to Pin 11) -0.5V to $+7.0\text{V}$

DC Voltage Applied to Outputs
in High Z State^[1] -0.5V to $+7.0\text{V}$

DC Input Voltage^[1] -0.5V to $+7.0\text{V}$

Output Current into Outputs (LOW) 20 mA

Static Discharge Voltage $>2001\text{V}$
(per MIL-STD-883, Method 3015)

Latch Up Current $>200\text{ mA}$

Operating Range

Range	Ambient Temperature	V _{CC}
Commercial	0°C to $+70^{\circ}\text{C}$	$5\text{V} \pm 10\%$

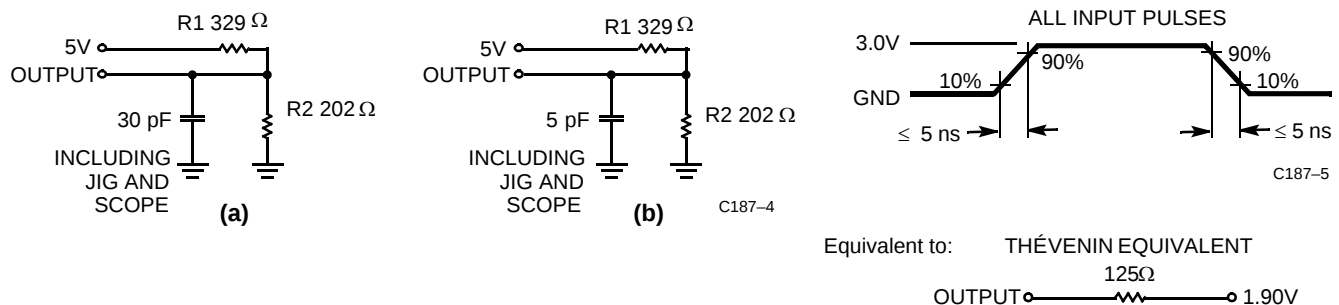
Electrical Characteristics Over the Operating Range

Parameter	Description	Test Conditions	-25 and -35		Unit
			Min	Max	
V _{OH}	Output HIGH Voltage	V _{CC} = Min., I _{OH} = -4.0 mA	2.4		V
V _{OL}	Output LOW Voltage	V _{CC} = Min., I _{OL} = 12.0 mA		0.4	V
V _{IH}	Input HIGH Voltage		2.2	V _{CC}	V
V _{IL}	Input LOW Voltage ^[1]		-0.5	0.8	V
I _{IX}	Input Leakage Current	$\text{GND} \leq V_I \leq V_{CC}$	-5	$+5$	μA
I _{OZ}	Output Leakage Current	$\text{GND} \leq V_O \leq V_{CC}$, Output Disabled	-5	$+5$	μA
I _{CC}	V _{CC} Operating Supply Current	V _{CC} = Max., I _{OUT} = 0 mA		70	mA
I _{SB1}	Automatic $\overline{\text{CE}}$ Power Down Current ^[3]	Max. V _{CC} , $\overline{\text{CE}} \geq V_{IH}$		20	mA
I _{SB2}	Automatic $\overline{\text{C}}$ Power Down Current	Max. V _{CC} , $\overline{\text{CE}} \geq V_{CC} - 0.3\text{V}$, V _{IN} $\geq V_{CC} - 0.3\text{V}$ or V _{IN} $\leq 0.3\text{V}$		20	mA

Capacitance^[4]

Parameter	Description	Test Conditions	Max	Unit
C _{IN}	Input Capacitance	T _A = 25°C , f = 1 MHz, V _{CC} = 5.0V	10	pF
C _{OUT}	Output Capacitance		10	pF

Figure 2. AC Test Loads and Waveforms

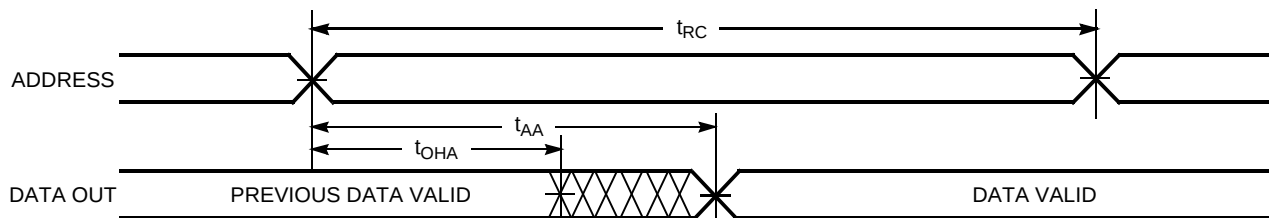


Notes

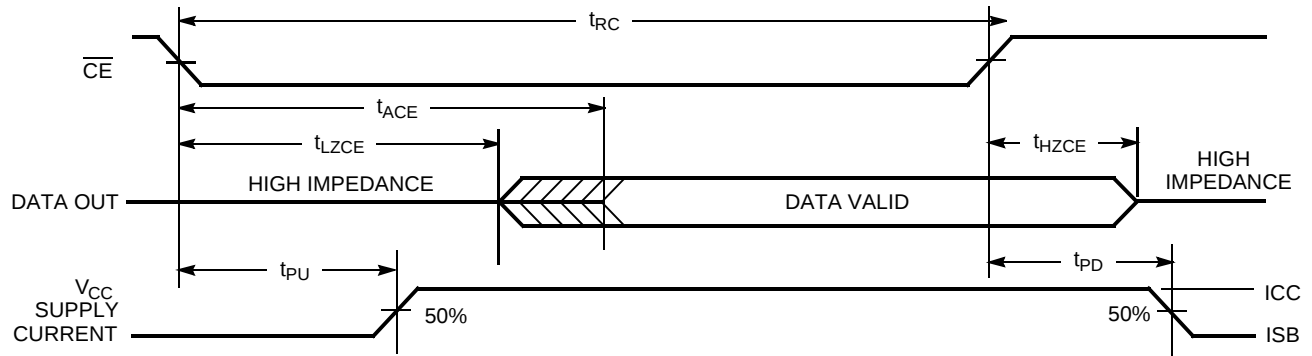
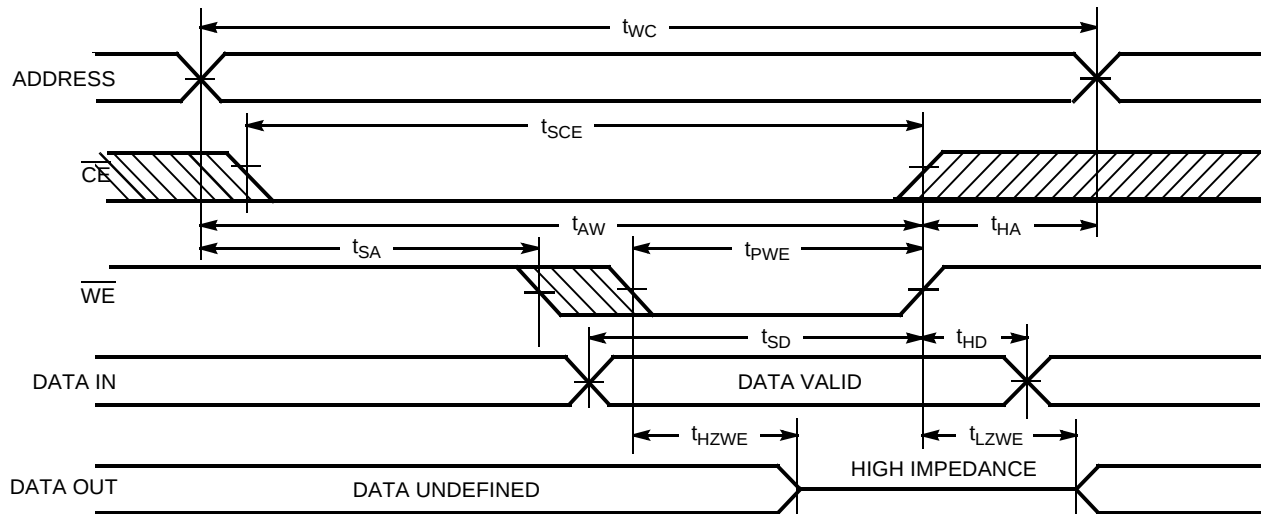
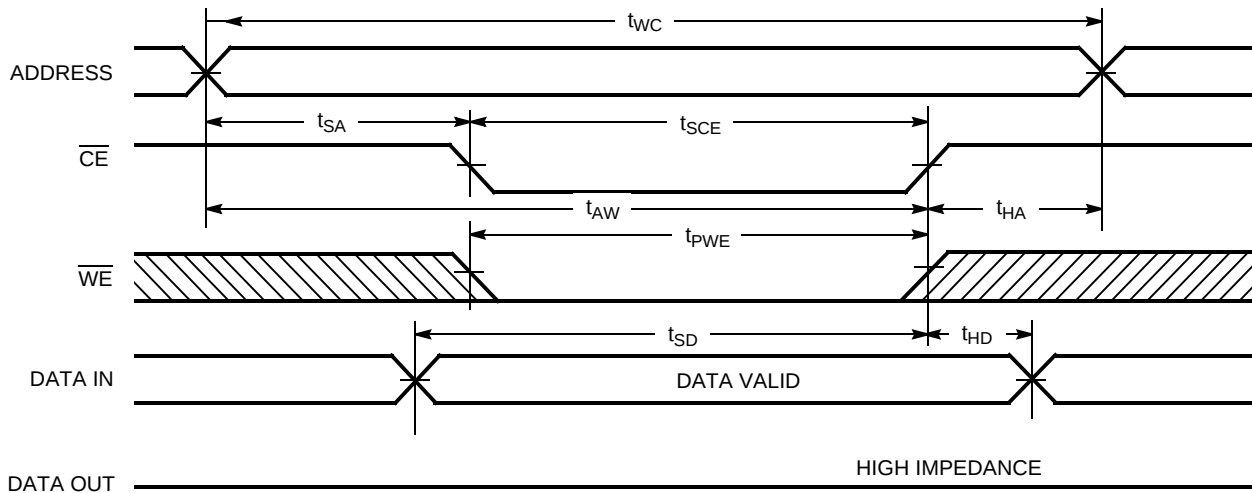
1. V_{IL} (min.) = -3.0V for pulse durations less than 30 ns.
2. Not more than one output should be shorted at one time. Duration of the short circuit should not exceed 30 seconds.
3. A pull up resistor to V_{CC} on the $\overline{\text{CE}}$ input is required to keep the device deselected during V_{CC} power up, otherwise I_{SB} exceeds values given.
4. Tested initially and after any design or process changes that may affect these parameters.

Switching Characteristics Over the Operating Range^[5]

Parameter	Description	-25		-35		Unit
		Min	Max	Min	Max	
Read Cycle						
t _{RC}	Read Cycle Time	25		35		ns
t _{AA}	Address to Data Valid		25		35	ns
t _{OHA}	Output Hold from Address Change	5		5		ns
t _{ACE}	$\overline{CE}$ LOW to Data Valid		25		35	ns
t _{LZCE}	$\overline{CE}$ LOW to Low Z ^[6]	5		5		ns
t _{HZCE}	$\overline{CE}$ HIGH to High Z ^[6,7]		10		15	ns
t _{PU}	$\overline{CE}$ LOW to Power Up	0		0		ns
t _{PD}	$\overline{CE}$ HIGH to Power Down		20		20	ns
Write Cycle ^[8]						
t _{WC}	Write Cycle Time	20		25		ns
t _{SCE}	$\overline{CE}$ LOW to Write End	20		25		ns
t _{AW}	Address Setup to Write End	20		25		ns
t _{HA}	Address Hold from Write End	0		0		ns
t _{SA}	Address Setup to Write Start	0		0		ns
t _{PWE}	$\overline{WE}$ Pulse Width	15		20		ns
t _{SD}	Data Setup to Write End	10		15		ns
t _{HD}	Data Hold from Write End	0		0		ns
t _{LZWE}	$\overline{WE}$ HIGH to Low Z	5		5		ns
t _{HZWE}	$\overline{WE}$ LOW to High Z ^[7]		7		10	ns

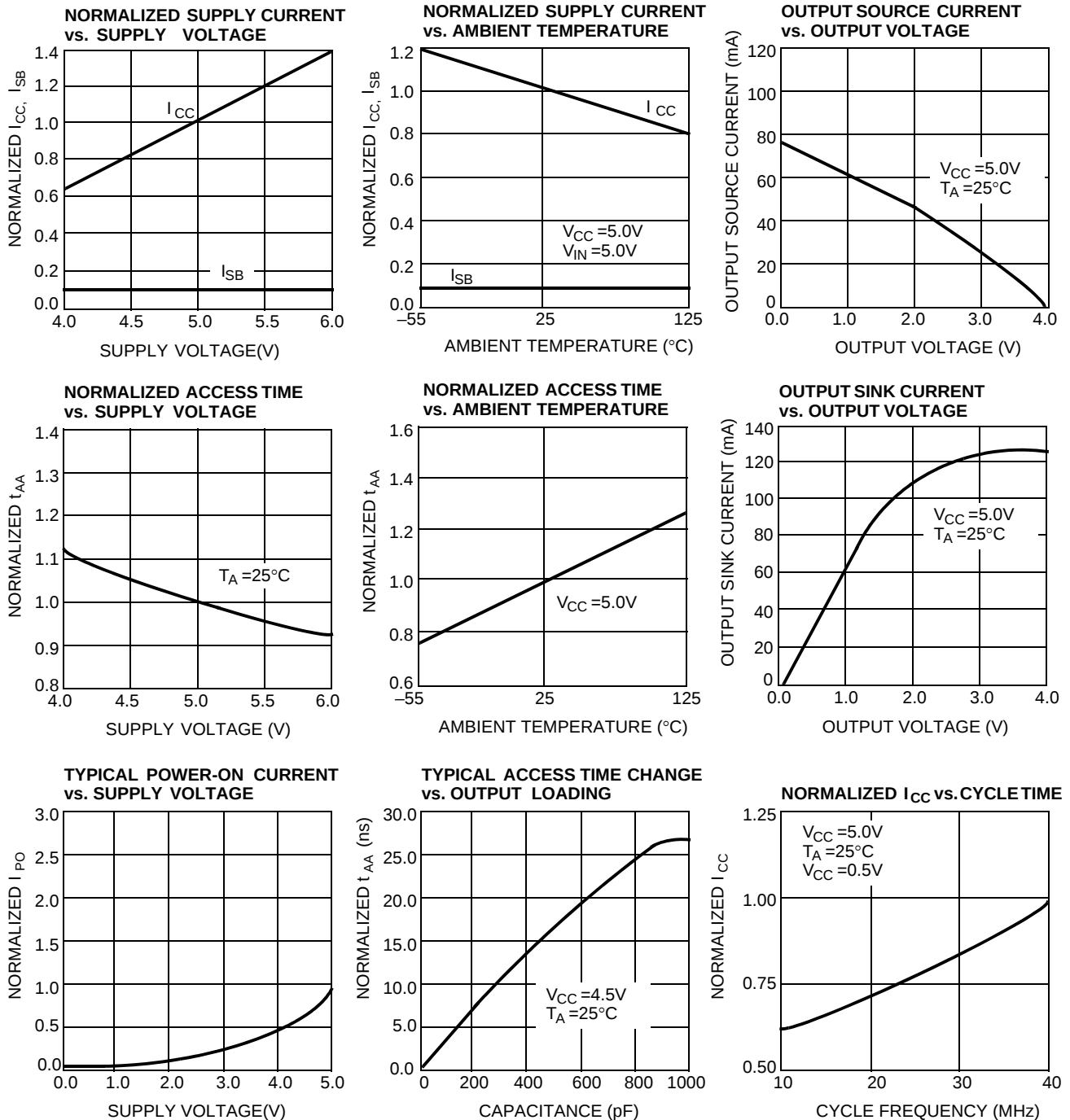
Switching Waveforms
Figure 3. Read Cycle No. 1^[9, 10]

Notes

- Test conditions assume signal transition time of 5 ns or less, timing reference levels of 1.5V, input pulse levels of 0 to 3.0V, and output loading of the specified I_{OL}/I_{OH} and 30 pF load capacitance.
- At any temperature and voltage condition, t_{HZCE} is less than t_{LZCE} for any device.
- t_{HZCE} and t_{HZWE} are specified with $C_L = 5$ pF as in part (b) of AC Test Loads and Waveforms on page 3. Transition is measured ± 500 mV from steady-state voltage.
- The internal write time of the memory is defined by the overlap of $\overline{CE}$ LOW and $\overline{WE}$ LOW. Both signals must be LOW to initiate a write and either signal can terminate a write by going HIGH. The data input setup and hold timing should be referenced to the rising edge of the signal that terminates the write.
- $\overline{WE}$ is HIGH for read cycle.
- Device is continuously selected, $\overline{CE} = V_{IL}$.

Figure 4. Read Cycle No. 2^[9, 11]

Figure 5. Write Cycle No. 1(WE Controlled)^[11]

Figure 6. Write Cycle No. 2(CE Controlled)^[11,12]

Notes

11. Address valid prior to or coincident with $\overline{CE}$ transition LOW.
12. If CE goes HIGH simultaneously with WE HIGH, the output remains in a high impedance state

Typical DC and AC Characteristics



Address Designators

Address Name	Address Function	Pin Number
A0	X3	1
A1	X4	2
A2	X5	3
A3	X6	4
A4	X7	5
A5	Y7	6
A6	Y6	7
A7	Y2	8
A8	Y3	14
A9	Y1	15
A10	Y0	16
A11	Y4	17
A12	Y5	18
A13	X0	19
A14	X1	20
A15	X2	21

Truth Table

CE	WE	Input/Output	Mode
H	X	High Z	Deselect/Power Down
L	H	Data Out	Read
L	L	Data In	Write

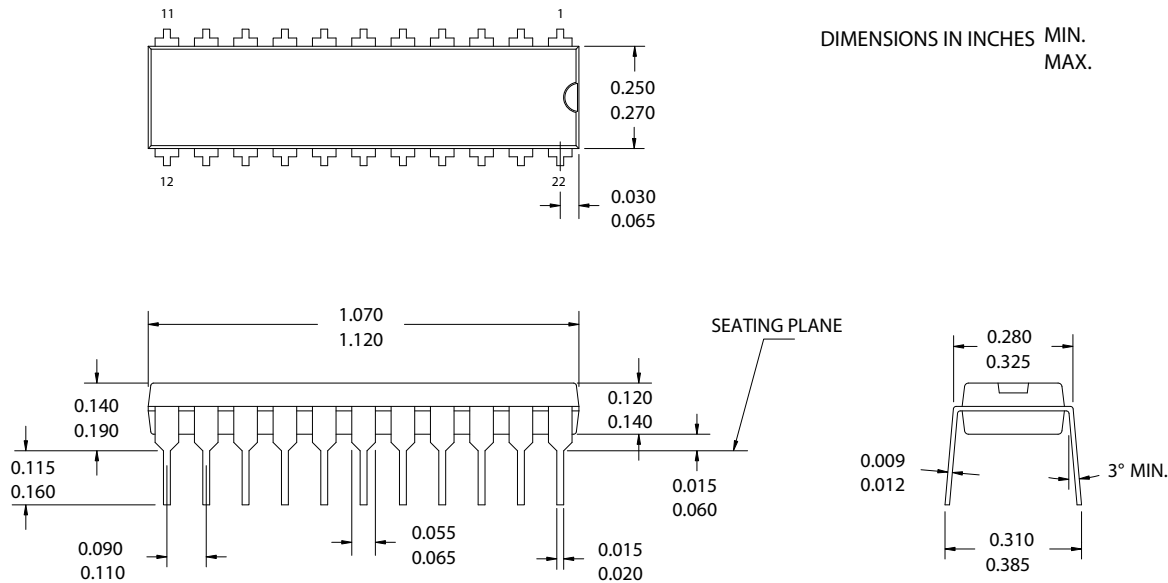
Ordering Information

Speed (ns)	Ordering Code	Package Diagram	Package Type	Operating Range
25	CY7C187-25PXC	51-85012	22-Pin (300-Mil) Molded DIP	Commercial
35	CY7C187-35PXC	51-85012	22-Pin (300-Mil) Molded DIP	

Contact your local Cypress sales representatives for the availability of parts

Package Diagram

Figure 7. 22-Pin (300 Mil) PDIP



51-85012-*A

Document History Page

Document Title: CY7C187 64K x 1 Static RAM Document Number: 38-05044				
Rev.	ECN No.	Orig. of Change	Submission Date	Description of Change
**	107146	SZV	09/10/01	Change from Spec number: 38-00038 to 38-05044
*A	486744	NXR	See ECN	Removed 20 ns speed bin Changed Low standby power from 220mW to 110mW Changed the description of I _{IX} from Input Load Current to Input Leakage Current in DC Electrical Characteristics table Updated the Ordering Information Table
*B	2753814	NXR	08/19/09	Removed SOJ package from product offering Updated the Ordering Information Table

Sales, Solutions, and Legal Information

Worldwide Sales and Design Support

Cypress maintains a worldwide network of offices, solution centers, manufacturer's representatives, and distributors. To find the office closest to you, visit us at cypress.com/sales.

Products

PSoC	psoc.cypress.com
Clocks & Buffers	clocks.cypress.com
Wireless	wireless.cypress.com
Memories	memory.cypress.com
Image Sensors	image.cypress.com

© Cypress Semiconductor Corporation, 2001-2009. The information contained herein is subject to change without notice. Cypress Semiconductor Corporation assumes no responsibility for the use of any circuitry other than circuitry embodied in a Cypress product. Nor does it convey or imply any license under patent or other rights. Cypress products are not warranted nor intended to be used for medical, life support, life saving, critical control or safety applications, unless pursuant to an express written agreement with Cypress. Furthermore, Cypress does not authorize its products for use as critical components in life-support systems where a malfunction or failure may reasonably be expected to result in significant injury to the user. The inclusion of Cypress products in life-support systems application implies that the manufacturer assumes all risk of such use and in doing so indemnifies Cypress against all charges.

Any Source Code (software and/or firmware) is owned by Cypress Semiconductor Corporation (Cypress) and is protected by and subject to worldwide patent protection (United States and foreign), United States copyright laws and international treaty provisions. Cypress hereby grants to licensee a personal, non-exclusive, non-transferable license to copy, use, modify, create derivative works of, and compile the Cypress Source Code and derivative works for the sole purpose of creating custom software and or firmware in support of licensee product to be used only in conjunction with a Cypress integrated circuit as specified in the applicable agreement. Any reproduction, modification, translation, compilation, or representation of this Source Code except as specified above is prohibited without the express written permission of Cypress.

Disclaimer: CYPRESS MAKES NO WARRANTY OF ANY KIND, EXPRESS OR IMPLIED, WITH REGARD TO THIS MATERIAL, INCLUDING, BUT NOT LIMITED TO, THE IMPLIED WARRANTIES OF MERCHANTABILITY AND FITNESS FOR A PARTICULAR PURPOSE. Cypress reserves the right to make changes without further notice to the materials described herein. Cypress does not assume any liability arising out of the application or use of any product or circuit described herein. Cypress does not authorize its products for use as critical components in life-support systems where a malfunction or failure may reasonably be expected to result in significant injury to the user. The inclusion of Cypress' product in a life-support systems application implies that the manufacturer assumes all risk of such use and in doing so indemnifies Cypress against all charges.

Use may be limited by and subject to the applicable Cypress software license agreement.