

Features

- Temperature ranges
 - Commercial: 0 °C to 70 °C
 - Industrial: -40 °C to 85 °C
 - Automotive-A: -40 °C to 85 °C
 - Automotive-E: -40 °C to 125 °C
- High speed
 - t_{AA} = 15 ns (Automotive)
- Complementary metal oxide semiconductor (CMOS) for optimum speed/power
- Low active power
 - 825 mW (maximum)
- Automatic power down when deselected
- Independent control of upper and lower bits
- Available in Pb-free and non Pb-free 44-pin TSOP II and 44-pin 400-mil-wide SOJ

Functional Description

The CY7C1021BN/CY7C10211BN is a high performance CMOS static RAM organized as 65,536 words by 16 bits. This device has an automatic power down feature that significantly reduces power consumption when deselected.

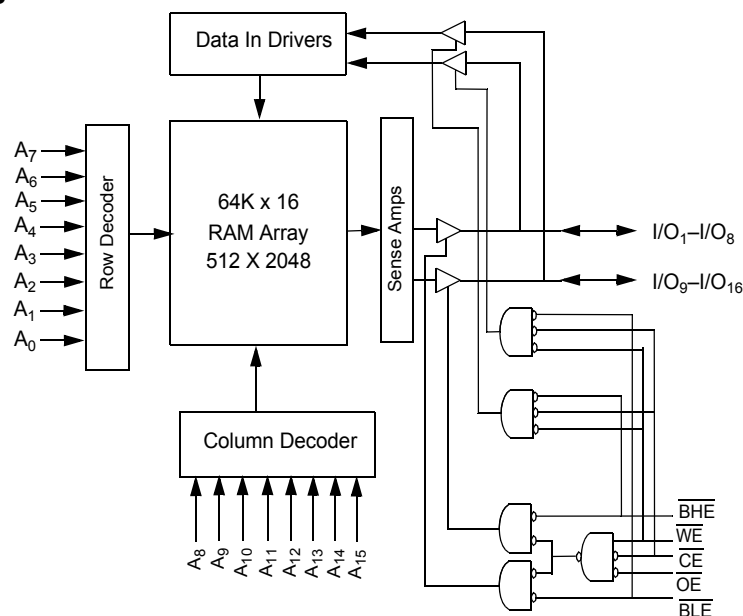
Writing to the device is accomplished by taking Chip Enable ($\overline{CE}$) and Write Enable (WE) inputs LOW. If Byte Low Enable (BLE) is LOW, then data from the input/output (I/O) pins (I/O₁ through I/O₈), is written into the location specified on the address pins (A₀ through A₁₅). If Byte High Enable (BHE) is LOW, then data from I/O pins (I/O₉ through I/O₁₆) is written into the location specified on the address pins (A₀ through A₁₅).

Reading from the device is accomplished by taking $\overline{CE}$ and Output Enable (OE) LOW while forcing WE HIGH. If BLE is LOW, then data from the memory location specified by the address pins appears on I/O₁ to I/O₈. If BHE is LOW, then data from memory appears on I/O₉ to I/O₁₆. See the [Truth Table on page 9](#) for a complete description of read and write modes.

The I/O pins (I/O₁ through I/O₁₆) are placed in a high impedance state when the device is deselected ($\overline{CE}$ HIGH), the outputs are disabled ($\overline{OE}$ HIGH), the BHE and BLE are disabled (BHE, BLE HIGH), or during a write operation ($\overline{CE}$ LOW, WE LOW).

The CY7C1021BN/CY7C10211BN is available in standard 44-pin TSOP type II and 44-pin 400-mil-wide SOJ packages. Use part number CY7C1021BN when ordering 15 ns t_{AA} .

Logic Block Diagram



Contents

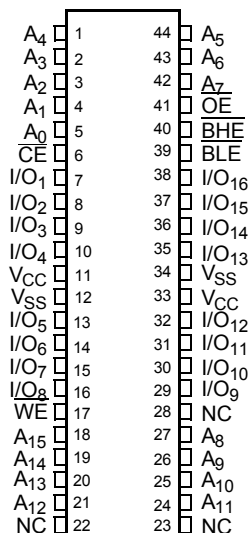
Selection Guide	3	Ordering Information	10
Pin Configuration	3	Ordering Code Definitions	10
Pin Definitions	3	Package Diagrams	11
Maximum Ratings	4	Acronyms	12
Operating Range	4	Document Conventions	12
Electrical Characteristics	4	Units of Measure	12
Capacitance	5	Document History Page	13
Thermal Resistance	5	Sales, Solutions, and Legal Information	14
AC Test Loads and Waveforms	5	Worldwide Sales and Design Support	14
Switching Characteristics	6	Products	14
Switching Waveforms	7	PSoC Solutions	14
Truth Table	9		

Selection Guide

Description		CY7C1021B-15
Maximum access time (ns)		15
Maximum operating current (mA)	Commercial/Industrial	130
	Automotive-A	130
	Automotive-E	130
Maximum CMOS standby current (mA)	Commercial/Industrial	10
	Commercial/Industrial (L version)	0.5
	Automotive-A (L version)	0.5
	Automotive-E	15

Pin Configuration

Figure 1. 44-pin SOJ/TSOP II (Top View)



Pin Definitions

Pin Name	Pin Number	I/O Type	Description
A ₀ –A ₁₅	1–5, 18–21, 24–27, 42–44	Input	Address inputs used to select one of the address locations.
I/O ₁ –I/O ₁₆	7–10, 13–16, 29–32, 35–38	Input/Output	Bidirectional data I/O lines. Used as input or output lines depending on operation.
NC	22, 23, 28	No Connect	Not connected to the die.
WE	17	Input/Control	Write enable input, active LOW. When selected LOW, a write is conducted. When deselected HIGH, a read is conducted.
CE	6	Input/Control	Chip enable input, active LOW. When LOW, selects the chip. When HIGH, deselects the chip.
BHE, BLE	40, 39	Input/Control	Byte enable select inputs, active LOW. BHE controls I/O ₁₆ –I/O ₉ , BLE controls I/O ₈ –I/O ₁ .
OE	41	Input/Control	Output enable, active LOW. Controls the direction of the I/O pins. When LOW, the I/O pins are allowed to behave as outputs. When deasserted HIGH, I/O pins are tristated, and act as input data pins.
V _{SS}	12, 34	Ground	Ground for the device. Should be connected to ground of the system.
V _{CC}	11, 33	Power Supply	Power supply inputs to the device.

Maximum Ratings

Exceeding the maximum ratings may impair the useful life of the device. These user guidelines are not tested.

Storage temperature -65 °C to +150 °C

Ambient temperature with power applied -55 °C to +125 °C

Supply voltage on V_{CC} relative to GND^[1] -0.5 V to +7.0 V

DC voltage applied to outputs in High Z state^[1] -0.5 V to $V_{CC} + 0.5$ V

DC input voltage^[1] -0.5 V to $V_{CC} + 0.5$ V

Current into outputs (LOW) 20 mA

Static discharge voltage (per MIL-STD-883, Method 3015) > 2001 V

Latch-up current > 200 mA

Operating Range

Range	Ambient Temperature (T_A) ^[2]	V_{CC}
Commercial	0 °C to +70 °C	5 V $\pm$ 10%
Industrial	-40 °C to +85 °C	
Automotive-A	-40 °C to +85 °C	
Automotive-E	-40 °C to +125 °C	

Electrical Characteristics

Over the operating range

Parameter	Description	Test Conditions		-15		Unit
				Min	Max	
V _{OH}	Output HIGH voltage	V _{CC} = Min, I _{OH} = −4.0 mA		2.4	−	V
V _{OL}	Output LOW voltage	V _{CC} = Min, I _{OL} = 8.0 mA		−	0.4	V
V _{IH}	Input HIGH voltage			2.2	6.0	V
V _{IL}	Input LOW voltage ^[1]			−0.5	0.8	V
I _{IX}	Input leakage current	GND ≤ V _I ≤ V _{CC}	Commercial / Industrial	−1	+1	μA
			Automotive-A	−1	+1	μA
			Automotive-E	−4	+4	μA
I _{OZ}	Output leakage current	GND ≤ V _I ≤ V _{CC} , Output Disabled	Commercial / Industrial	−1	+1	μA
			Automotive-A	−1	+1	μA
			Automotive-E	−4	+4	μA
I _{CC}	V _{CC} operating supply current	V _{CC} = Max, I _{OUT} = 0 mA, f = f _{MAX} = 1/t _{RC}	Commercial / Industrial	−	130	mA
			Automotive-A	−	130	
			Automotive-E	−	130	
I _{SB1}	Automatic CE power down current—TTL inputs	Max V _{CC} , $\overline{CE} \geq V_{IH}$, V _{IN} ≥ V _{IH} or V _{IN} ≤ V _{IL} , f = f _{MAX}	Commercial / Industrial	−	40	mA
			Automotive-A	−	40	
			Automotive-E	−	50	
I _{SB2}	Automatic CE power down current—CMOS inputs	Max V _{CC} , CE ≥ V _{CC} − 0.3 V, V _{IN} ≥ V _{CC} − 0.3 V, or V _{IN} ≤ 0.3 V, f = 0	Commercial / Industrial	−	10	mA
			Commercial / Industrial (L)	−	0.5	
			Automotive-A (L)	−	0.5	
			Automotive-E	−	15	

Notes

- V_{IL} (min.) = -2.0 V and V_{IH} (max) = $V_{CC} + 0.5$ V for pulse durations of less than 20 ns.
- T_A is the "Instant On" case temperature.

Capacitance

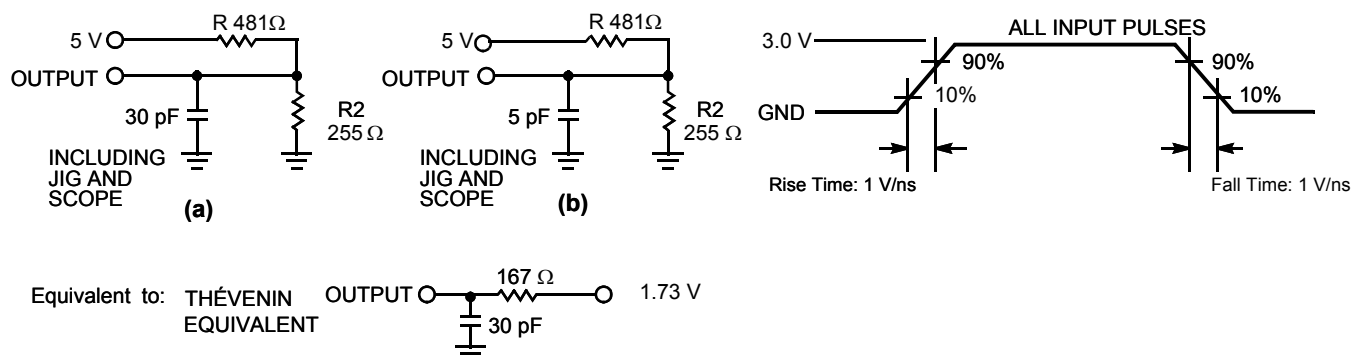
Parameter ^[3]	Description	Test Conditions	Max	Unit
C_{IN}	Input capacitance	$T_A = 25\text{ }^{\circ}\text{C}$, $f = 1\text{ MHz}$, $V_{CC} = 5.0\text{ V}$	8	pF
C_{OUT}	Output capacitance		8	pF

Thermal Resistance

Parameter ^[3]	Description	Test Conditions	44-pin SOJ	44-pin TSOP II	Unit
Θ_{JA}	Thermal resistance (junction to ambient)	Test conditions follow standard test methods and procedures for measuring thermal impedance, per EIA / JESD51.	64.32	76.89	$^{\circ}\text{C/W}$
Θ_{JC}	Thermal resistance (junction to case)		31.03	14.28	$^{\circ}\text{C/W}$

AC Test Loads and Waveforms

Figure 2. AC Test Loads and Waveforms



Note

3. Tested initially and after any design or process changes that may affect these parameters.

Switching Characteristics

Over the operating range

Parameter ^[4]	Description	CY7C1021B-15		Unit
		Min	Max	
Read Cycle				
t _{RC}	Read cycle time	15	–	ns
t _{AA}	Address to data valid	–	15	ns
t _{OHA}	Data hold from address change	3	–	ns
t _{ACE}	$\overline{CE}$ LOW to data valid	–	15	ns
t _{DOE}	$\overline{OE}$ LOW to data valid	–	7	ns
t _{LZOE}	$\overline{OE}$ LOW to low Z ^[4]	0	–	ns
t _{HZOE}	$\overline{OE}$ HIGH to high Z ^[5, 6]	–	7	ns
t _{LZCE}	$\overline{CE}$ LOW to low Z ^[5]	3	–	ns
t _{HZCE}	$\overline{CE}$ HIGH to high Z ^[5, 6]	–	7	ns
t _{PU}	$\overline{CE}$ LOW to power up	0	–	ns
t _{PD}	$\overline{CE}$ HIGH to power down	–	15	ns
t _{DBE}	Byte enable to data valid	–	7	ns
t _{LZBE}	Byte enable to low Z ^[5]	0	–	ns
t _{HZBE}	Byte disable to high Z ^[5, 6]	–	7	ns
Write Cycle ^[7]				
t _{WC}	Write cycle time	15	–	ns
t _{SCE}	$\overline{CE}$ LOW to write end	10	–	ns
t _{AW}	Address setup to write end	10	–	ns
t _{HA}	Address hold from write end	0	–	ns
t _{SA}	Address setup to write start	0	–	ns
t _{SD}	Data setup to write end	8	–	ns
t _{HD}	Data hold from write end	0	–	ns
t _{LZWE}	$\overline{WE}$ HIGH to low Z ^[5]	3	–	ns
t _{HZWE}	$\overline{WE}$ LOW to high Z ^[5, 6]	–	7	ns
t _{BW}	Byte enable to write end	9	–	ns

Notes

- Test conditions assume signal transition time of 3 ns or less, timing reference levels of 1.5 V, input pulse levels of 0 to 3.0 V, and output loading of the specified I_{OL}/I_{OH} and 30 pF load capacitance.
- At any temperature and voltage condition, t_{HZCE} is less than t_{LZCE} , t_{HZOE} is less than t_{LZOE} , t_{HZBE} is less than t_{LZBE} , and t_{HZWE} is less than t_{LZWE} for any device.
- t_{HZOE} , t_{HZBE} , t_{HZCE} , and t_{HZWE} are specified with a load capacitance of 5 pF as in part (b) of AC Test Loads. Transition is measured ± 500 mV from steady-state voltage.
- The internal write time of the memory is defined by the overlap of $\overline{CE}$ LOW, $\overline{WE}$ LOW, and $\overline{BHE} / \overline{BLE}$ LOW. $\overline{CE}$, $\overline{WE}$, and $\overline{BHE} / \overline{BLE}$ must be LOW to initiate a write, and the transition of these signals can terminate the write. The input data setup and hold timing should be referenced to the leading edge of the signal that terminates the write.

Switching Waveforms

Figure 3. Read Cycle No. 1 [8, 9]

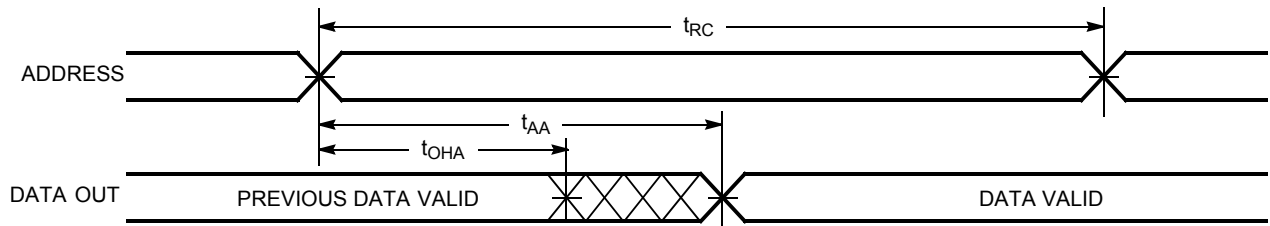
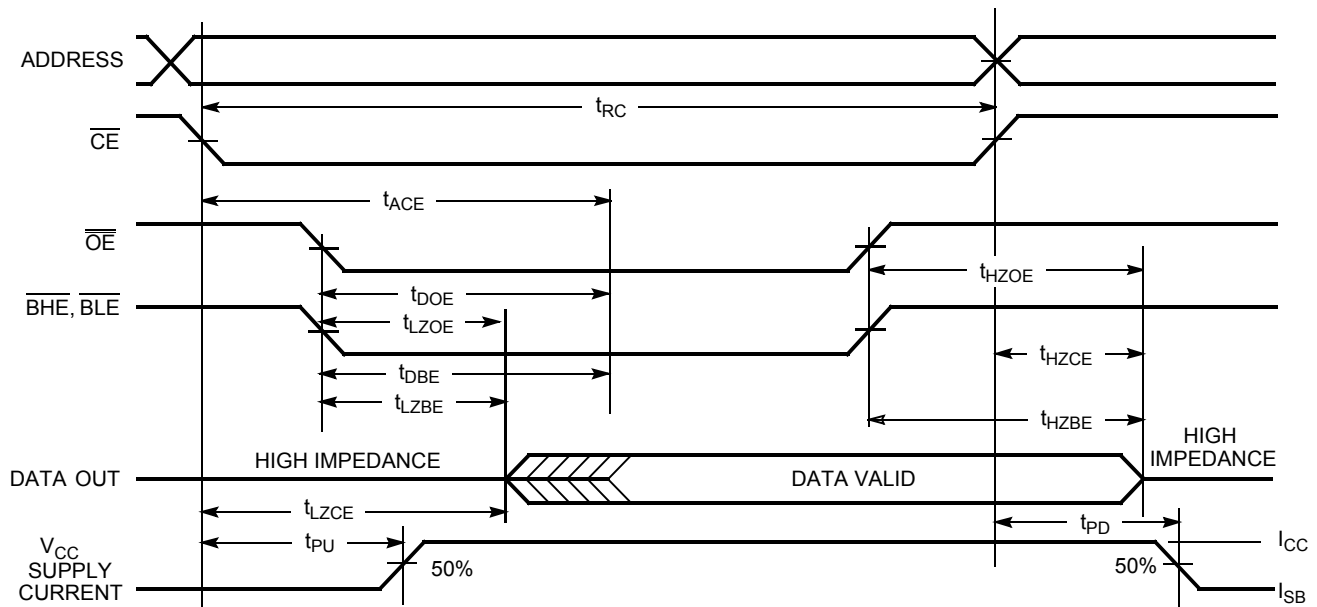


Figure 4. Read Cycle No. 2 ($\overline{OE}$ Controlled) [9, 10]



Notes

8. Device is continuously selected. $\overline{OE}$, $\overline{CE}$, $\overline{BHE}$, and $\overline{BLE}$ = V_{IL} .
9. $\overline{WE}$ is HIGH for read cycle.
10. Address valid prior to or coincident with $\overline{CE}$ transition LOW.

Figure 5. Write Cycle No. 1 ($\overline{\text{CE}}$ Controlled) [11, 12]

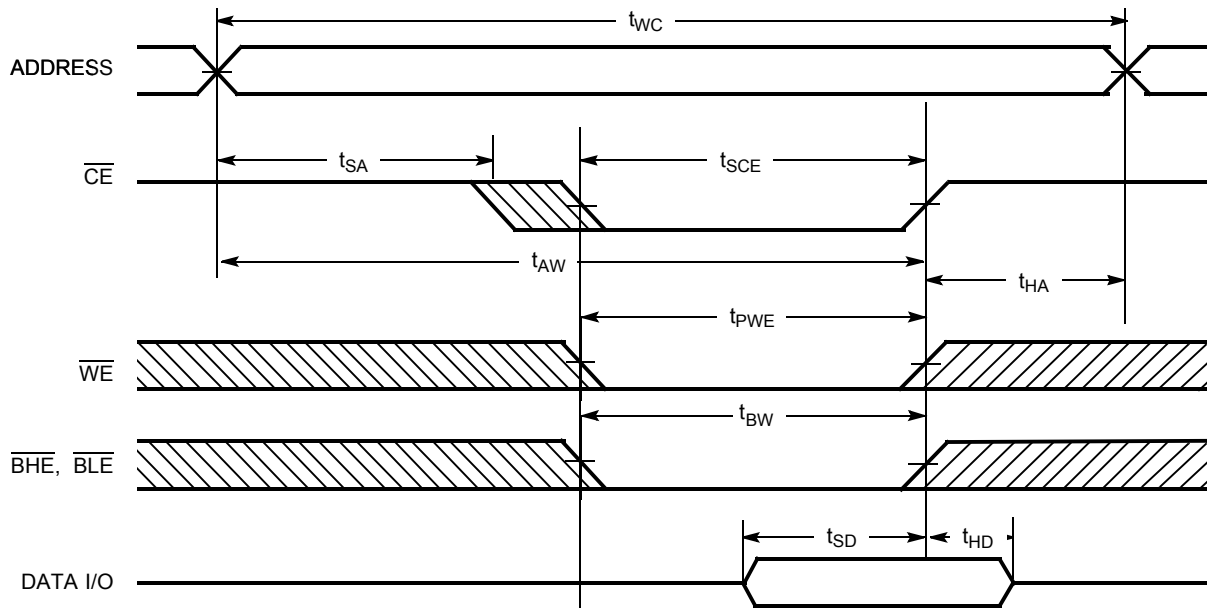
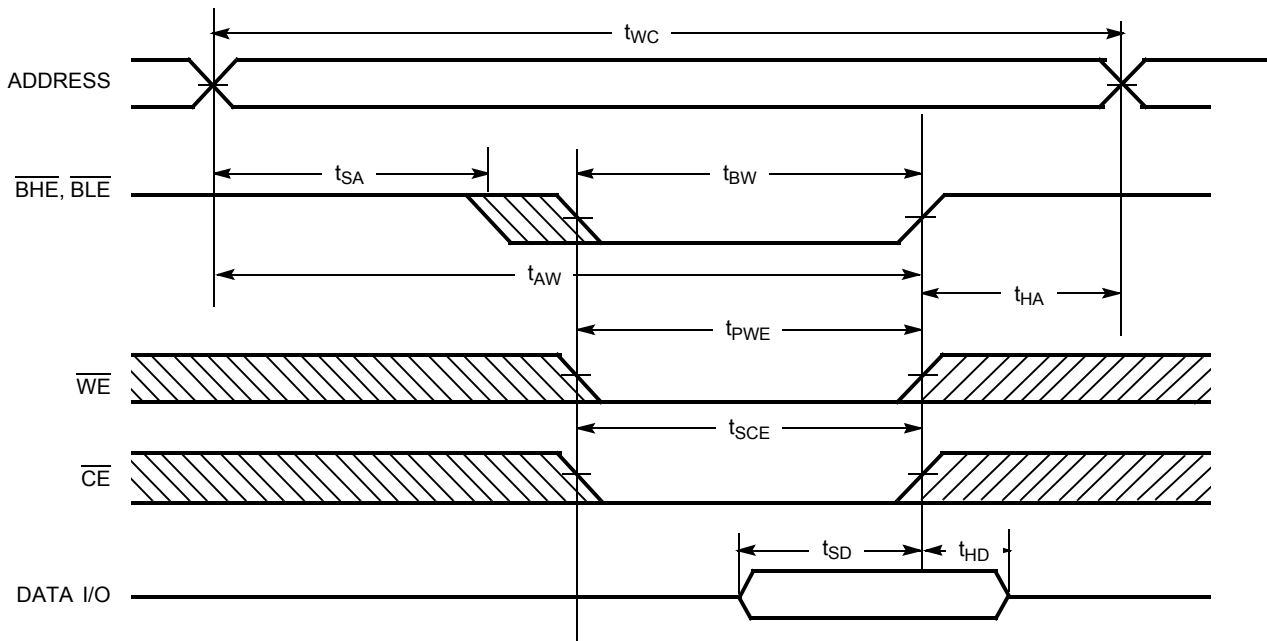
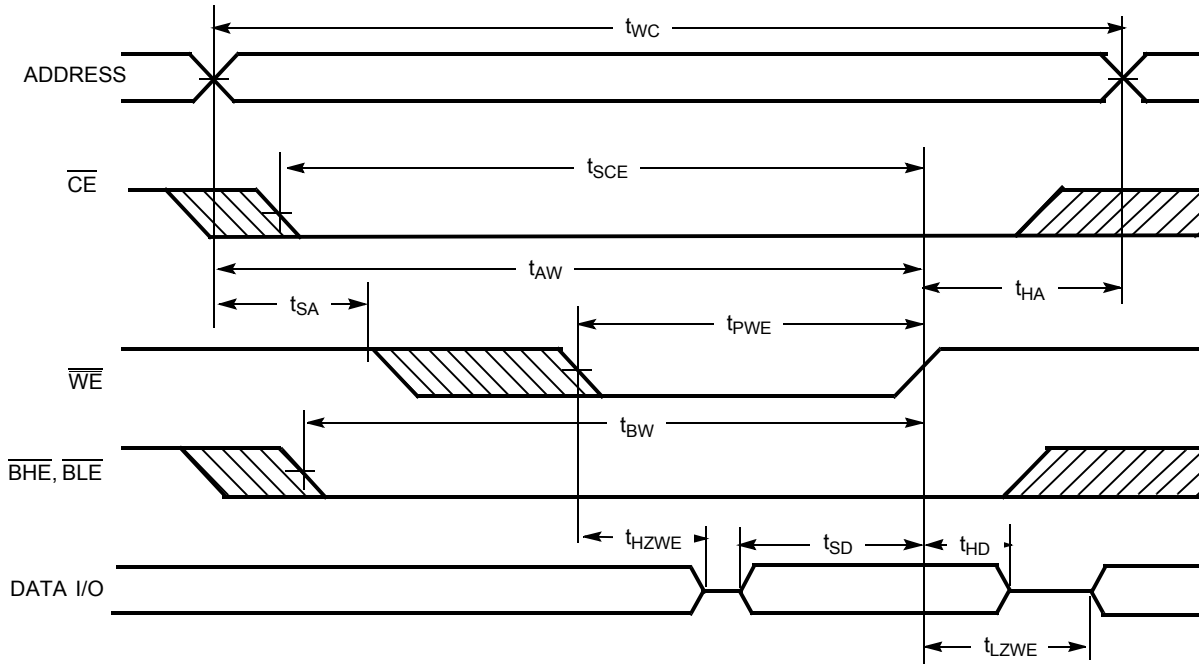


Figure 6. Write Cycle No. 2 ($\overline{\text{BLE}}$ or $\overline{\text{BHE}}$ Controlled)



Notes

11. Data I/O is high impedance if $\overline{\text{OE}}$ or $\overline{\text{BHE}}$ and/or $\overline{\text{BLE}} = V_{IH}$.
12. If $\overline{\text{CE}}$ goes HIGH simultaneously with $\overline{\text{WE}}$ going HIGH, the output remains in a high impedance state.

Figure 7. Write Cycle No. 3 ($\overline{\text{WE}}$ Controlled, $\overline{\text{OE}}$ LOW)

Truth Table

$\overline{\text{CE}}$	$\overline{\text{OE}}$	$\overline{\text{WE}}$	$\overline{\text{BLE}}$	$\overline{\text{BHE}}$	I/O ₁ –I/O ₈	I/O ₉ –I/O ₁₆	Mode	Power
H	X	X	X	X	High Z	High Z	Power down	Standby (I_{SB})
L	L	H	L	L	Data out	Data out	Read - All bits	Active (I_{CC})
			L	H	Data out	High Z	Read - Lower bits only	Active (I_{CC})
			H	L	High Z	Data out	Read - Upper bits only	Active (I_{CC})
L	X	L	L	L	Data In	Data In	Write - All bits	Active (I_{CC})
			L	H	Data In	High Z	Write - Lower bits only	Active (I_{CC})
			H	L	High Z	Data In	Write - Upper bits only	Active (I_{CC})
L	H	H	X	X	High Z	High Z	Selected, outputs disabled	Active (I_{CC})
L	X	X	H	H	High Z	High Z	Selected, outputs disabled	Active (I_{CC})

Ordering Information

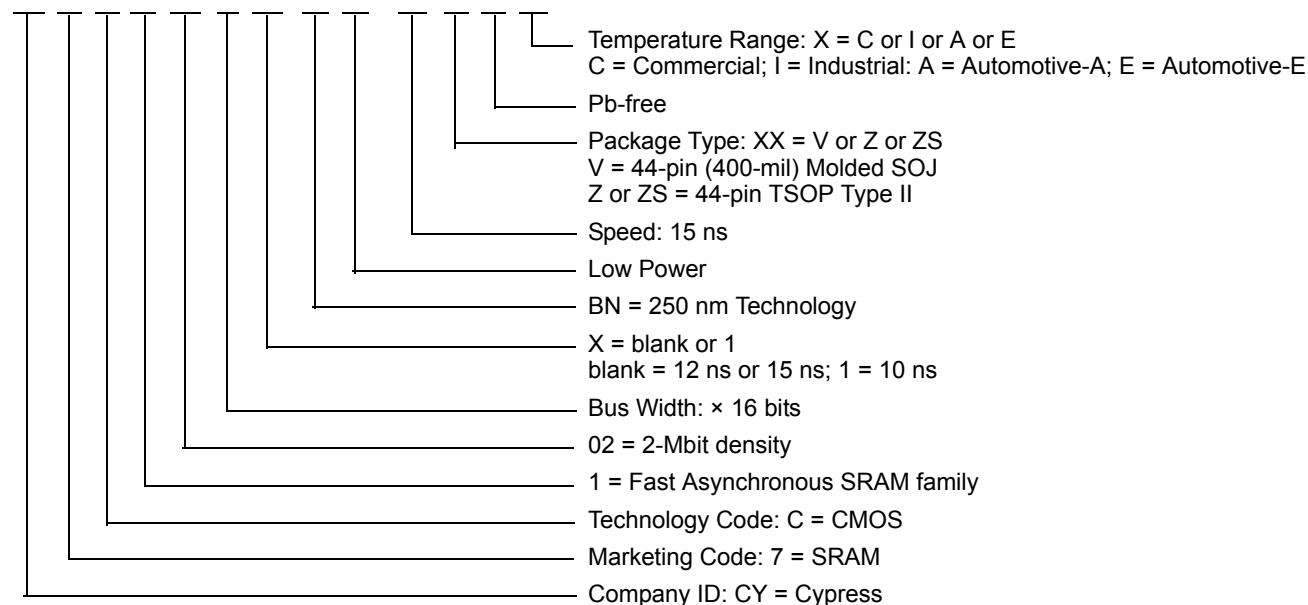
Cypress offers other versions of this product type in many different configurations and features. The following table contains only the list of parts that are currently available. For a complete listing of all options, refer to the product summary page at <http://www.cypress.com/products> or contact your local sales representative.

Cypress maintains a worldwide network of offices, solution centers, manufacturers' representatives and distributors. To find the office closest to you, visit us at <http://www.cypress.com/go/datasheet/offices>.

Speed (ns)	Ordering Code	Package Diagram	Package Type	Operating Range
15	CY7C1021BNL-15VXC	51-85082	44-pin (400-mil) Molded SOJ (Pb-free)	Commercial
	CY7C1021BN-15VXE			Automotive-E
	CY7C1021BNL-15ZXI	51-85087	44-pin TSOP Type II (Pb-free)	Industrial
	CY7C1021BNL-15ZSXA	51-85087	44-pin TSOP Type II (Pb-free)	Automotive-A
	CY7C1021BN-15ZSXE			Automotive-E

Ordering Code Definitions

CY 7 C 1 02 1 X BN L - 15 XX X X



Package Diagrams

Figure 8. 44-pin Molded SOJ (400-Mil) V44.4

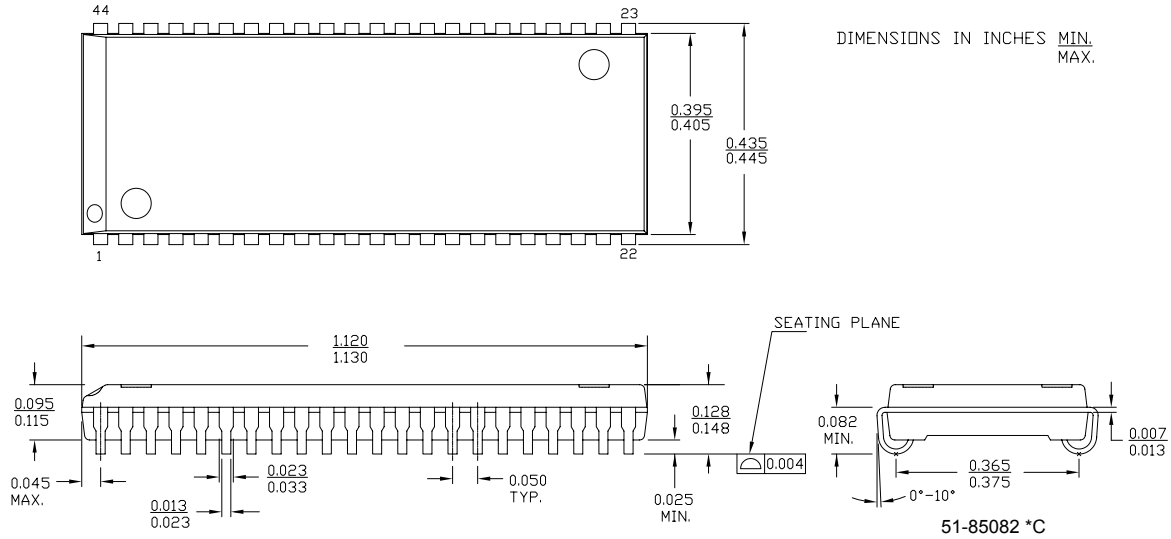
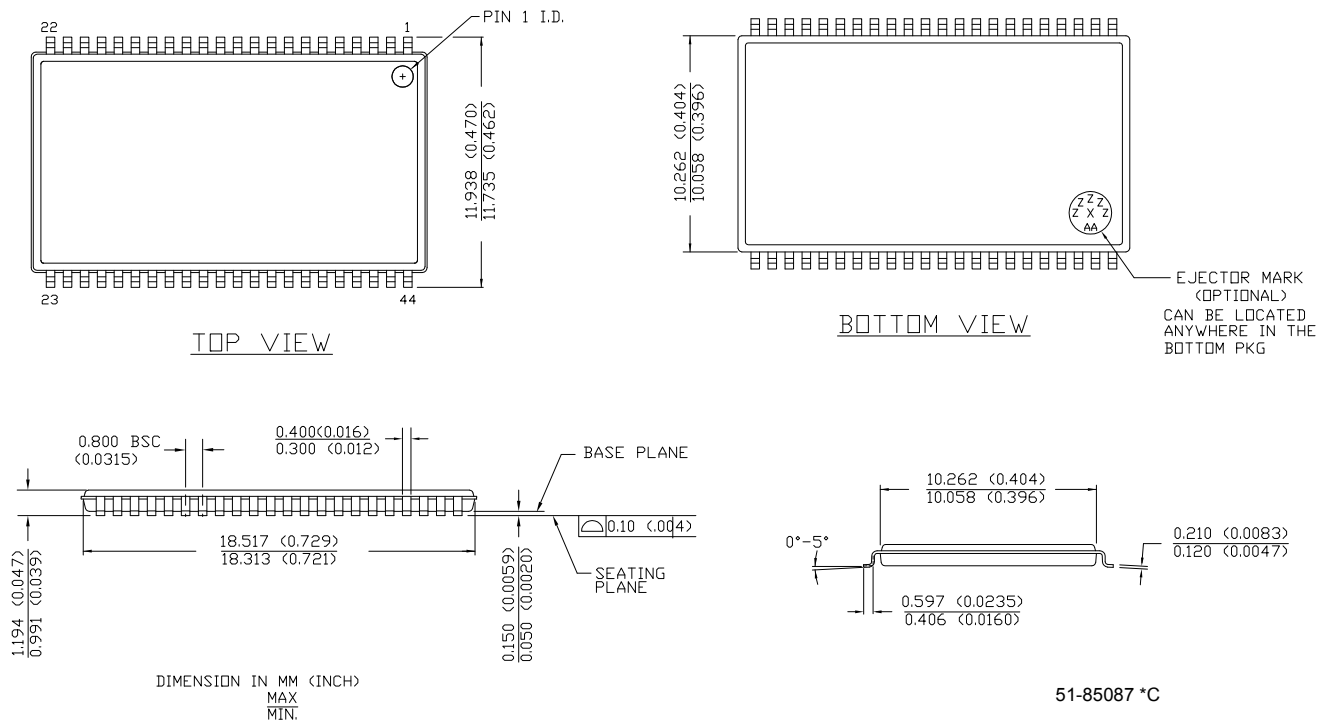


Figure 9. 44-pin TSOP Z44-II



Acronyms

Acronym	Description
BHE	byte high enable
BLE	byte low enable
$\overline{\text{CE}}$	chip enable
CMOS	complementary metal oxide semiconductor
I/O	input/output
OE	output enable
SOJ	small outline J-lead
SRAM	static random access memory
TSOP	thin small outline package
TTL	transistor-transistor logic
WE	write enable

Document Conventions

Units of Measure

Symbol	Unit of Measure
°C	degree Celsius
MHz	Mega Hertz
μA	micro Amperes
mA	milli Amperes
mm	milli meter
mW	milli Watts
ns	nano seconds
Ω	ohms
%	percent
pF	pico Farad
V	Volts
W	Watts

Document History Page

Document Title: CY7C1021BN, CY7C10211BN, 1-Mbit (64 K × 16) Static RAM Document Number: 001-06494				
Rev.	ECN No.	Submission Date	Orig. of Change	Description of Change
**	423877	See ECN	NXR	New datasheet
*A	505726	See ECN	NXR	Removed I _{OS} parameter from DC Electrical Characteristics table. Added Automotive products Updated ordering Information table
*B	2897061	03/22/10	AJU	Removed obsolete parts from ordering information table Updated package diagrams
*C	2947254	06/08/10	RAME	Corrected 'Byte write select inputs' to 'Byte Enable select inputs' on page 2. Added ohm (Ω) symbol in Thevenin equivalent circuit on page 4. Included T _{HZBE} and T _{LZBE} to Switching Characteristics table footnote 2 Included operating range for CY7C1021BNL-15ZXI in ordering information table.
*D	3328634	26/07/2011	AJU	Updated Features (Removed the information associated with speed bins -10 and -12). Removed the note "For best practice recommendations, refer to the Cypress application note, SRAM System Design Guidelines-AN1064." in page 1 and its reference in Functional Description . Updated Functional Description (Removed the information associated with speed bins -10 and -12). Updated Selection Guide (Removed the information associated with speed bins -10 and -12). Updated Electrical Characteristics (Removed the information associated with speed bins -10 and -12). Updated Switching Characteristics (Removed the information associated with speed bins -10 and -12). Updated Ordering Information . Added Acronyms and Units of Measure . Updated in new template.

Sales, Solutions, and Legal Information

Worldwide Sales and Design Support

Cypress maintains a worldwide network of offices, solution centers, manufacturers' representatives, and distributors. To find the office closest to you, visit us at [Cypress Locations](#).

Products

Automotive	cypress.com/go/automotive
Clocks & Buffers	cypress.com/go/clocks
Interface	cypress.com/go/interface
Lighting & Power Control	cypress.com/go/powerpsoc cypress.com/go/plc
Memory	cypress.com/go/memory
Optical & Image Sensing	cypress.com/go/image
PSoC	cypress.com/go/psoc
Touch Sensing	cypress.com/go/touch
USB Controllers	cypress.com/go/USB
Wireless/RF	cypress.com/go/wireless

PSoC Solutions

[psoc.cypress.com/solutions](#)
PSoC 1 | PSoC 3 | PSoC 5

© Cypress Semiconductor Corporation, 2006-2011. The information contained herein is subject to change without notice. Cypress Semiconductor Corporation assumes no responsibility for the use of any circuitry other than circuitry embodied in a Cypress product. Nor does it convey or imply any license under patent or other rights. Cypress products are not warranted nor intended to be used for medical, life support, life saving, critical control or safety applications, unless pursuant to an express written agreement with Cypress. Furthermore, Cypress does not authorize its products for use as critical components in life-support systems where a malfunction or failure may reasonably be expected to result in significant injury to the user. The inclusion of Cypress products in life-support systems application implies that the manufacturer assumes all risk of such use and in doing so indemnifies Cypress against all charges.

Any Source Code (software and/or firmware) is owned by Cypress Semiconductor Corporation (Cypress) and is protected by and subject to worldwide patent protection (United States and foreign), United States copyright laws and international treaty provisions. Cypress hereby grants to licensee a personal, non-exclusive, non-transferable license to copy, use, modify, create derivative works of, and compile the Cypress Source Code and derivative works for the sole purpose of creating custom software and or firmware in support of licensee product to be used only in conjunction with a Cypress integrated circuit as specified in the applicable agreement. Any reproduction, modification, translation, compilation, or representation of this Source Code except as specified above is prohibited without the express written permission of Cypress.

Disclaimer: CYPRESS MAKES NO WARRANTY OF ANY KIND, EXPRESS OR IMPLIED, WITH REGARD TO THIS MATERIAL, INCLUDING, BUT NOT LIMITED TO, THE IMPLIED WARRANTIES OF MERCHANTABILITY AND FITNESS FOR A PARTICULAR PURPOSE. Cypress reserves the right to make changes without further notice to the materials described herein. Cypress does not assume any liability arising out of the application or use of any product or circuit described herein. Cypress does not authorize its products for use as critical components in life-support systems where a malfunction or failure may reasonably be expected to result in significant injury to the user. The inclusion of Cypress' product in a life-support systems application implies that the manufacturer assumes all risk of such use and in doing so indemnifies Cypress against all charges.

Use may be limited by and subject to the applicable Cypress software license agreement.