

Product Preview

TMOS E-FET™

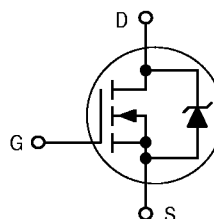
High Energy Power FET

D2PAK for Surface Mount

N-Channel Enhancement-Mode Silicon Gate

This advanced high voltage TMOS E-FET is designed to withstand high energy in the avalanche mode and switch efficiently. This new high energy device also offers a drain-to-source diode with fast recovery time. Designed for high voltage, high speed switching applications such as power supplies, PWM motor controls and other inductive loads, the avalanche energy capability is specified to eliminate the guesswork in designs where inductive loads are switched and offer additional safety margin against unexpected voltage transients.

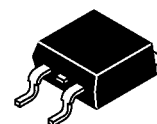
- Avalanche Energy Capability Specified at Elevated Temperature
- Low Stored Gate Charge for Efficient Switching
- Internal Source-to-Drain Diode Designed to Replace External Zener Transient Suppressor — Absorbs High Energy in the Avalanche Mode
- Source-to-Drain Diode Recovery Time Comparable to Discrete Fast Recovery Diode



MTB3N60E

Motorola Preferred Device

TMOS POWER FET
3.0 AMPERES
600 VOLTS
R_{DS(on)} = 2.2 OHMS



CASE 418B-03, Style 2
D2PAK

MAXIMUM RATINGS (T_C = 25°C unless otherwise noted)

Rating	Symbol	Value	Unit
Drain-Source Voltage	V _{DSS}	600	V _{dc}
Drain-Gate Voltage (R _{GS} = 1.0 MΩ)	V _{DGR}	600	V _{dc}
Gate-Source Voltage — Continuous	V _{GS}	±20	V _{dc}
— Non-repetitive	V _{GSM}	±40	V _{pk}
Drain Current — Continuous	I _D	3.0	A _{dc}
— Continuous @ 100°C	I _D	2.4	
— Pulsed	I _{DM}	14	
Total Power Dissipation @ T _C = 25°C	P _D	75	Watts
Derate above 25°C		0.6	W/°C
Total Power Dissipation @ T _A = 25°C ⁽¹⁾		2.5	Watts
Operating and Storage Temperature Range	T _J , T _{stg}	-55 to 150	°C

UNCLAMPED DRAIN-TO-SOURCE AVALANCHE CHARACTERISTICS (T_J < 150°C)

Single Pulse Drain-to-Source Avalanche Energy — T _J = 25°C	W _{DSR} ⁽²⁾	290	mJ
— T _J = 100°C		46	
Repetitive Pulse Drain-to-Source Avalanche Energy	W _{DSR} ⁽³⁾	7.5	

THERMAL CHARACTERISTICS

Thermal Resistance — Junction to Case	R _{θJC}	1.67	°C/W
— Junction to Ambient	R _{θJA}	62.5	
— Junction to Ambient ⁽¹⁾	R _{θJA}	50	
Maximum Lead Temperature for Soldering Purposes, 1/8" from case for 10 seconds	T _L	260	°C

(1) When surface mounted to an FR-4 board using the minimum recommended pad size

(2) V_{DD} = 50 V, I_D = 3.0 A

(3) Pulse Width and frequency is limited by T_{J(max)} and thermal response

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Preferred devices are Motorola recommended choices for future use and best overall value.

MTB3N60E**ELECTRICAL CHARACTERISTICS** ($T_J = 25^\circ\text{C}$ unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Drain-to-Source Breakdown Voltage ($V_{GS} = 0$, $I_D = 250\ \mu\text{Adc}$)	$V_{(BR)DSS}$	600	—	—	Vdc
Zero Gate Voltage Drain Current ($V_{DS} = 600\ \text{V}$, $V_{GS} = 0$) ($V_{DS} = 480\ \text{V}$, $V_{GS} = 0$, $T_J = 125^\circ\text{C}$)	I_{DSS}	— —	— —	10 100	μAdc
Gate-Body Leakage Current — Forward ($V_{GSF} = 20\ \text{Vdc}$, $V_{DS} = 0$)	I_{GSSF}	—	—	100	nAdc
Gate-Body Leakage Current — Reverse ($V_{GSR} = 20\ \text{Vdc}$, $V_{DS} = 0$)	I_{GSSR}	—	—	100	nAdc

ON CHARACTERISTICS*

Gate Threshold Voltage ($V_{DS} = V_{GS}$, $I_D = 250\ \mu\text{Adc}$) ($T_J = 125^\circ\text{C}$)	$V_{GS(th)}$	2.0 1.5	— —	4.0 3.5	Vdc
Static Drain-to-Source On-Resistance ($V_{GS} = 10\ \text{Vdc}$, $I_D = 1.5\ \text{A}$)	$R_{DS(on)}$	—	2.1	2.2	Ohms
Drain-to-Source On-Voltage ($V_{GS} = 10\ \text{Vdc}$) ($I_D = 3.0\ \text{A}$) ($I_D = 1.5\ \text{A}$, $T_J = 100^\circ\text{C}$)	$V_{DS(on)}$	— —	— —	9.0 7.5	Vdc
Forward Transconductance ($V_{DS} = 15\ \text{Vdc}$, $I_D = 1.5\ \text{A}$)	g_{FS}	1.5	—	—	mhos

DYNAMIC CHARACTERISTICS

Input Capacitance	(VDS = 25 V, VGS = 0, f = 1.0 MHz)	C_{iss}	—	770	—	pF
Output Capacitance		C_{oss}	—	105	—	
Transfer Capacitance		C_{rss}	—	19	—	

SWITCHING CHARACTERISTICS*

Turn-On Delay Time	(VDD = 300 V, $I_D \approx 3.0\ \text{A}$, $R_L = 100\ \Omega$, $R_G = 12\ \Omega$, $V_{GS(on)} = 10\ \text{V}$)	$t_{d(on)}$	—	23	—	ns
Rise Time		t_r	—	34	—	
Turn-Off Delay Time		$t_{d(off)}$	—	58	—	
Fall Time		t_f	—	35	—	
Total Gate Charge	(VDS = 420 V, $I_D = 3.0\ \text{A}$, $V_{GS} = 10\ \text{V}$)	Q_g	—	28	31	nC
Gate-Source Charge		Q_{gs}	—	5.0	—	
Gate-Drain Charge		Q_{gd}	—	17	—	

SOURCE-DRAIN DIODE CHARACTERISTICS

Forward On-Voltage	(IS = 3.0 A, di/dt = 100 A/ μs)	V_{SD}	—	—	1.4	Vdc
Forward Turn-On Time		t_{on}	—	**	—	ns
Reverse Recovery Time		t_{rr}	—	400	—	

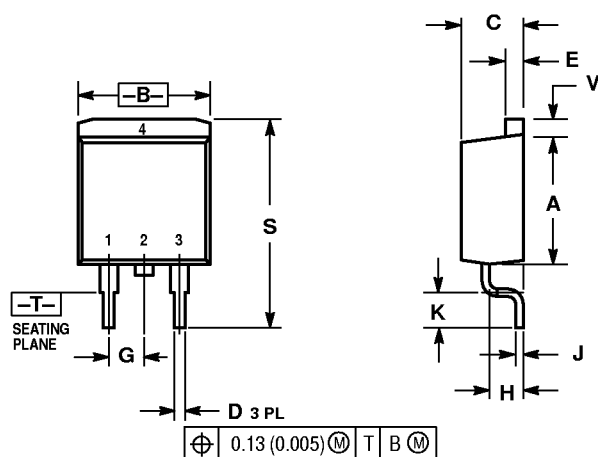
INTERNAL PACKAGE INDUCTANCE

Internal Drain Inductance (Measured from the contact screw on tab to center of die) (Measured from the drain lead 0.25" from package to center of die)	L_d	— —	3.5 4.5	— —	nH
Internal Source Inductance (Measured from the source lead 0.25" from package to source bond pad)	L_s	—	7.5	—	

* Pulse Test: Pulse Width = 300 μs , Duty Cycle $\leq 2.0\%$.

** Limited by circuit inductance.

PACKAGE DIMENSIONS



- NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
 2. CONTROLLING DIMENSION: INCH.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.340	0.380	8.64	9.65
B	0.380	0.405	9.65	10.29
C	0.160	0.190	4.06	4.83
D	0.020	0.035	0.51	0.89
E	0.045	0.055	1.14	1.40
G	0.100	BSC	2.54	BSC
H	0.080	0.110	2.03	2.79
J	0.018	0.025	0.46	0.64
K	0.090	0.110	2.29	2.79
S	0.575	0.625	14.60	15.88
V	0.045	0.055	1.14	1.40

STYLE 2:
PIN 1. GATE
2. DRAIN
3. SOURCE
4. DRAIN

CASE 418B-03
ISSUE C