



Is Now Part of



ON Semiconductor®

To learn more about ON Semiconductor, please visit our website at
www.onsemi.com

Please note: As part of the Fairchild Semiconductor integration, some of the Fairchild orderable part numbers will need to change in order to meet ON Semiconductor's system requirements. Since the ON Semiconductor product management systems do not have the ability to manage part nomenclature that utilizes an underscore (_), the underscore (_) in the Fairchild part numbers will be changed to a dash (-). This document may contain device numbers with an underscore (_). Please check the ON Semiconductor website to verify the updated device numbers. The most current and up-to-date ordering information can be found at www.onsemi.com. Please email any questions regarding the system integration to Fairchild_questions@onsemi.com.

ON Semiconductor and the ON Semiconductor logo are trademarks of Semiconductor Components Industries, LLC dba ON Semiconductor or its subsidiaries in the United States and/or other countries. ON Semiconductor owns the rights to a number of patents, trademarks, copyrights, trade secrets, and other intellectual property. A listing of ON Semiconductor's product/patent coverage may be accessed at www.onsemi.com/site/pdf/Patent-Marking.pdf. ON Semiconductor reserves the right to make changes without further notice to any products herein. ON Semiconductor makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does ON Semiconductor assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. Buyer is responsible for its products and applications using ON Semiconductor products, including compliance with all laws, regulations and safety requirements or standards, regardless of any support or applications information provided by ON Semiconductor. "Typical" parameters which may be provided in ON Semiconductor data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals" must be validated for each customer application by customer's technical experts. ON Semiconductor does not convey any license under its patent rights nor the rights of others. ON Semiconductor products are not designed, intended, or authorized for use as a critical component in life support systems or any FDA Class 3 medical devices or medical devices with a same or similar classification in a foreign jurisdiction or any devices intended for implantation in the human body. Should Buyer purchase or use ON Semiconductor products for any such unintended or unauthorized application, Buyer shall indemnify and hold ON Semiconductor and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that ON Semiconductor was negligent regarding the design or manufacture of the part. ON Semiconductor is an Equal Opportunity/Affirmative Action Employer. This literature is subject to all applicable copyright laws and is not for resale in any manner.



December 2015

FDPC8014AS

PowerTrench® Power Clip 25V Asymmetric Dual N-Channel MOSFET

Features

Q1: N-Channel

■ Max $r_{DS(on)}$ = 3.8 mΩ at V_{GS} = 10 V, I_D = 20 A

■ Max $r_{DS(on)}$ = 4.7 mΩ at V_{GS} = 4.5 V, I_D = 18 A

Q2: N-Channel

■ Max $r_{DS(on)}$ = 1.0 mΩ at V_{GS} = 10 V, I_D = 40 A

■ Max $r_{DS(on)}$ = 1.2 mΩ at V_{GS} = 4.5 V, I_D = 37 A

■ Low Inductance Packaging Shortens Rise/fall Times, Resulting in Lower Switching Losses

■ MOSFET Integration Enables Optimum Layout for Lower Circuit Inductance and Reduced Switch Node Ringing

■ RoHS Compliant

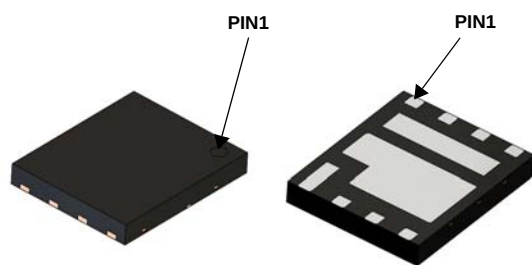


General Description

This device includes two specialized N-Channel MOSFETs in a dual package. The switch node has been internally connected to enable easy placement and routing of synchronous buck converters. The control MOSFET (Q1) and synchronous SyncFET™ (Q2) have been designed to provide optimal power efficiency.

Applications

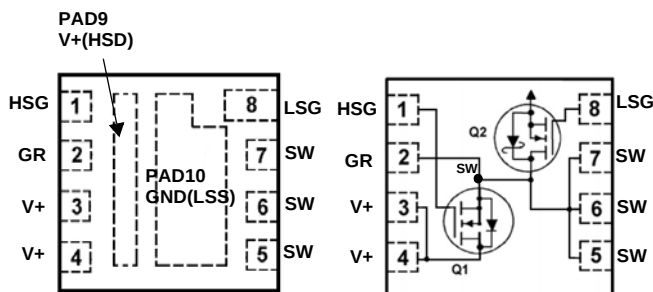
- Computing
- Communications
- General Purpose Point of Load



Top

Power Clip 5X6

Bottom



Pin	Name	Description	Pin	Name	Description	Pin	Name	Description
1	HSG	High Side Gate	3,4,9	V+(HSD)	High Side Drain	8	LSG	Low Side Gate
2	GR	Gate Return	5,6,7	SW	Switching Node, Low Side Drain	10	GND(LSS)	Low Side Source

MOSFET Maximum Ratings $T_A = 25^\circ\text{C}$ unless otherwise noted.

Symbol	Parameter	Q1	Q2	Units
V_{DS}	Drain to Source Voltage	25 ^{Note5}	25	V
V_{GS}	Gate to Source Voltage	±12	±12	V
I_D	Drain Current -Continuous $T_C = 25^\circ\text{C}$ (Note 6)	59	159	A
	-Continuous $T_C = 100^\circ\text{C}$ (Note 6)	37	100	
	-Continuous $T_A = 25^\circ\text{C}$	20 ^{Note1a}	40 ^{Note1b}	
	-Pulsed (Note 4)	266	1116	
E_{AS}	Single Pulse Avalanche Energy (Note 3)	73	294	mJ
P_D	Power Dissipation for Single Operation $T_C = 25^\circ\text{C}$	21	37	W
	Power Dissipation for Single Operation $T_A = 25^\circ\text{C}$	2.1 ^{Note1a}	2.3 ^{Note1b}	
T_J, T_{STG}	Operating and Storage Junction Temperature Range	-55 to +150		°C

Thermal Characteristics

$R_{\theta JC}$	Thermal Resistance, Junction to Case	6.0	3.3	°C/W
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient	60 ^{Note1a}	55 ^{Note1b}	
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient	130 ^{Note1c}	120 ^{Note1d}	

Package Marking and Ordering Information

Device Marking	Device	Package	Reel Size	Tape Width	Quantity
FDPC8014AS	FDPC8014AS	Power Clip 56	13 "	12 mm	3000 units

Electrical Characteristics $T_J = 25\text{ }^{\circ}\text{C}$ unless otherwise noted.

Symbol	Parameter	Test Conditions	Type	Min.	Typ.	Max.	Units
--------	-----------	-----------------	------	------	------	------	-------

Off Characteristics

BV_{DSS}	Drain to Source Breakdown Voltage	$I_D = 250\text{ }\mu\text{A}$, $V_{GS} = 0\text{ V}$ $I_D = 1\text{ mA}$, $V_{GS} = 0\text{ V}$	Q1 Q2	25 25			V
$\frac{\Delta BV_{DSS}}{\Delta T_J}$	Breakdown Voltage Temperature Coefficient	$I_D = 250\text{ }\mu\text{A}$, referenced to $25\text{ }^{\circ}\text{C}$ $I_D = 10\text{ mA}$, referenced to $25\text{ }^{\circ}\text{C}$	Q1 Q2		24 25		mV/ $^{\circ}\text{C}$
I_{DSS}	Zero Gate Voltage Drain Current	$V_{DS} = 20\text{ V}$, $V_{GS} = 0\text{ V}$ $V_{DS} = 20\text{ V}$, $V_{GS} = 0\text{ V}$	Q1 Q2			1 500	μA μA
I_{GSS}	Gate to Source Leakage Current, Forward	$V_{GS} = 12\text{ V/-8 V}$, $V_{DS} = 0\text{ V}$ $V_{GS} = 12\text{ V/-8 V}$, $V_{DS} = 0\text{ V}$	Q1 Q2			± 100 ± 100	nA nA

On Characteristics

$V_{GS(th)}$	Gate to Source Threshold Voltage	$V_{GS} = V_{DS}$, $I_D = 250\text{ }\mu\text{A}$ $V_{GS} = V_{DS}$, $I_D = 1\text{ mA}$	Q1 Q2	0.8 1.0	1.3 1.5	2.5 3.0	V
$\frac{\Delta V_{GS(th)}}{\Delta T_J}$	Gate to Source Threshold Voltage Temperature Coefficient	$I_D = 250\text{ }\mu\text{A}$, referenced to $25\text{ }^{\circ}\text{C}$ $I_D = 10\text{ mA}$, referenced to $25\text{ }^{\circ}\text{C}$	Q1 Q2		-4 -3		mV/ $^{\circ}\text{C}$
$r_{DS(on)}$	Drain to Source On Resistance	$V_{GS} = 10\text{ V}$, $I_D = 20\text{ A}$ $V_{GS} = 4.5\text{ V}$, $I_D = 18\text{ A}$ $V_{GS} = 10\text{ V}$, $I_D = 20\text{ A}$, $T_J = 125\text{ }^{\circ}\text{C}$	Q1		2.9 3.6 3.9	3.8 4.7 5.3	m Ω
		$V_{GS} = 10\text{ V}$, $I_D = 40\text{ A}$ $V_{GS} = 4.5\text{ V}$, $I_D = 37\text{ A}$ $V_{GS} = 10\text{ V}$, $I_D = 40\text{ A}$, $T_J = 125\text{ }^{\circ}\text{C}$	Q2		0.75 0.9 1.0	1.0 1.2 1.5	
g_{FS}	Forward Transconductance	$V_{DS} = 5\text{ V}$, $I_D = 20\text{ A}$	Q1		182		S
		$V_{DS} = 5\text{ V}$, $I_D = 40\text{ A}$	Q2		296		

Dynamic Characteristics

C_{iss}	Input Capacitance	Q1: Q2:	Q1 Q2		1695 6985	2375 9780	pF
C_{oss}	Output Capacitance	$V_{DS} = 13\text{ V}$, $V_{GS} = 0\text{ V}$, $f = 1\text{ MHz}$	Q1 Q2		495 2170	710 3040	pF
C_{rss}	Reverse Transfer Capacitance	Q2: $V_{DS} = 13\text{ V}$, $V_{GS} = 0\text{ V}$, $f = 1\text{ MHz}$	Q1 Q2		54 172	100 245	pF
R_g	Gate Resistance		Q1	0.1	0.4	1.2	Ω
			Q2	0.1	0.4	1.2	

Switching Characteristics

$t_{d(on)}$	Turn-On Delay Time	Q1: $V_{DD} = 13\text{ V}$, $I_D = 20\text{ A}$, $R_{GEN} = 6\text{ }\Omega$	Q1 Q2		8 16	16 29	ns
t_r	Rise Time		Q1 Q2		2 6	10 12	ns
$t_{d(off)}$	Turn-Off Delay Time	Q2: $V_{DD} = 13\text{ V}$, $I_D = 40\text{ A}$, $R_{GEN} = 6\text{ }\Omega$	Q1 Q2		24 48	38 76	ns
t_f	Fall Time		Q1 Q2		2 5	10 10	ns
Q_g	Total Gate Charge	$V_{GS} = 0\text{ V to }10\text{ V}$	Q1 Q2		25 97	35 135	nC
Q_g	Total Gate Charge	$V_{GS} = 0\text{ V to }4.5\text{ V}$	Q1 Q2		11 44	16 62	nC
Q_{gs}	Gate to Source Gate Charge	Q2 $V_{DD} = 13\text{ V}$, $I_D = 40\text{ A}$	Q1 Q2		3.4 14		nC
Q_{gd}	Gate to Drain "Miller" Charge		Q1 Q2		2.2 9		nC

Electrical Characteristics $T_J = 25^\circ\text{C}$ unless otherwise noted.

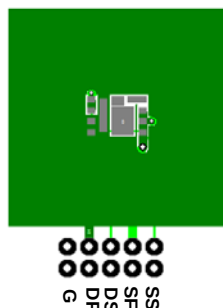
Symbol	Parameter	Test Conditions	Type	Min.	Typ.	Max.	Units
--------	-----------	-----------------	------	------	------	------	-------

Drain-Source Diode Characteristics

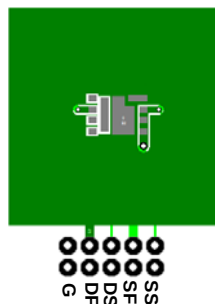
V_{SD}	Source to Drain Diode Forward Voltage	$V_{GS} = 0\text{ V}, I_S = 20\text{ A}$ (Note 2) $V_{GS} = 0\text{ V}, I_S = 40\text{ A}$ (Note 2)	Q1 Q2		0.8 0.8	1.2 1.2	V
I_S	Diode continuous forward current	$T_C = 25^\circ\text{C}$	Q1 Q2		59 159		A
$I_{S,\text{Pulse}}$	Diode pulse current		Q1 Q2		266 1116		A
t_{rr}	Reverse Recovery Time	Q1 $I_F = 20\text{ A}, di/dt = 100\text{ A}/\mu\text{s}$	Q1 Q2		25 44	40 70	ns
Q_{rr}	Reverse Recovery Charge	Q2 $I_F = 40\text{ A}, di/dt = 300\text{ A}/\mu\text{s}$	Q1 Q2		10 78	20 125	nC

Notes:

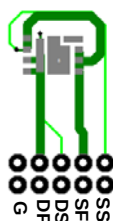
1. $R_{\theta JA}$ is determined with the device mounted on a 1 in² pad 2 oz copper pad on a 1.5 x 1.5 in. board of FR-4 material. $R_{\theta JC}$ is guaranteed by design while $R_{\theta CA}$ is determined by the user's board design.



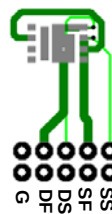
a. 60 °C/W when mounted on a 1 in² pad of 2 oz copper



b. 55 °C/W when mounted on a 1 in² pad of 2 oz copper



c. 130 °C/W when mounted on a minimum pad of 2 oz copper



d. 120 °C/W when mounted on a minimum pad of 2 oz copper

2 Pulse Test: Pulse Width < 300 μs , Duty cycle < 2.0%.

3. Q1 : E_{AS} of 73 mJ is based on starting $T_J = 25^\circ\text{C}$; N-ch: $L = 3\text{ mH}$, $I_{AS} = 7\text{ A}$, $V_{DD} = 30\text{ V}$, $V_{GS} = 10\text{ V}$. 100% test at $L = 0.1\text{ mH}$, $I_{AS} = 24\text{ A}$.

Q2: E_{AS} of 294 mJ is based on starting $T_J = 25^\circ\text{C}$; N-ch: $L = 3\text{ mH}$, $I_{AS} = 14\text{ A}$, $V_{DD} = 25\text{ V}$, $V_{GS} = 10\text{ V}$. 100% test at $L = 0.1\text{ mH}$, $I_{AS} = 46\text{ A}$.

4. Pulsed Id please refer to Fig 11 and Fig 24 SOA graph for more details.

5. The continuous V_{DS} rating is 25 V; However, a pulse of 30 V peak voltage for no longer than 100 ns duration at 600 KHz frequency can be applied.

6. Computed continuous current limited to Max Junction Temperature only, actual continuous current will be limited by thermal & electro-mechanical application board design.

Typical Characteristics (Q1 N-Channel) $T_J = 25^\circ\text{C}$ unless otherwise noted.

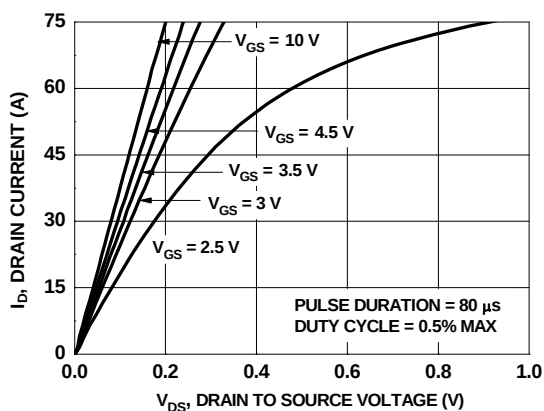


Figure 1. On Region Characteristics

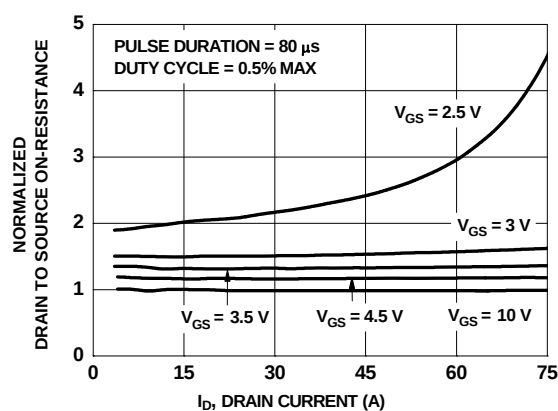


Figure 2. Normalized On-Resistance vs. Drain Current and Gate Voltage

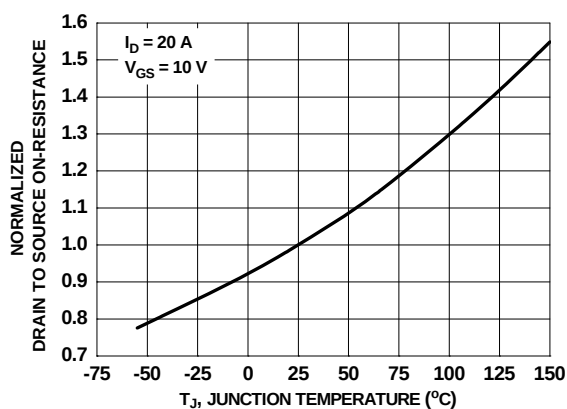


Figure 3. Normalized On Resistance vs. Junction Temperature

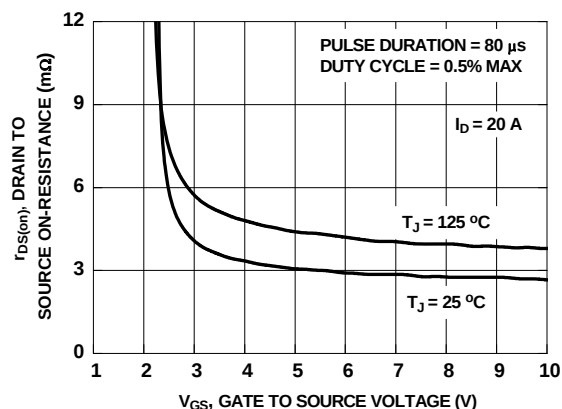


Figure 4. On-Resistance vs. Gate to Source Voltage

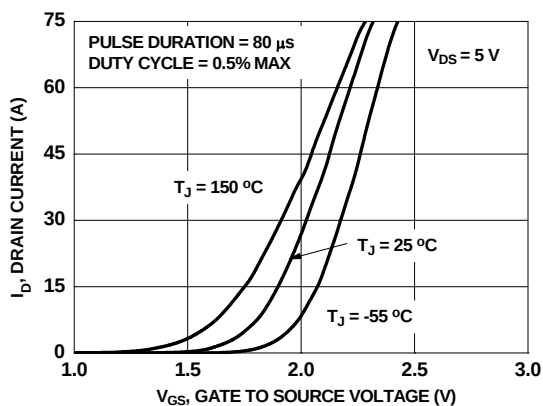


Figure 5. Transfer Characteristics

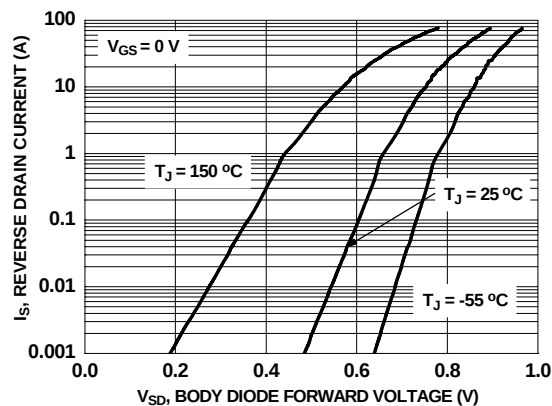


Figure 6. Source to Drain Diode Forward Voltage vs. Source Current

Typical Characteristics (Q1 N-Channel) $T_J = 25^\circ\text{C}$ unless otherwise noted.

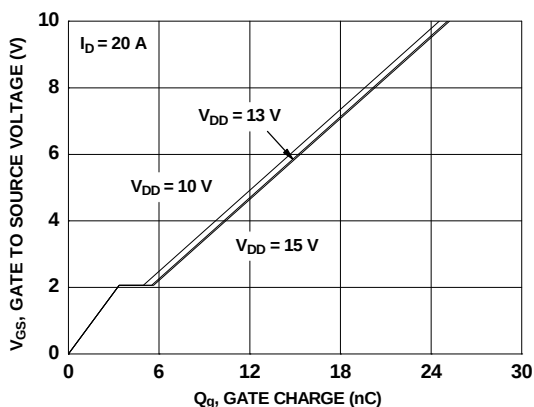


Figure 7. Gate Charge Characteristics

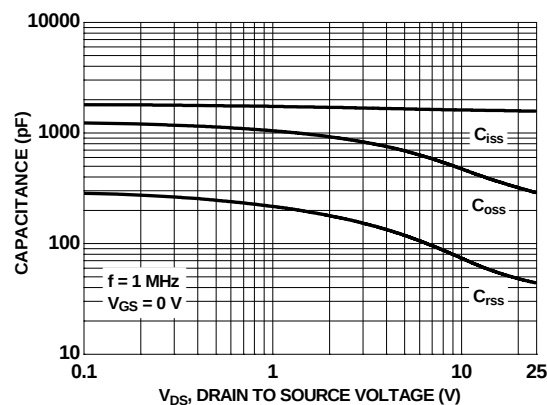


Figure 8. Capacitance vs. Drain to Source Voltage

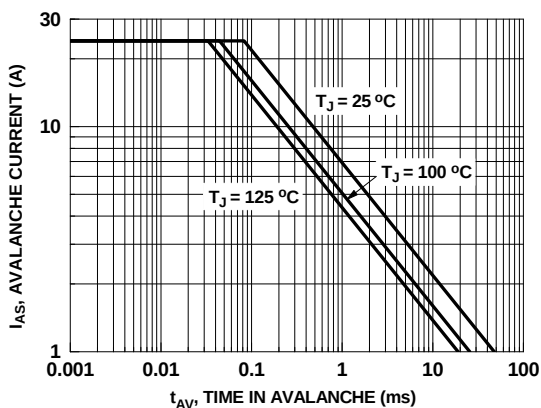


Figure 9. Unclamped Inductive Switching Capability

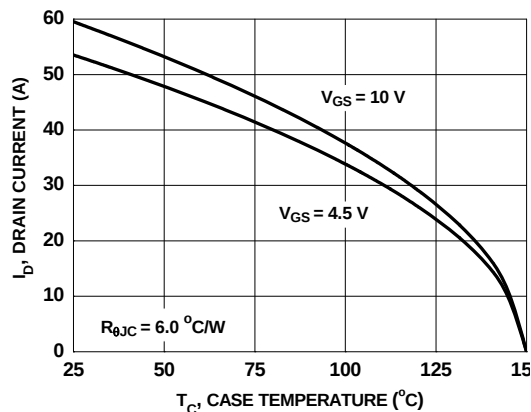


Figure 10. Maximum Continuous Drain Current vs. Case Temperature

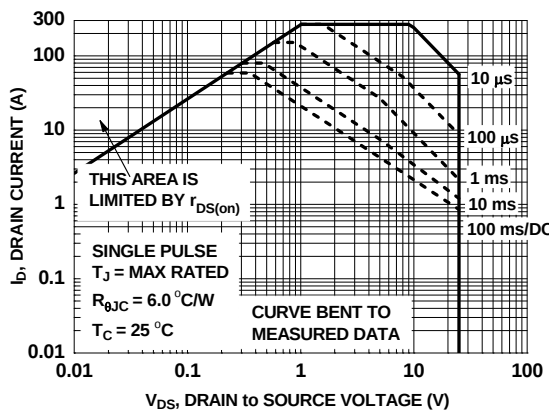


Figure 11. Forward Bias Safe Operating Area

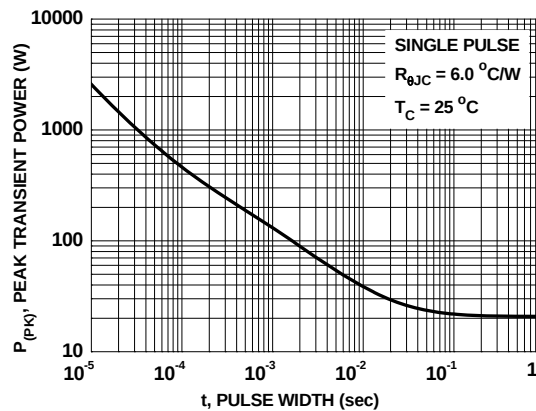


Figure 12. Single Pulse Maximum Power Dissipation

Typical Characteristics (Q1 N-Channel) $T_J = 25^\circ\text{C}$ unless otherwise noted.

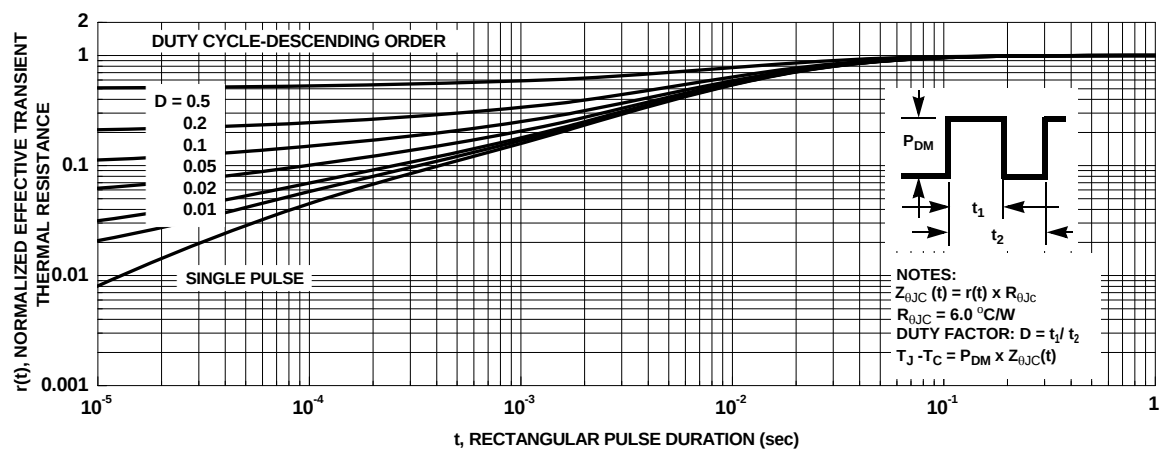


Figure 13. Junction-to-Case Transient Thermal Response Curve

Typical Characteristics (Q2 N-Channel) $T_J = 25^\circ\text{C}$ unless otherwise noted.

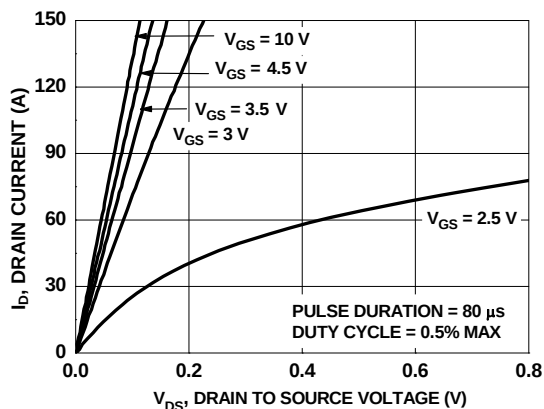


Figure 14. On- Region Characteristics

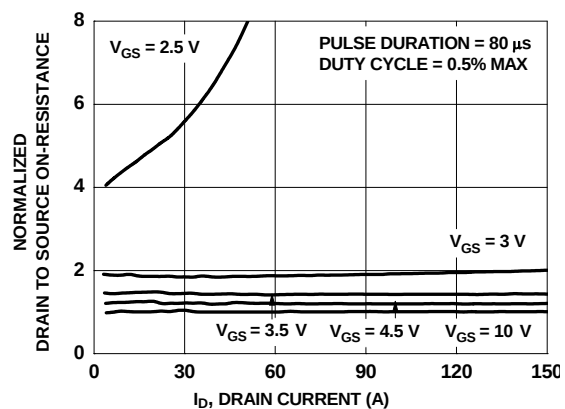


Figure 15. Normalized on-Resistance vs. Drain Current and Gate Voltage

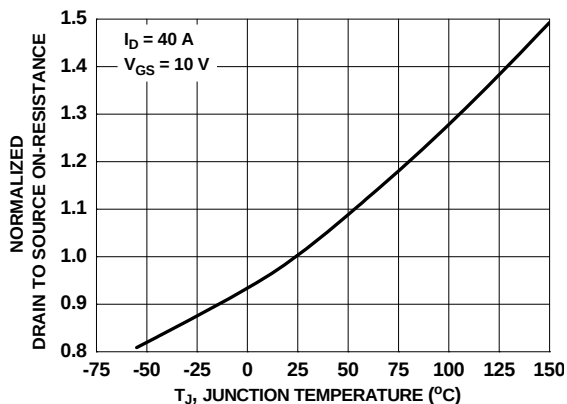


Figure 16. Normalized On-Resistance vs. Junction Temperature

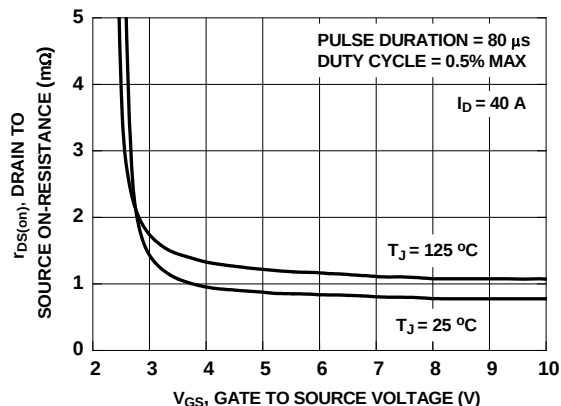


Figure 17. On-Resistance vs. Gate to Source Voltage

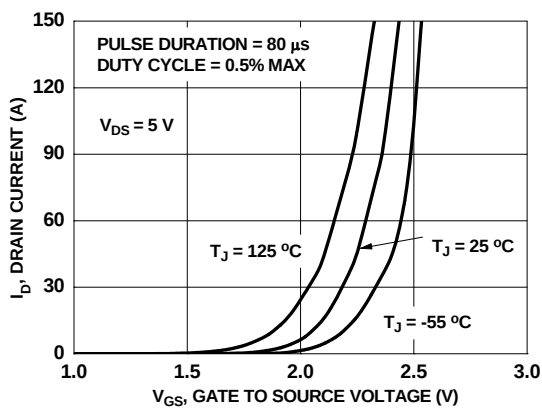


Figure 18. Transfer Characteristics

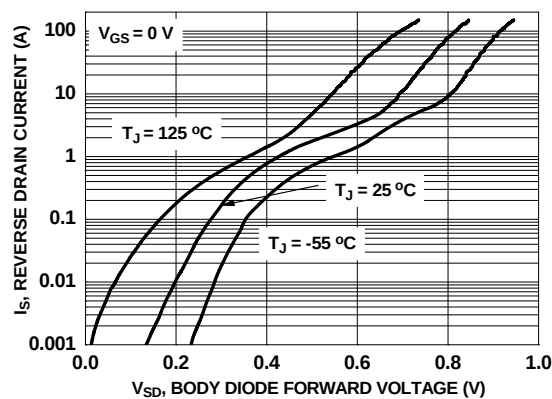


Figure 19. Source to Drain Diode Forward Voltage vs. Source Current

Typical Characteristics (Q2 N-Channel) $T_J = 25^\circ\text{C}$ unless otherwise noted.

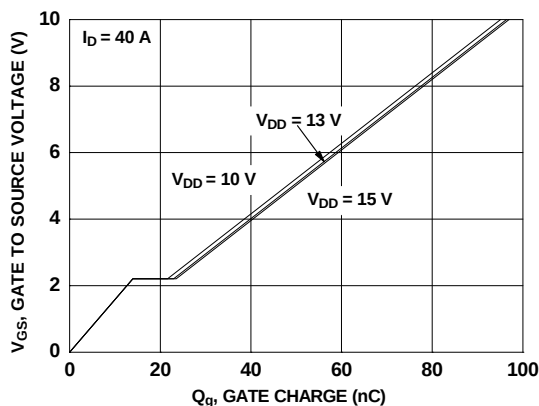


Figure 20. Gate Charge Characteristics

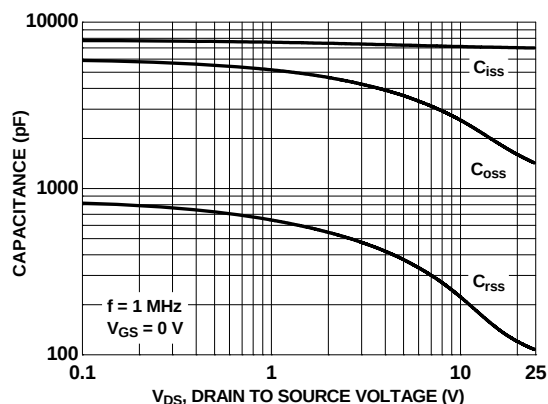


Figure 21. Capacitance vs. Drain to Source Voltage

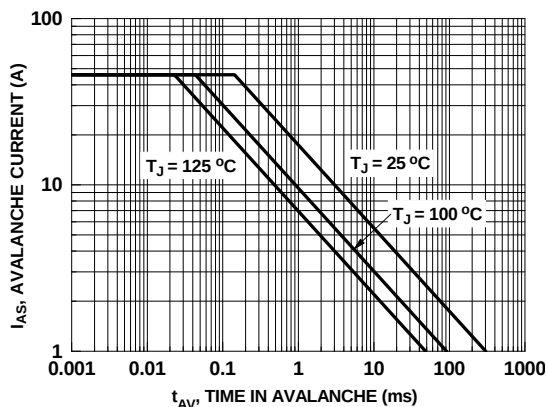


Figure 22. Unclamped Inductive Switching Capability

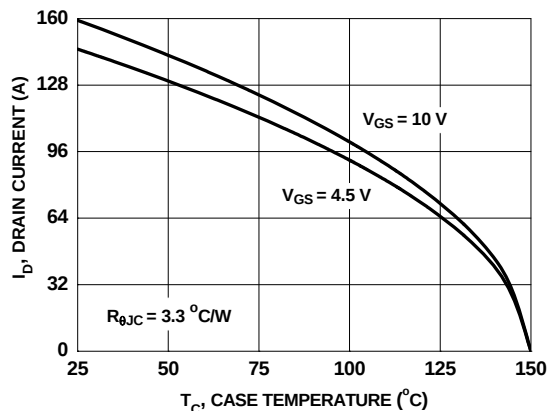


Figure 23. Maximum Continuous Drain Current vs. Case Temperature

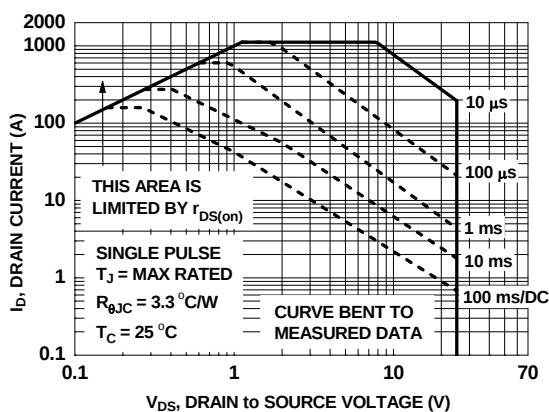


Figure 24. Forward Bias Safe Operating Area

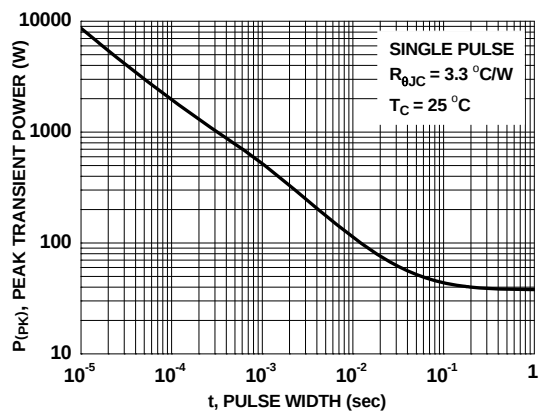


Figure 25. Single Pulse Maximum Power Dissipation

Typical Characteristics (Q2 N-Channel) $T_J = 25\text{ }^{\circ}\text{C}$ unless otherwise noted.

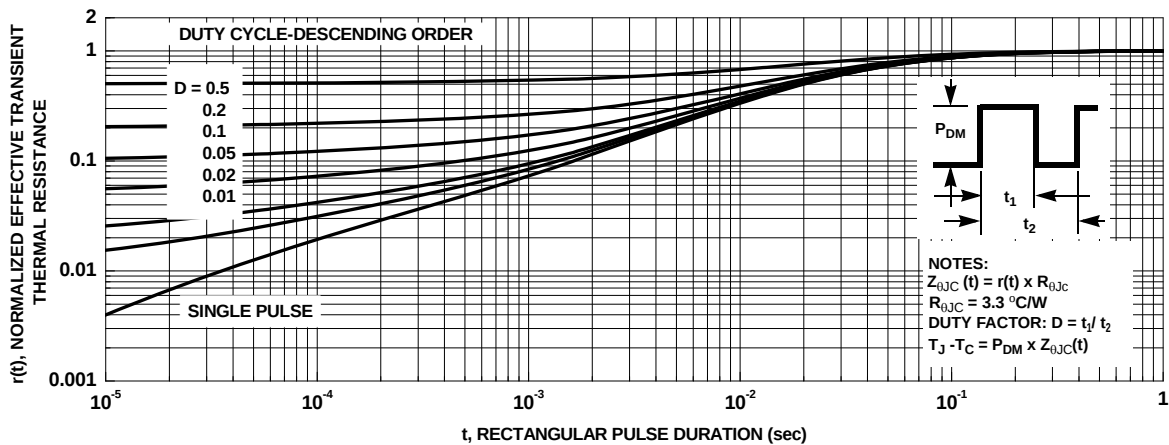


Figure 26. Junction-to-Case Transient Thermal Response Curve

Typical Characteristics (continued)

SyncFET™ Schottky body diode Characteristics

Fairchild's SyncFET™ process embeds a Schottky diode in parallel with PowerTrench® MOSFET. This diode exhibits similar characteristics to a discrete external Schottky diode in parallel with a MOSFET. Figure 27 shows the reverse recovery characteristic of the FDPC8014AS.

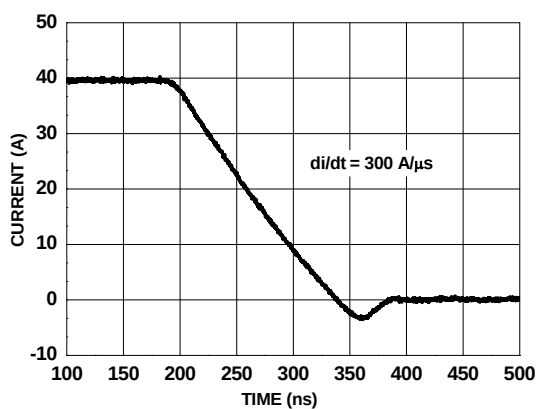


Figure 27. FDPC8014AS SyncFET™ Body Diode Reverse Recovery Characteristic

Schottky barrier diodes exhibit significant leakage at high temperature and high reverse voltage. This will increase the power in the device.

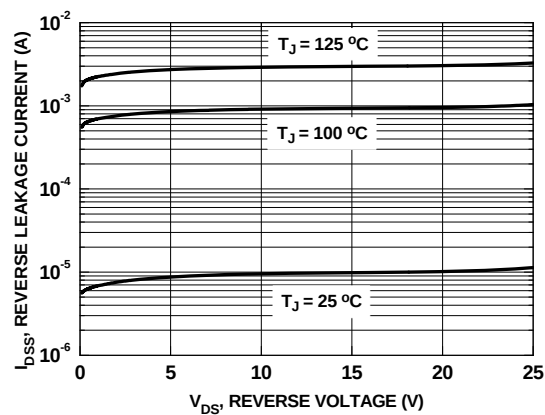
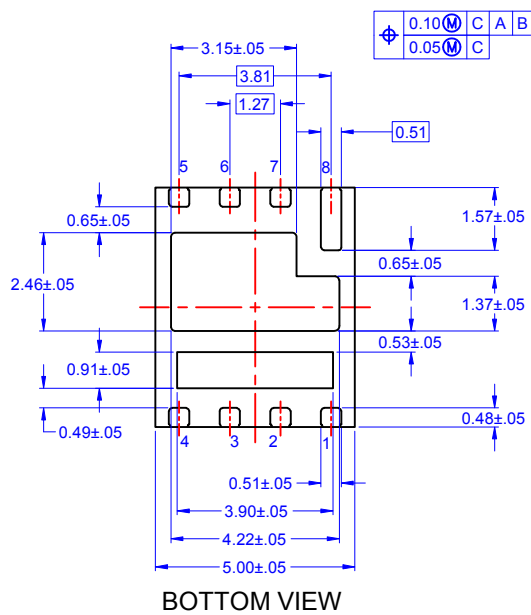
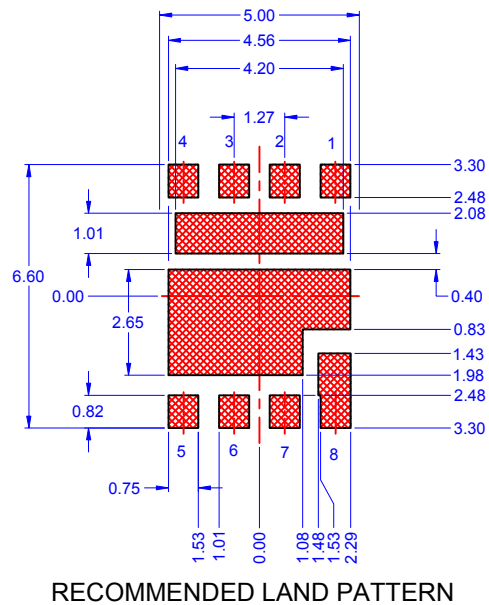
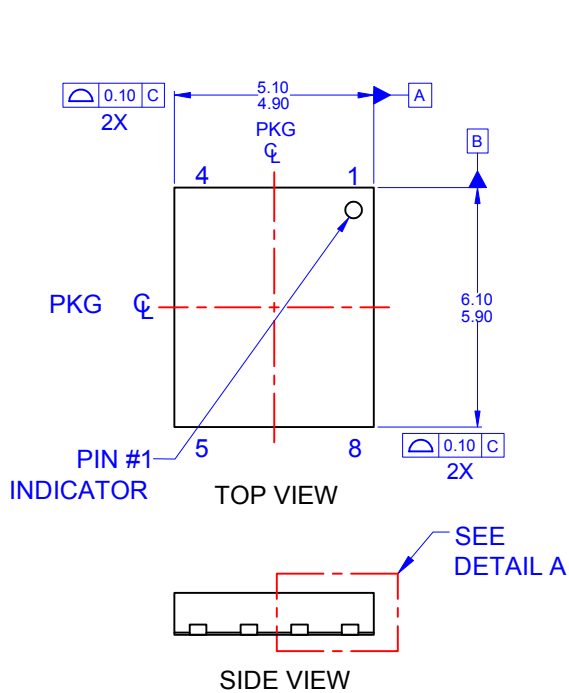
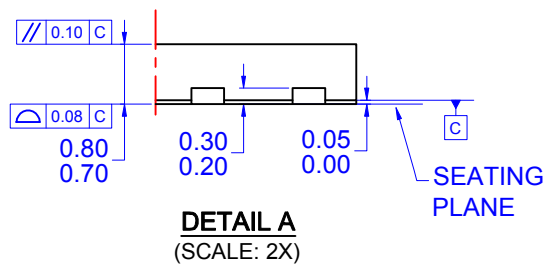


Figure 28. SyncFET™ Body Diode Reverse Leakage vs. Drain-source Voltage



NOTES: UNLESS OTHERWISE SPECIFIED

- A) DOES NOT FULLY CONFORM TO JEDEC REGISTRATION, MO-229, DATED 11/2001.
- B) ALL DIMENSIONS ARE IN MILLIMETERS.
- C) DIMENSIONS DO NOT INCLUDE BURRS OR MOLD FLASH. MOLD FLASH OR BURRS DOES NOT EXCEED 0.10MM.
- D) DIMENSIONING AND TOLERANCING PER ASME Y14.5M-1994.
- E) DRAWING FILE NAME: PQFN08KREV2



ON Semiconductor and  are trademarks of Semiconductor Components Industries, LLC dba ON Semiconductor or its subsidiaries in the United States and/or other countries. ON Semiconductor owns the rights to a number of patents, trademarks, copyrights, trade secrets, and other intellectual property. A listing of ON Semiconductor's product/patent coverage may be accessed at www.onsemi.com/site/pdf/Patent-Marking.pdf. ON Semiconductor reserves the right to make changes without further notice to any products herein. ON Semiconductor makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does ON Semiconductor assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. Buyer is responsible for its products and applications using ON Semiconductor products, including compliance with all laws, regulations and safety requirements or standards, regardless of any support or applications information provided by ON Semiconductor. "Typical" parameters which may be provided in ON Semiconductor data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals" must be validated for each customer application by customer's technical experts. ON Semiconductor does not convey any license under its patent rights nor the rights of others. ON Semiconductor products are not designed, intended, or authorized for use as a critical component in life support systems or any FDA Class 3 medical devices or medical devices with a same or similar classification in a foreign jurisdiction or any devices intended for implantation in the human body. Should Buyer purchase or use ON Semiconductor products for any such unintended or unauthorized application, Buyer shall indemnify and hold ON Semiconductor and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that ON Semiconductor was negligent regarding the design or manufacture of the part. ON Semiconductor is an Equal Opportunity/Affirmative Action Employer. This literature is subject to all applicable copyright laws and is not for resale in any manner.

PUBLICATION ORDERING INFORMATION

LITERATURE FULFILLMENT:

Literature Distribution Center for ON Semiconductor
19521 E. 32nd Pkwy, Aurora, Colorado 80011 USA
Phone: 303-675-2175 or 800-344-3860 Toll Free USA/Canada
Fax: 303-675-2176 or 800-344-3867 Toll Free USA/Canada
Email: orderlit@onsemi.com

N. American Technical Support: 800-282-9855 Toll Free
USA/Canada

Europe, Middle East and Africa Technical Support:
Phone: 421 33 790 2910

Japan Customer Focus Center
Phone: 81-3-5817-1050

ON Semiconductor Website: www.onsemi.com

Order Literature: <http://www.onsemi.com/orderlit>

For additional information, please contact your local
Sales Representative