CY7C1024AV33

128K x 24 Static RAM

Features

- **High speed**
  - **t_{AA} = 10 ns**
- **CMOS for optimum speed/power**
- **Center power/ground pinout**
- **Automatic power-down when deselected**
- **Easy memory expansion with CE1, CE2, CE3 and OE options**

Functional Description[1]

The CY7C1024AV33 is a high-performance CMOS static RAM organized as 131,072 words by 24 bits. Easy memory expansion is provided by an active LOW CE1, CE3, active HIGH CE2, an active LOW Output Enable (OE), and three-state drivers. This device has an automatic power-down feature that significantly reduces power consumption when deselected.

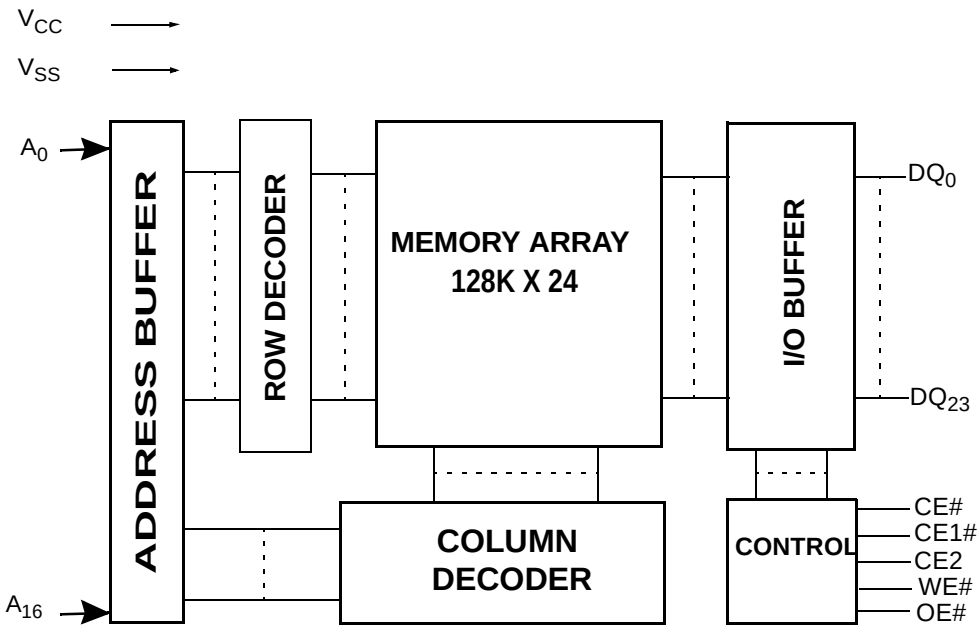
Writing to the device is accomplished by taking Chip Enable (CE1, CE2, CE3) active and Write Enable (WE) inputs LOW. Data on the 24 I/O pins (I/O_0 through I/O_{23}) is then written into the location specified on the address pins (A_0 through A_{16}).

Reading from the device is accomplished by taking Chip Enable (CE1, CE2, CE3) active and Output Enable (OE) LOW while forcing Write Enable (WE) HIGH. Under these conditions, the contents of the memory location specified by the address pins will appear on the I/O pins.

The 24 input/output pins (I/O_0 through I/O_{23}) are placed in a high-impedance state when the device is deselected (CE HIGH), the outputs are disabled (OE HIGH), or during a write operation (CE1, CE3 LOW, CE2 HIGH, and WE LOW).

The CY7C1024AV33 is available in a standard 119-ball BGA package and a 100-pin TQFP package.

Functional Block Diagram



Selection Guide

	7C1024AV33-10	7C1024AV33-12	7C1024AV33-15
Maximum Access Time (ns)	10	12	15
Maximum Operating Current (mA)	275	250	225
Maximum Standby Current (mA)	15	15	15

Note:

1. For guidelines on SRAM system design, please refer to the 'System Design Guidelines' Cypress application note, available on the internet at www.cypress.com.

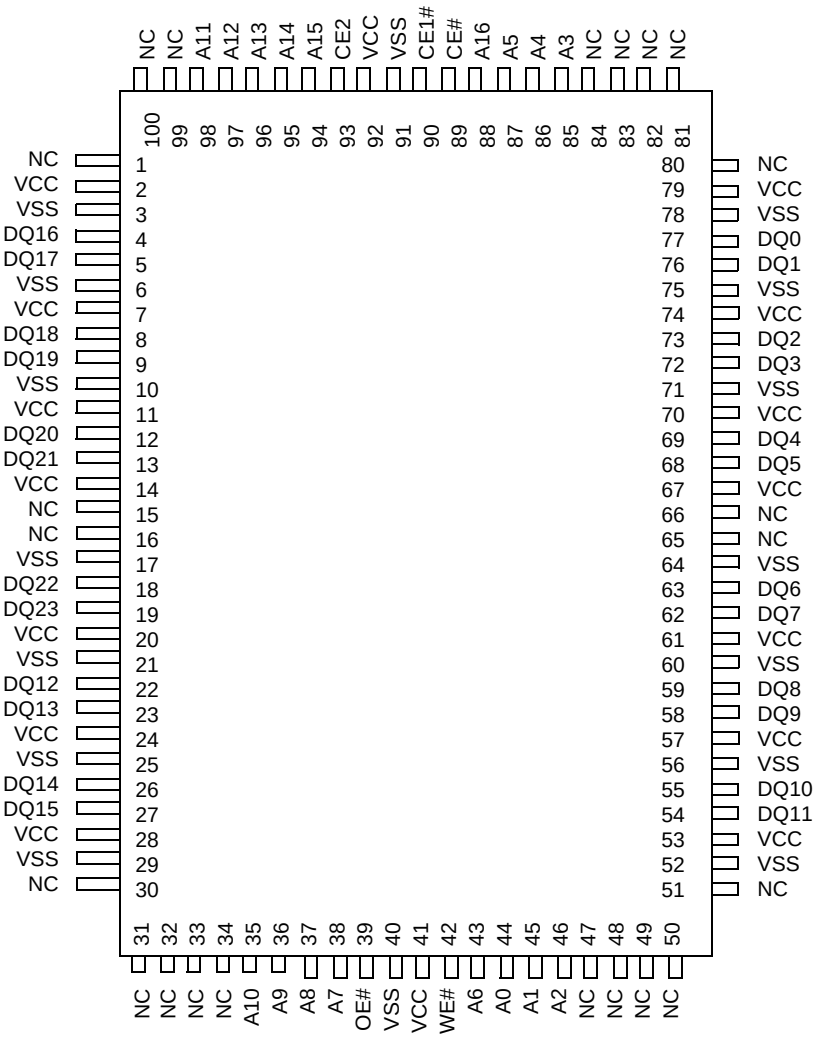
Pin Configurations

119 BGA
Top View

	1	2	3	4	5	6	7
A	NC	A	A	A	A	A	NC
B	NC	A	A	$\overline{CE1}$	A	A	NC
C	DQ	NC	CE2	NC	$\overline{CE3}$	NC	DQ
D	DQ	V_{CC}	V_{SS}	V_{SS}	V_{SS}	V_{CC}	DQ
E	DQ	V_{SS}	V_{CC}	V_{SS}	V_{CC}	V_{SS}	DQ
F	DQ	V_{CC}	V_{SS}	V_{SS}	V_{SS}	V_{CC}	DQ
G	DQ	V_{SS}	V_{CC}	V_{SS}	V_{CC}	V_{SS}	DQ
H	DQ	V_{CC}	V_{SS}	V_{SS}	V_{SS}	V_{CC}	DQ
J	NC	V_{SS}	V_{CC}	V_{SS}	V_{CC}	V_{SS}	NC
K	DQ	V_{CC}	V_{SS}	V_{SS}	V_{SS}	V_{CC}	DQ
L	DQ	V_{SS}	V_{CC}	V_{SS}	V_{CC}	V_{SS}	DQ
M	DQ	V_{CC}	V_{SS}	V_{SS}	V_{SS}	V_{CC}	DQ
N	DQ	V_{SS}	V_{CC}	V_{SS}	V_{CC}	V_{SS}	DQ
P	DQ	V_{CC}	V_{SS}	V_{SS}	V_{SS}	V_{CC}	DQ
R	DQ	NC	NC	NC	NC	NC	DQ
T	NC	A	A	$\overline{WE}$	A	A	NC
U	NC	A	A	$\overline{OE}$	A	A	NC

Pin Configurations (continued)

100-pin TQFP
Top View



Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature ..... –65°C to +150°C

Ambient Temperature with Power Applied..... –55°C to +125°C

Supply Voltage on V_{CC} to Relative GND[2] .... –0.5V to +7.0V

DC Voltage Applied to Outputs in High Z State[2] ..... –0.5V to V_{CC} + 0.5V

DC Input Voltage[2]..... –0.5V to V_{CC} + 0.5V

Current into Outputs (LOW) ..... 20 mA

Static Discharge Voltage..... >2001V (per MIL-STD-883, Method 3015)

Latch-Up Current..... >200 mA

Operating Range

Range	Ambient Temperature	V_{CC}
Commercial	0°C to +70°C	3.3V ±10%
Industrial	–40°C to +85°C	3.3V ±10%

Note:
2. Minimum Voltage is = –2.0V for pulse durations of less than 20 ns.

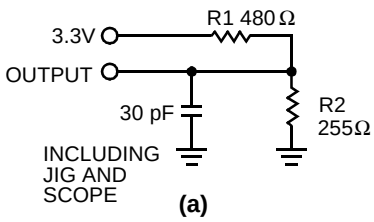
Electrical Characteristics Over the Operating Range

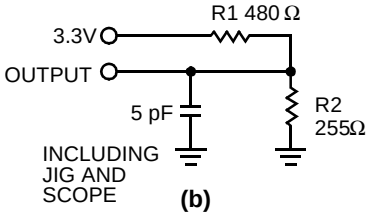
Parameter	Description	Test Conditions[3]	1024AV33-10		1024AV33-12		1024AV33-15		Unit
			Min.	Max.	Min.	Max.	Min.	Max.	
V_{OH}	Output HIGH Voltage	V_{CC} = Min., I_{OH} = –4.0 mA	2.4		2.4		2.4		V
V_{OL}	Output LOW Voltage	V_{CC} = Min., I_{OL} = 8.0 mA		0.4		0.4		0.4	V
V_{IH}	Input HIGH Voltage		2.2	V_{CC} + 0.3	2.2	V_{CC} + 0.3	2.2	V_{CC} + 0.3	V
V_{IL}	Input LOW Voltage[2]		–0.3	0.8	–0.3	0.8	–0.3	0.8	V
I_{IX}	Input Load Current	GND ≤ V_I ≤ V_{CC}	–3	+3	–3	+3	–3	+3	µA
I_{OZ}	Output Leakage Current	GND ≤ V_I ≤ V_{CC}, Output Disabled	–5	+5	–5	+5	–5	+5	µA
I_{CC}	V_{CC} Operating Supply Current	V_{CC} = Max., I_{OUT} = 0 mA, f = f_{MAX} = $1/t_{RC}$		275		250		225	mA
I_{SB1}	Automatic CE Power-Down Current —TTL Inputs	Max. V_{CC}, $\overline{CE}$ ≥ V_{IH} V_{IN} ≥ V_{IH} or V_{IN} ≤ V_{IL}, f = f_{MAX}		60		60		60	mA
I_{SB2}	Automatic CE Power-Down Current —CMOS Inputs	Max. V_{CC}, $\overline{CE}$ ≥ V_{CC} – 0.3V, V_{IN} ≥ V_{CC} – 0.3V, or V_{IN} ≤ 0.3V, f = 0		15		15		15	mA

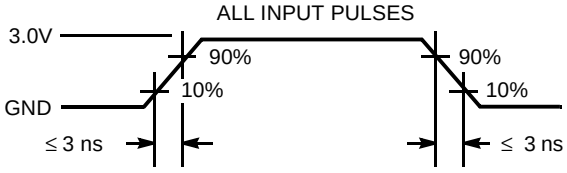
Capacitance[4]

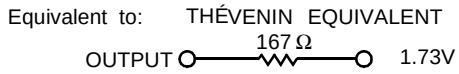
Parameter	Description	Test Conditions	Max.	Unit
C_{IN}	Input Capacitance	T_A = 25°C, f = 1 MHz, V_{CC} = 3.3V	10	pF
C_{OUT}	Output Capacitance		8	pF

AC Test Loads and Waveforms









Notes:
3. CE is a combination of $\overline{CE1}$, CE2, and $\overline{CE3}$
4. Tested initially and after any design or process changes that may affect these parameters.

Switching Characteristics[5] Over the Operating Range

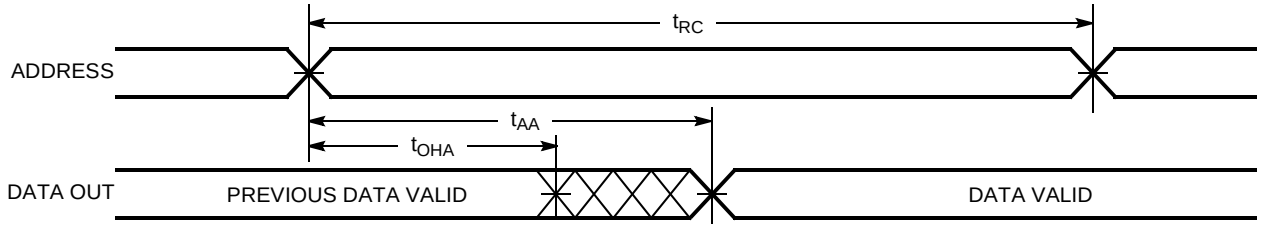
Parameter	Description[3]	7C1024AV33-10		7C1024AV33-12		7C1024AV33-15		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
READ CYCLE								
t_{RC}	Read Cycle Time	10		12		15		ns
t_{AA}	Address to Data Valid		10		12		15	ns
t_{OHA}	Data Hold from Address Change	3		3		3		ns
t_{ACE}	$\overline{CE}$ active to Data Valid		10		12		15	ns
t_{DOE}	$\overline{OE}$ LOW to Data Valid		5		6		7	ns
t_{LZOE}	$\overline{OE}$ LOW to Low Z	0		0		0		ns
t_{HZOE}	$\overline{OE}$ HIGH to High Z[6, 7]		5		6		6	ns
t_{LZCE}	$\overline{CE}$ active to Low Z[7]	3		3		3		ns
t_{HZCE}	$\overline{CE}$ inactive to High Z[6, 7]		5		6		6	ns
t_{PU}	$\overline{CE}$ active to Power-Up	0		0		0		ns
t_{PD}	$\overline{CE}$ inactive to Power-Down		10		12		15	ns
WRITE CYCLE[8, 9]								
t_{WC}	Write Cycle Time	10		12		15		ns
t_{SCE}	$\overline{CE}$ active to Write End	8		9		9		ns
t_{AW}	Address Set-Up to Write End	7		8		8		ns
t_{HA}	Address Hold from Write End	0		0		0		ns
t_{SA}	Address Set-Up to Write Start	0		0		0		ns
t_{PWE}	$\overline{WE}$ Pulse Width	7		8		8		ns
t_{SD}	Data Set-Up to Write End	5		6		6		ns
t_{HD}	Data Hold from Write End	0		0		0		ns
t_{LZWE}	$\overline{WE}$ HIGH to Low Z[7]	3		3		3		ns
t_{HZWE}	$\overline{WE}$ LOW to High Z[6, 7]		5		6		6	ns

Notes:

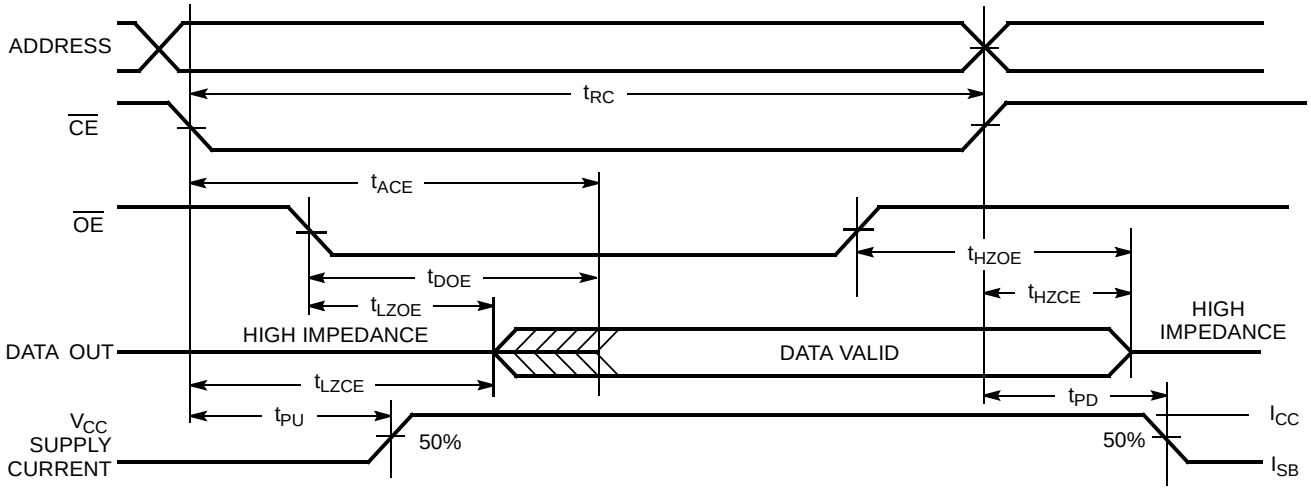
5. Test conditions assume signal transition time of 3 ns or less, timing reference levels of 1.5V, input pulse levels of 0 to 3.0V, and output loading of the specified I_{OL}/I_{OH} and 30-pF load capacitance.
6. t_{HZOE}, t_{HZCE}, and t_{HZWE} are specified with a load capacitance of 5 pF as in part (b) of AC Test Loads. Transition is measured ±500 mV from steady-state voltage.
7. At any given temperature and voltage condition, t_{HZCE} is less than t_{LZCE}, t_{HZOE} is less than t_{LZOE}, and t_{HZWE} is less than t_{LZWE} for any given device.
8. The internal write time of the memory is defined by the overlap of CE LOW and WE LOW. CE and WE must be LOW to initiate a write, and the transition of any of these signals can terminate the write. The input data set-up and hold timing should be referenced to the leading edge of the signal that terminates the write.
9. The minimum write cycle time for Write Cycle no. 3 (WE controlled, OE LOW) is the sum of t_{HZWE} and t_{SD}.

Switching Waveforms

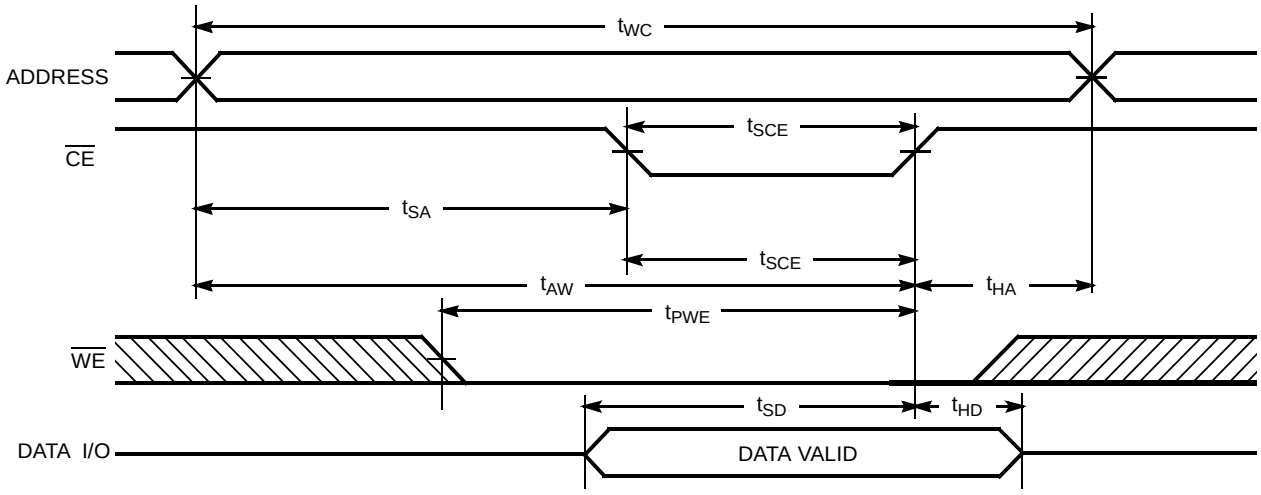
Read Cycle No. 1[10, 11]



Read Cycle No. 2 ($\overline{OE}$ Controlled)[3, 11, 12]



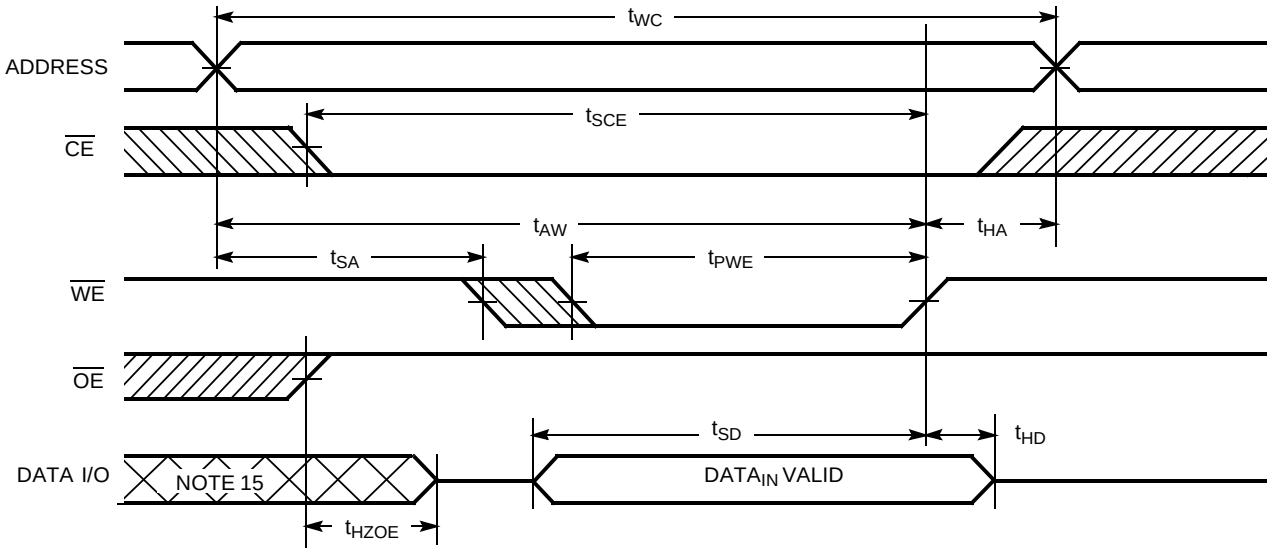
Write Cycle No. 1 ($\overline{CE}$ Controlled)[3, 13, 14]



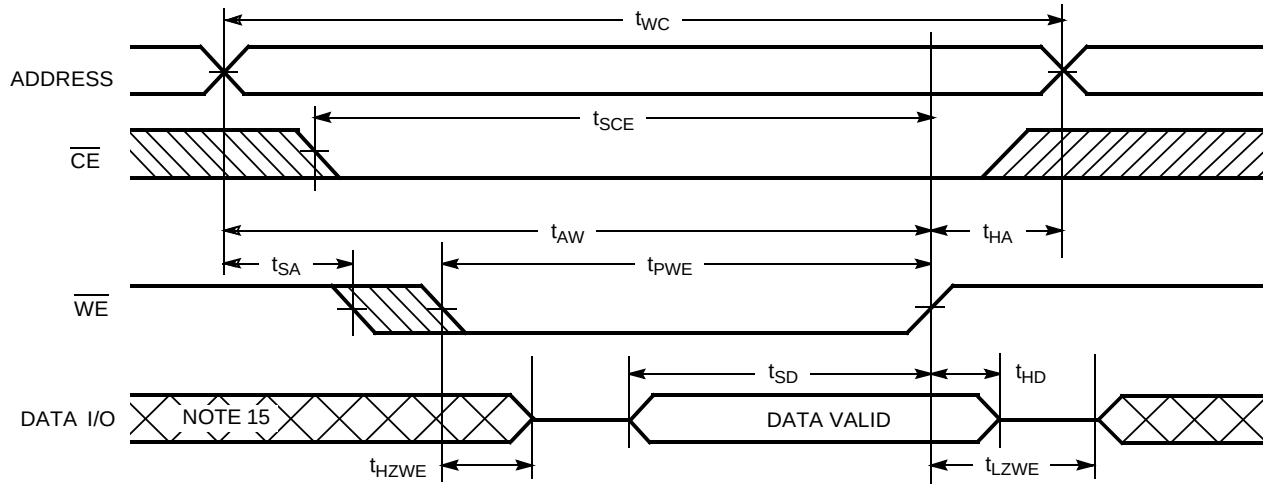
Notes:
10. Device is continuously selected. $\overline{OE}$, $\overline{CE}$ = V_{IL}.
11. $\overline{WE}$ is HIGH for read cycle.
12. Address valid prior to or coincident with $\overline{CE}$ transition LOW.
13. Data I/O is high impedance if $\overline{OE}$ = V_{IH}.
14. If $\overline{CE}$ goes HIGH simultaneously with $\overline{WE}$ going HIGH, the output remains in a high-impedance state.

Switching Waveforms (continued)

Write Cycle No. 2 ($\overline{WE}$ Controlled, $\overline{OE}$ HIGH During Write)[13, 14]



Write Cycle No. 3 ($\overline{WE}$ Controlled, $\overline{OE}$ LOW)[3, 14]



Note:

15. During this period the I/Os are in the output state and input signals should not be applied.

Truth Table

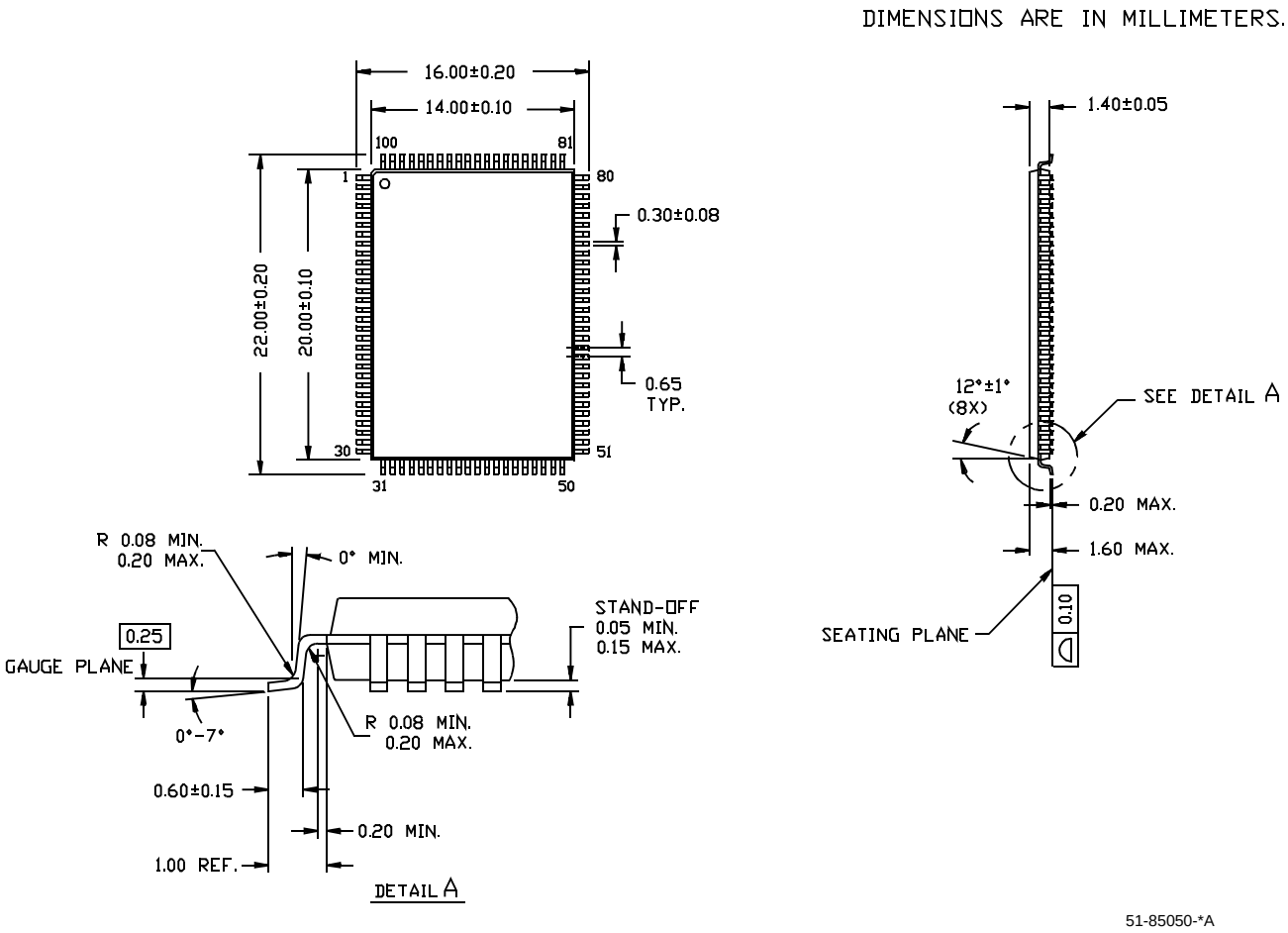
$\overline{CE1}$	CE2	$\overline{CE3}$	$\overline{OE}$	$\overline{WE}$	I/O_0–I/O_{23}	Mode	Power
H	X	X	X	X	High Z	Power-Down	Standby (I_{SB})
X	L	X	X	X	High Z	Power-Down	Standby (I_{SB})
X	X	H	X	X	High Z	Power-Down	Standby (I_{SB})
L	H	L	L	H	Data Out	Read	Active (I_{CC})
L	H	L	X	L	Data In	Write	Active (I_{CC})
L	H	L	H	H	High Z	Selected, Outputs Disabled	Active (I_{CC})

Ordering Information

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
10	CY7C1024AV33-10AC	A101	100-Pin Thin Plastic Quad Flatpack (14 x 20 x 1.4 mm)	Commercial
	CY7C1024AV33-10BGC	BG119	119-Ball PBGA	
12	CY7C1024AV33-12AC	A101	100-Pin Thin Plastic Quad Flatpack (14 x 20 x 1.4 mm)	
	CY7C1024AV33-12BGC	BG119	119-Ball PBGA	
	CY7C1024AV33-12BGI	BG119	119-Ball PBGA	Industrial
15	CY7C1024AV33-15AC	A101	100-Pin Thin Plastic Quad Flatpack (14 x 20 x 1.4 mm)	Commercial
	CY7C1024AV33-15BGC	BG119	119-Ball PBGA	
	CY7C1024AV33-15BGI	BG119	119-Ball PBGA	Industrial

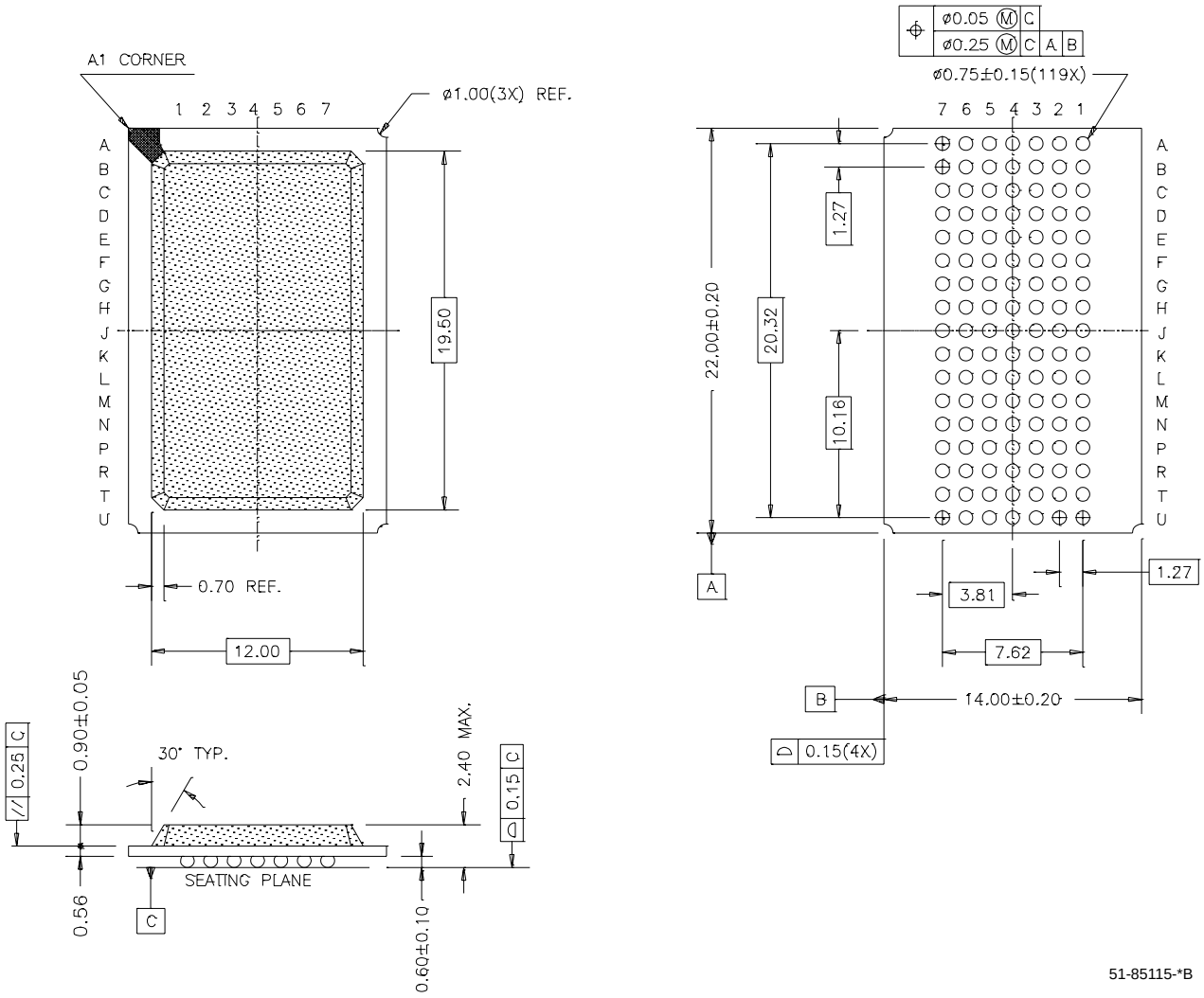
Package Diagrams

100-Pin Thin Plastic Quad Flatpack (14 x 20 x 1.4 mm) A101



Package Diagrams (continued)

119-Lead PBGA (14 x 22 x 2.4 mm) BG119



Document History Page

Document Title: CY7C1024AV33 128K x 24 Static RAM Document Number: 38-05149				
REV.	**ECN NO.**	**Issue Date**	**Orig. of Change**	**Description of Change**
**	109893	09/22/01	SZV	Change from Spec number: 38-00983 to 38-05149
*A	116473	09/16/02	CEA	Add applications foot note to data sheet, page 1.
*B	121472	11/14/02	DSG	Update package diagram 51-85115 (BG119) to rev. *B