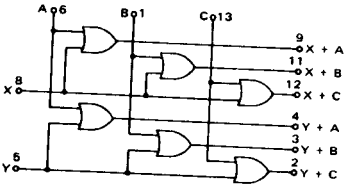
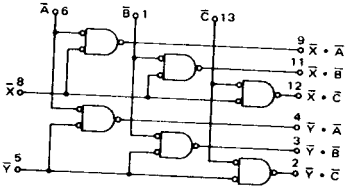
MC1029
MC1229

A 2 X 3 array of 2-input OR gates, designed primarily for the handling of data in a digital system.

POSITIVE LOGIC



NEGATIVE LOGIC

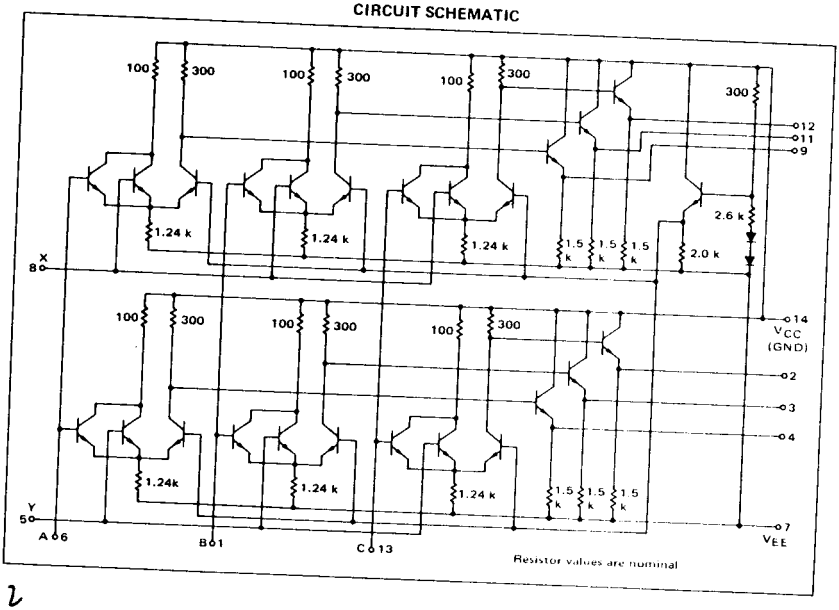


DC Input Loading Factors: X, Y = 3; A, B, C = 2
DC Output Loading Factor = 25
Power Dissipation = 160 mW typical

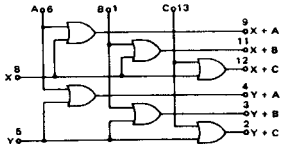
TRUTH TABLE (POSITIVE LOGIC)

X	Y	A	B	C	PIN NUMBER 9	11	12	4	3	2
0	0	0	0	0	0	0	0	0	0	0
0	0	0	0	1	0	0	0	0	0	1
0	0	0	1	0	0	0	0	0	1	0
0	0	0	1	1	0	0	0	0	1	0
0	0	1	0	0	0	0	0	1	0	0
0	0	1	0	1	0	0	0	1	0	0
0	0	1	1	0	0	0	0	1	0	0
0	0	1	1	1	0	0	0	1	0	0
0	1	0	0	0	0	0	1	0	0	0
0	1	0	0	1	0	0	1	0	0	0
0	1	0	1	0	0	0	1	0	0	0
0	1	0	1	1	0	0	1	0	0	0
0	1	1	0	0	0	0	1	0	0	0
0	1	1	0	1	0	0	1	0	0	0
0	1	1	1	0	0	0	1	0	0	0
0	1	1	1	1	0	0	1	0	0	0
1	0	0	0	0	0	1	0	0	0	0
1	0	0	0	1	0	1	0	0	0	0
1	0	0	1	0	0	1	0	0	0	0
1	0	0	1	1	0	1	0	0	0	0
1	0	1	0	0	0	1	0	0	0	0
1	0	1	0	1	0	1	0	0	0	0
1	0	1	1	0	0	1	0	0	0	0
1	0	1	1	1	0	1	0	0	0	0
1	1	0	0	0	1	0	0	0	0	0
1	1	0	0	1	1	0	0	0	0	0
1	1	0	1	0	1	0	0	0	0	0
1	1	0	1	1	1	0	0	0	0	0
1	1	1	0	0	1	0	0	0	0	0
1	1	1	0	1	1	0	0	0	0	0
1	1	1	1	0	1	0	0	0	0	0
1	1	1	1	1	1	0	0	0	0	0

CIRCUIT SCHEMATIC



Resistor values are nominal

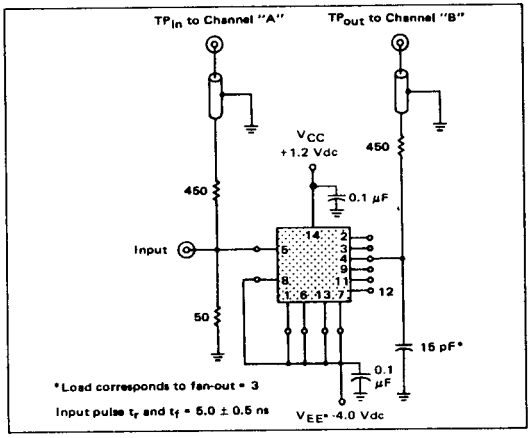


ELECTRICAL CHARACTERISTICS

Characteristic	Symbol	Pin Under Test	MC1229 Test Limits −55°C Min	−55°C Max	+25°C Min	+25°C Max	+125°C Min	+125°C Max	Unit	MC1029 Test Limits 0°C Min	0°C Max	+25°C Min	+25°C Max	+75°C Min	+75°C Max	Unit
Power Supply Drain Current	I_E	7	-	-	-	36	-	-	mAdc	-	-	-	45	-	-	mAdc
Input Current	I_{in}	5	-	-	-	300	-	-	μAdc	-	-	-	300	-	-	μAdc
		8	-	-	-	300	-	-		-	-	-	300	-	-	
		1	-	-	-	200	-	-		-	-	-	200	-	-	
		6	-	-	-	200	-	-		-	-	-	200	-	-	
		13	-	-	-	200	-	-		-	-	-	200	-	-	
Input Leakage Current	I_R	5, 8*	-	-	-	0.6	-	3.0	μAdc	-	-	-	0.6	-	3.0	μAdc
		1, 6, 13*	-	-	-	0.4	-	2.0	μAdc	-	-	-	0.4	-	2.0	μAdc
Logical "1" Output Voltage	V_{OH}‡	3, 11† 4, 9† 2, 12† 2, 3, 4† 9, 11, 12†	-0.990	-0.825	-0.850	-0.700	-0.700	-0.530	Vdc	-0.895	-0.740	-0.850	-0.700	-0.775	-0.615	Vdc
Logical "0" Output Voltage	V_{OL}	3, 11† 4, 9† 2, 12† 2, 3, 4† 9, 11, 12†	-1.890	-1.580	-1.800	-1.500	-1.720	-1.380	Vdc	-1.830	-1.525	-1.800	-1.500	-1.760	-1.435	Vdc
Switching Times			Typ	Max	Typ	Max	Typ	Max		Typ	Max	Typ	Max	Typ	Max	
Propagation Delay	t_{5+4+}	4	4.0	7.5	4.0	7.5	6.0	9.0	ns	4.0	7.5	4.0	7.5	5.0	8.0	ns
	t_{5-4-}		4.0	7.5	4.0	7.5	6.0	9.0		4.0	7.5	4.0	7.5	5.0	8.0	
Rise Time	t_{4+}		5.0	8.5	5.0	8.5	7.0	9.5		5.0	8.5	5.0	8.5	6.0	9.0	
Fall Time	t_{4-}		5.0	8.0	5.0	8.0	7.0	9.0		5.0	8.0	5.0	8.0	6.0	8.5	
Propagation Delay	t_{1+3+}	3	4.0	7.5	4.0	7.5	6.0			4.0	7.5	4.0	7.5	5.0	8.0	
	t_{1-3-}		4.0	7.5	4.0	7.5	6.0			4.0	7.5	4.0	7.5	5.0	8.0	
Rise Time	t_{3+}		5.0	8.5	5.0	8.5	7.0	9.5		5.0	8.5	5.0	8.5	6.0	9.0	
Fall Time	t_{3-}		5.0	8.0	5.0	8.0	7.0	9.0		5.0	8.0	5.0	8.0	6.0	8.5	

* Individually test each input using the pin connections shown. † Individually test each output using the pin connections shown.

SWITCHING TIME TEST CIRCUIT @ 25°C



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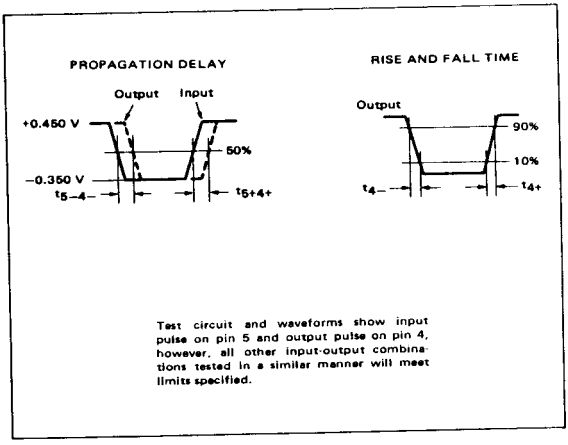
@Test Temperature		TEST VOLTAGE/CURRENT VALUES Vdc ±1.0% $V_{IL\ min}$ to $V_{IL\ max}$	$V_{IH\ min}$ to $V_{IH\ max}$	$V_{IH\ max}$	V_{EE}	mAdc I_L
MC1229	−55°C	-5.2 to -1.405	-1.165 to -0.825	-	-5.2	-2.5
	+25°C	-5.2 to -1.325	-1.025 to -0.700	-0.700	-5.2	-2.5
	+125°C	-5.2 to -1.205	-0.875 to -0.530	-	-5.2	-2.5
MC1029	0°C	-5.2 to -1.350	-1.070 to -0.740	-	-5.2	-2.5
	+25°C	-5.2 to -1.325	-1.025 to -0.700	-0.700	-5.2	-2.5
	+75°C	-5.2 to -1.260	-0.950 to -0.615	-	-5.2	-2.5

Characteristic	Symbol	Pin Under Test	TEST VOLTAGE/CURRENT APPLIED TO PINS LISTED BELOW: $V_{IL\ min}$ to $V_{IL\ max}$	$V_{IH\ min}$ to $V_{IH\ max}$	$V_{IH\ max}$	V_{EE}	I_L	V_{CC} (Gnd)
Power Supply Drain Current	I_E	7	-	-	-	1, 5, 6, 7, 8, 13	-	14
Input Current	I_{in}	5	-	-	5	1, 6, 7, 8, 13	-	14
		8	-	-	8	1, 5, 6, 7, 13	-	↓
		1	-	-	1	5, 6, 7, 8, 13	-	
		6	-	-	6	1, 5, 7, 8, 13	-	
		13	-	-	13	1, 5, 6, 7, 8	-	
Input Leakage Current	I_R	5, 8*	-	-	-	1, 5, 6, 7, 8, 13	-	14
		1, 6, 13*	-	-	-	1, 5, 6, 7, 8, 13	-	14
Logical "1" Output Voltage	V_{OH}‡	3, 11†	-	1	-	5, 6, 7, 8, 13	‡	14
		4, 9†	-	6	-	1, 5, 7, 8, 13	↓	↓
		2, 12†	-	13	-	1, 5, 6, 7, 8		
		2, 3, 4†	-	5	-	1, 6, 7, 8, 13		
		9, 11, 12†	-	8	-	1, 5, 6, 7, 13		
Logical "0" Output Voltage	V_{OL}	3, 11†	1	-	-	5, 6, 7, 8, 13	-	14
		4, 9†	6	-	-	1, 5, 7, 8, 13	-	↓
		2, 12†	13	-	-	1, 5, 6, 7, 8	-	
		2, 3, 4†	5	-	-	1, 6, 7, 8, 13	-	
		9, 11, 12†	8	-	-	1, 5, 6, 7, 13	-	
Switching Times			Pulse In	Pulse Out		V_{EE} = −4.0 Vdc		(+1.2 V)
Propagation Delay	t_{5+4+}	4	5	4	-	1, 6, 7, 8, 13	-	14
	t_{5-4-}	↓	↓	↓		↓		↓
Rise Time	t_{4+}							
Fall Time	t_{4-}							
Propagation Delay	t_{1+3+}	3	1	3	-	5, 6, 7, 8, 13	-	
	t_{1-3-}	↓	↓	↓		↓		
Rise Time	t_{3+}							
Fall Time	t_{3-}							

‡V_{OH} limits apply from no load (0 mA) to full load (-2.5 mA). I_L applied to output under test.



Test circuit and waveforms show input pulse on pin 5 and output pulse on pin 4, however, all other input-output combinations tested in a similar manner will meet limits specified.

SWITCHING TIME WAVEFORMS

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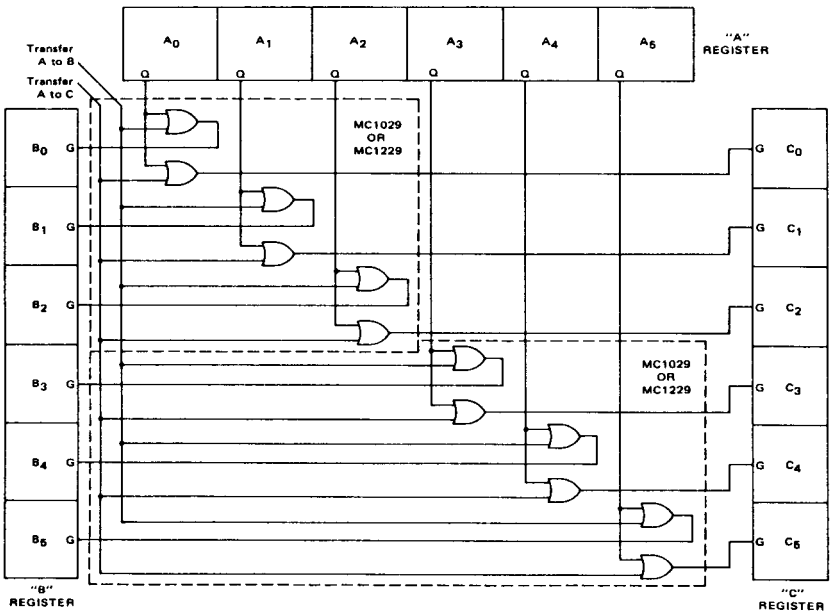
APPLICATIONS INFORMATION

The MC1029/MC1229 data distributor is a 2 X 3 array of 2-input OR gates, as shown in the logic diagram. Inputs X and Y may be used as control inputs to transfer the data on inputs A, B, and C, to the outputs on pins 9, 11, and 12, or to the outputs on pins 4, 3, and 2. Also, if it is desired to distribute data to three destinations, inputs X and Y may be used for data and A, B, and C as control inputs. The data distributor utilizes negative logic; i.e., the positive OR function becomes the negative AND. Data is transferred for a low level on the control inputs.

The data distributor is an example of the manner in which part of a logic system may be partitioned to reduce wiring and package count. Figure 1 illustrates the logic required for the transfer of data from "A" register to "B" register gating or to "C" register gating. Six stages per register are shown in the figure but arrays of any desired length may be built. The typical propagation delay of the data distributor in a system is 5.0 ns, permitting the rapid transfer of data through distribution gating. If data distribution is done on a double-rail basis instead of single-rail as shown, then twice the number of data distributors are required.

FIGURE 1 – REGISTER DATA TRANSFER



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