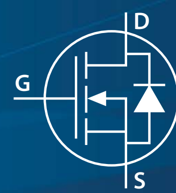
EPC2045 – Enhancement Mode Power Transistor

V_{DS} , 100 V
$R_{DS(on)}$, 7 mΩ
I_D , 16 A



EFFICIENT POWER CONVERSION

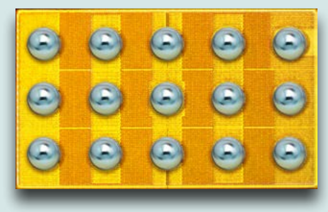
RoHS Halogen-Free

Gallium Nitride's exceptionally high electron mobility and low temperature coefficient allows very low $R_{DS(on)}$, while its lateral device structure and majority carrier diode provide exceptionally low Q_G and zero Q_{RR}. The end result is a device that can handle tasks where very high switching frequency, and low on-time are beneficial as well as those where on-state losses dominate.

Maximum Ratings				
PARAMETER		VALUE	UNIT
V_{DS}	Drain-to-Source Voltage (Continuous)	100	V
	Drain-to-Source Voltage (up to 10,000 5 ms pulses at 150°C)	120	
I_D	Continuous (T_A = 25°C)	16	A
	Pulsed (25°C, T_{PULSE} = 300 µs)	130	
V_{GS}	Gate-to-Source Voltage	6	V
	Gate-to-Source Voltage	-4	
T_J	Operating Temperature	-40 to 150	°C
T_{STG}	Storage Temperature	-40 to 150	

Thermal Characteristics			
PARAMETER		TYP	UNIT
$R_{\theta JC}$	Thermal Resistance, Junction-to-Case	1.4	°C/W
$R_{\theta JB}$	Thermal Resistance, Junction-to-Board	8.5	
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient (Note 1)	64	

Note 1: $R_{\theta JA}$ is determined with the device mounted on one square inch of copper pad, single layer 2 oz copper on FR4 board.
See https://epc-co.com/epc/documents/product-training/Appnote_Thermal_Performance_of_eGaN_FETs.pdf for details.



EPC2045 eGaN® FETs are supplied passivated die form with solder bumps
Die size: 2.5 mm x 1.5 mm

Applications
- Open Rack Server Architectures
- Lidar/Pulsed Power Applications
- USB-C
- Isolated Power Supplies
- Point of Load Converters
- Class D Audio
- LED Lighting
- Low Inductance Motor Drive

Benefits
- Ultra High Efficiency
- No Reverse Recovery
- Ultra Low Q_G
- Ultra Small Footprint

Static Characteristics (T_J = 25°C unless otherwise stated)						
PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
BV_{DSS}	Drain-to-Source Voltage	V_{GS} = 0 V, I_D = 300 µA	100			V
I_{DSS}	Drain-Source Leakage	V_{GS} = 0 V, V_{DS} = 80 V		40	250	µA
I_{GSS}	Gate-to-Source Forward Leakage	V_{GS} = 5 V, T_J = 25°C		0.01	1.3	mA
	Gate-to-Source Forward Leakage#	V_{GS} = 5 V, T_J = 125°C		0.1	5	mA
	Gate-to-Source Reverse Leakage	V_{GS} = -4 V		40	500	µA
$V_{GS(TH)}$	Gate Threshold Voltage	V_{DS} = V_{GS}, I_D = 5 mA	0.8	1.4	2.5	V
$R_{DS(on)}$	Drain-Source On Resistance	V_{GS} = 5 V, I_D = 16 A		5.6	7	mΩ
V_{SD}	Source-Drain Forward Voltage	I_S = 0.5 A, V_{GS} = 0 V		1.7		V

Defined by design. Not subject to production test.

Dynamic Characteristics (T_J = 25°C unless otherwise stated)						
PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
C_{ISS}	Input Capacitance#	V_{DS} = 50 V, V_{GS} = 0 V		767	1016	pF
C_{RSS}	Reverse Transfer Capacitance			3		
C_{OSS}	Output Capacitance#			295	443	
$C_{OSS(ER)}$	Effective Output Capacitance, Energy Related (Note 2)	V_{DS} = 0 to 50 V, V_{GS} = 0 V		383		
$C_{OSS(TR)}$	Effective Output Capacitance, Time Related (Note 3)			500		
R_G	Gate Resistance			0.6		Ω
Q_G	Total Gate Charge#	V_{DS} = 50 V, V_{GS} = 5 V, I_D = 16 A		6	7.8	nC
Q_{GS}	Gate-to-Source Charge	V_{DS} = 50 V, I_D = 16 A		1.9		
Q_{GD}	Gate-to-Drain Charge			0.8		
$Q_{G(TH)}$	Gate Charge at Threshold			1.3		
Q_{OSS}	Output Charge#	V_{DS} = 50 V, V_{GS} = 0 V		25	38	
Q_{RR}	Source-Drain Recovery Charge			0		

Defined by design. Not subject to production test.
Note 2: $C_{OSS(ER)}$ is a fixed capacitance that gives the same stored energy as C_{OSS} while V_{DS} is rising from 0 to 50% BV_{DSS}.
Note 3: $C_{OSS(TR)}$ is a fixed capacitance that gives the same charging time as C_{OSS} while V_{DS} is rising from 0 to 50% BV_{DSS}.

Figure 1: Typical Output Characteristics at 25°C

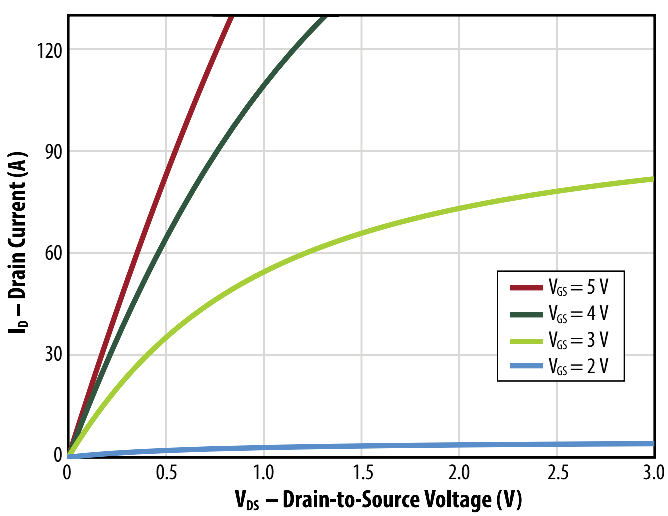


Figure 2: Transfer Characteristics

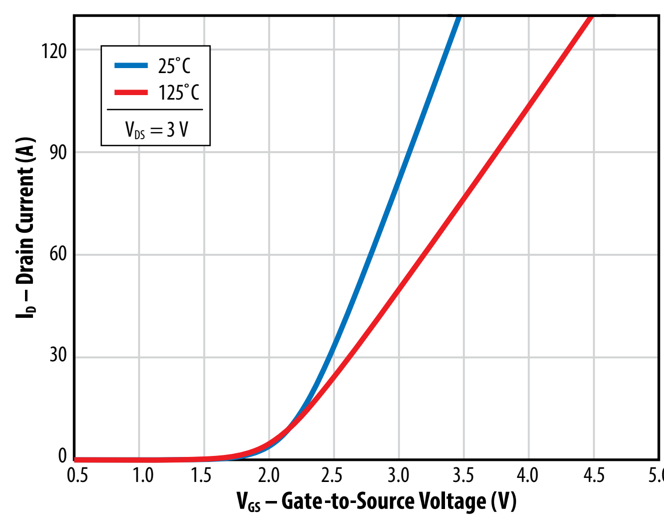


Figure 3: $R_{DS(on)}$ vs. V_{GS} for Various Drain Currents

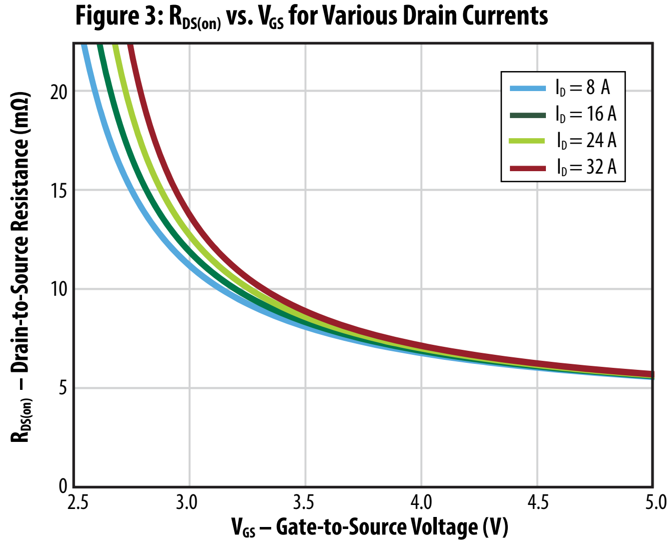


Figure 4: $R_{DS(on)}$ vs. V_{GS} for Various Temperatures

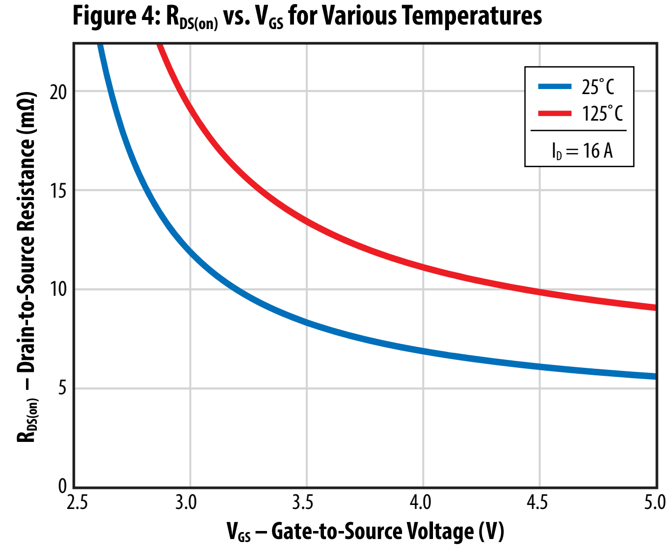


Figure 5a: Capacitance (Linear Scale)

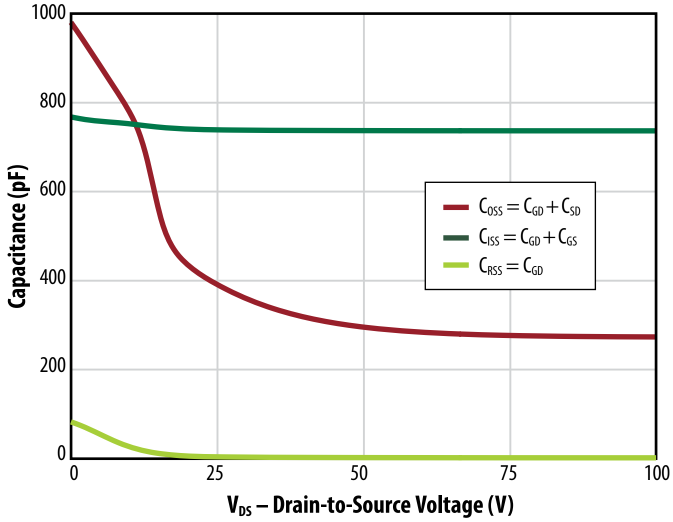


Figure 5b: Capacitance (Log Scale)

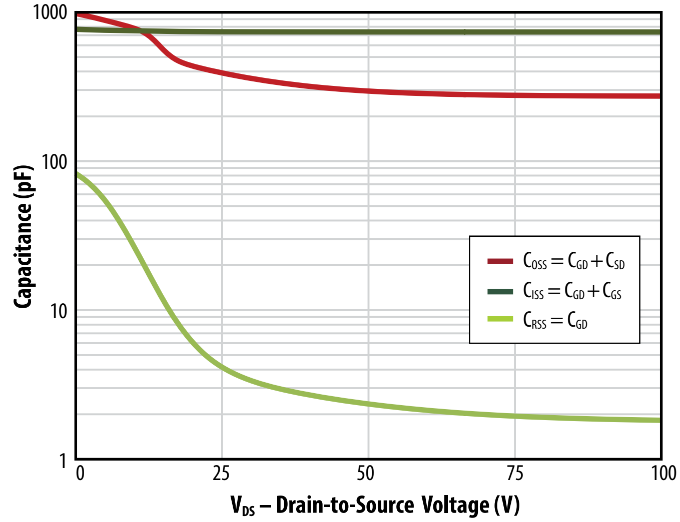


Figure 6: Output Charge and C_{OSS} Stored Energy

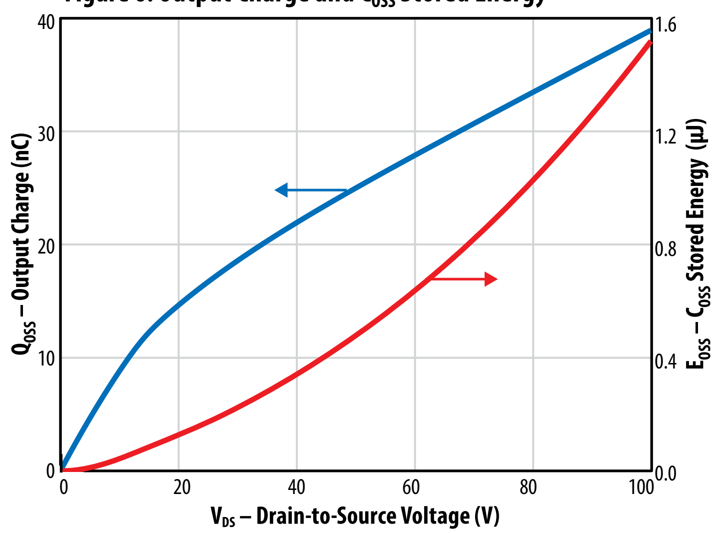


Figure 7: Gate Charge

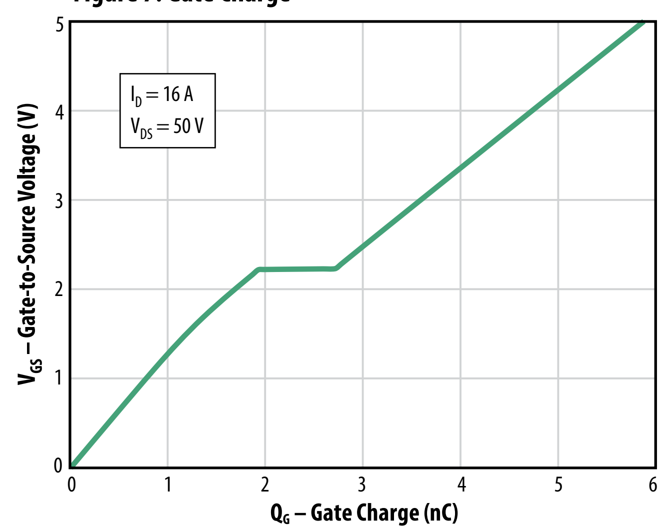


Figure 8: Reverse Drain-Source Characteristics

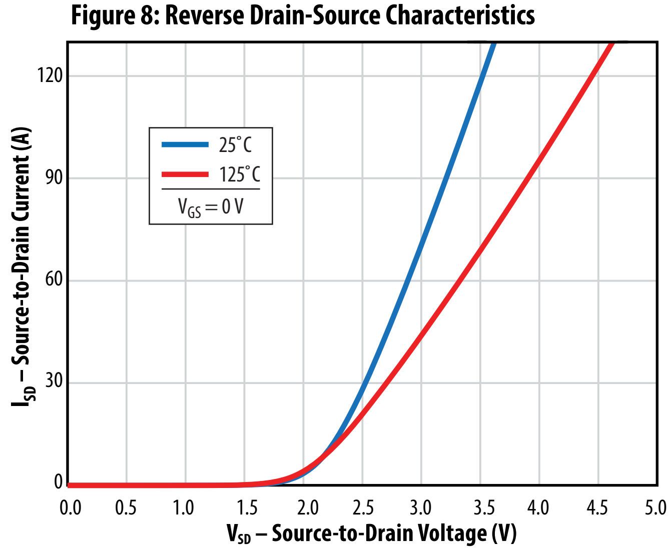


Figure 9: Normalized On-State Resistance vs. Temperature

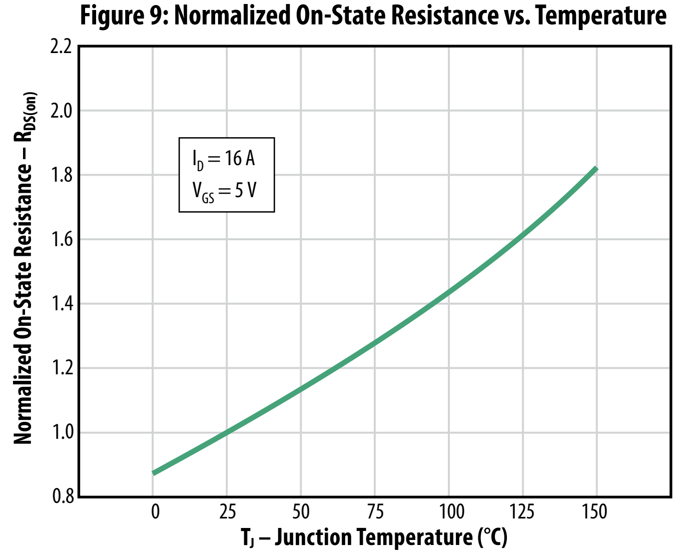


Figure 10: Normalized Threshold Voltage vs. Temperature

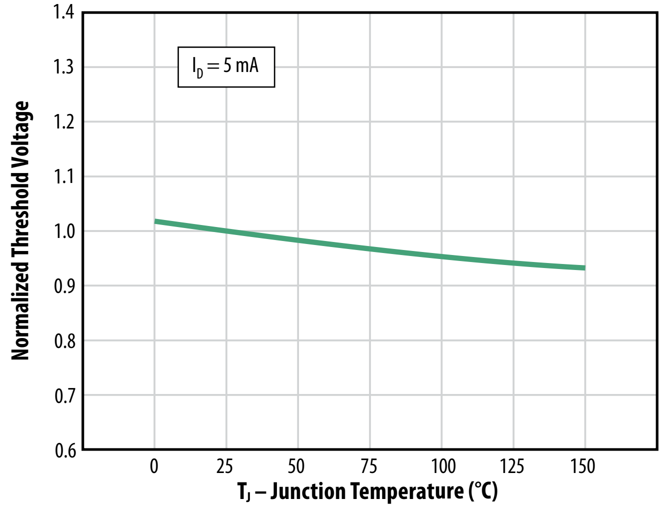


Figure 11: Transient Thermal Response Curves

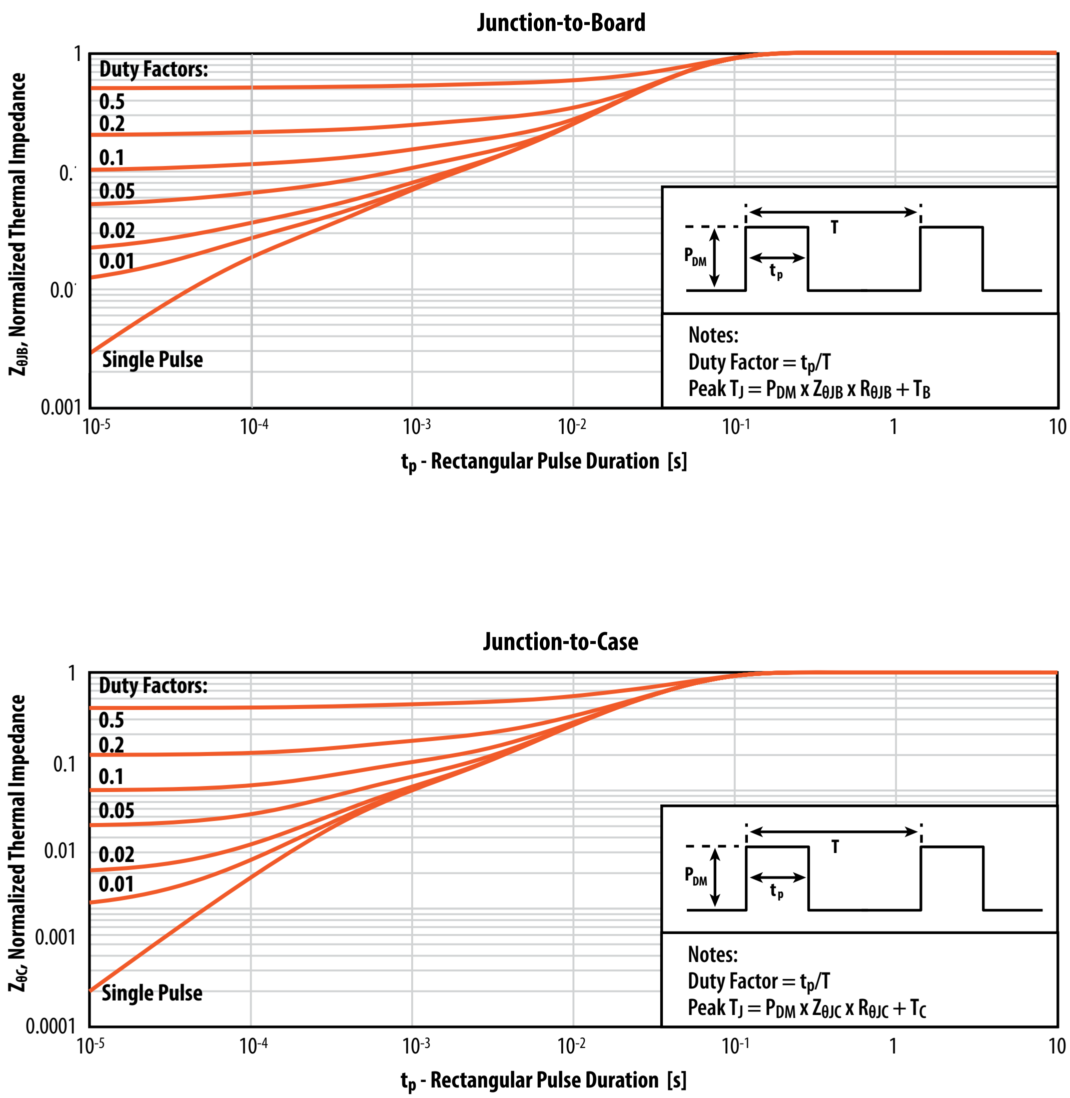
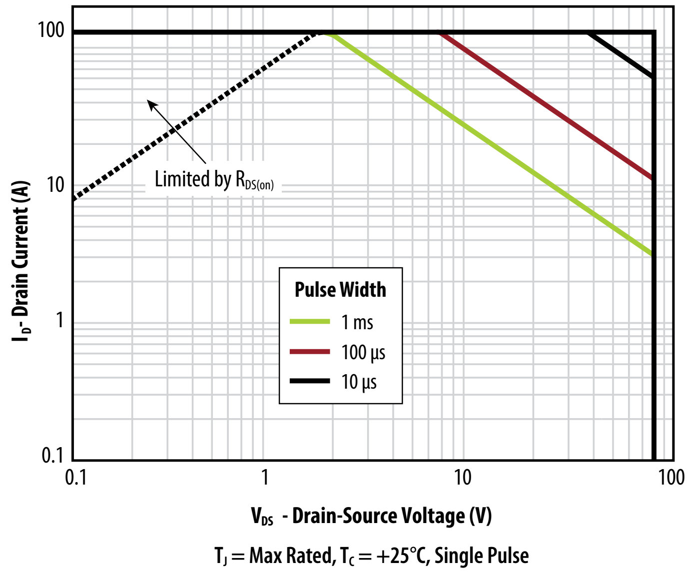
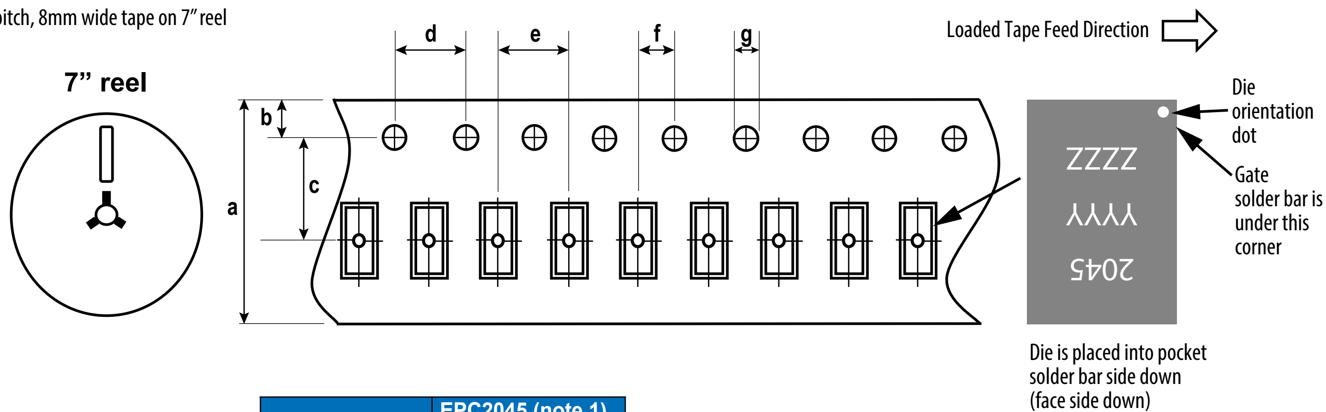


Figure 12: Safe Operating Area



TAPE AND REEL CONFIGURATION

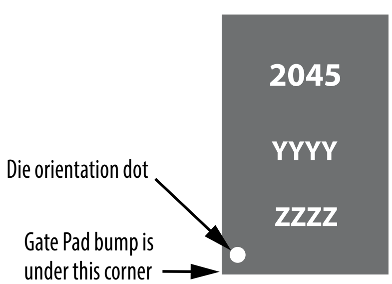
4mm pitch, 8mm wide tape on 7" reel



	EPC2045 (note 1)		
Dimension (mm)	**target**	**min**	**max**
a	8.00	7.90	8.30
b	1.75	1.65	1.85
c (see note)	3.50	3.45	3.55
d	4.00	3.90	4.10
e	4.00	3.90	4.10
f (see note)	2.00	1.95	2.05
g	1.5	1.5	1.6

Note 1: MSL 1 (moisture sensitivity level 1) classified according to IPC/JEDEC industry standard.
Note 2: Pocket position is relative to the sprocket hole measured as true position of the pocket, not the pocket hole.

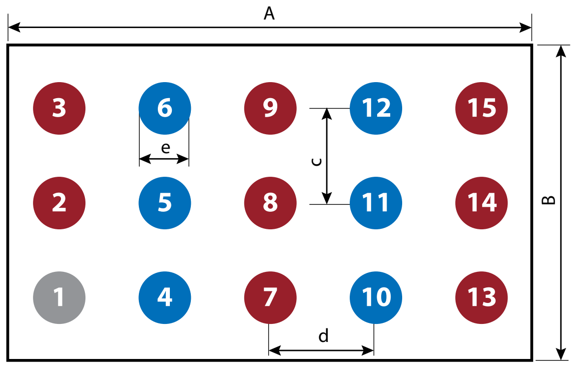
DIE MARKINGS



Part Number	Laser Markings		
	Part # Marking Line 1	Lot_Date Code Marking line 2	Lot_Date Code Marking Line 3
EPC2045	2045	YYYY	ZZZZ

DIE OUTLINE

Solder Bar View



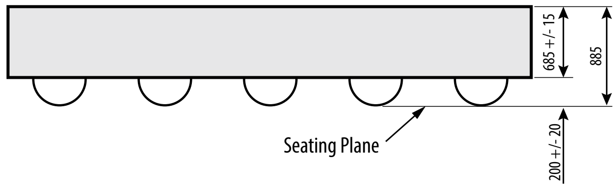
DIM	MICROMETERS		
	MIN	Nominal	MAX
A	2470	2500	2530
B	1470	1500	1530
c		450	
d		500	
e	238	264	290

Pads 1 is Gate;

Pads 2, 3, 7, 8, 9, 13, 14, 15 are Source;

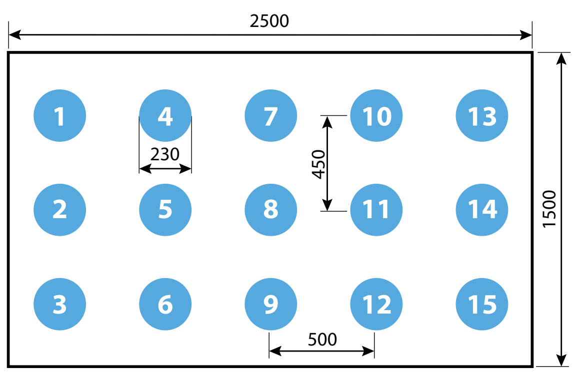
Pads 4, 5, 6, 10, 11, 12 are Drain;

Side View



RECOMMENDED LAND PATTERN

(units in µm)



The land pattern is solder mask defined.
Copper is larger than the solder mask opening.

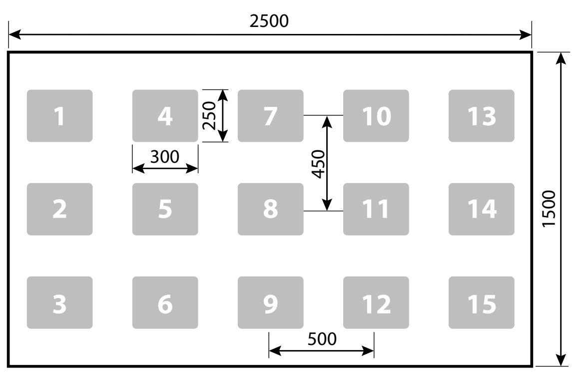
Pads 1 is Gate;

Pads 2, 3, 7, 8, 9, 13, 14, 15 are Source;

Pads 4, 5, 6, 10, 11, 12 are Drain;

RECOMMENDED STENCIL DRAWING

(measurements in µm)



Recommended stencil should be 4 mil (100 µm) thick, laser cut. The corner has a radius of R60.

Intended for use with SAC305 Type 4 solder, reference 88.5% metals content.

Additional assembly resources available at https://epc-co.com/epc/DesignSupport/AssemblyBasics.aspx

EPC Patent Listing: epc-co.com/epc/AboutEPC/Patents.aspx

Information subject to change without notice.
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