

FEATURES

- Reduces Systemic EMI.
- Modulates external clocks including crystals, crystal oscillators and ceramic resonators.
- 1X and 2X modulated frequency outputs.
- Modulation programmable with simple external loop filter (LF).
- 4 to 68 MHz operating frequency range.
- Digitally controlled modulation.
- TTL/CMOS compatible outputs.
- Center Spread Modulation.
- Low short term jitter.
- Bi-Directional buffers for reduced pin count.
- 3 - 5 Volt power supply.
- Low Power Dissipation;
 - 3.3 VDC = 30 mw - typical
 - 5.0 VDC = 100 mw - typical
- Available in 8 pin SOIC package.

APPLICATIONS

- Desktop/Laptop Computer
- Modems
- Scanners, Printers, Copiers, Fax Machines, MFP's
- Disk and CD-ROM Drives
- Automotive and Embedded Systems
- Networking, LAN/WAN
- Digital Cameras, Games
- LCD displays

BENEFITS

- Reduction of radiated EMI
- Fast Time to Market
- Lower cost of compliance
- Programmable EMI reduction
- No degradation in Rise/Fall times
- Lower component and PCB layer count

PRODUCT DESCRIPTION

The IMI FS731 is a Frequency Spreading EMI Attenuator designed for the purpose of reducing Electro Magnetic Interference (EMI) found in today's high speed digital systems. The FS731 uses a proprietary technique to modulate the output clock, Modout. By modulating the frequency of the digital clock, measured EMI at the fundamental and harmonic frequencies is greatly reduced. This reduction in radiated energy can significantly reduce the cost of complying with regulatory requirements without degrading digital waveforms.

The IMI FS731 is a very simple device to use and provides 1X and 2X frequency modulated outputs of the input reference frequency. By programming the two range select lines, RS0 and RS1, the FS731 can operate over a very wide range of input frequencies. By utilizing IMI's Bi-Directional Buffer design, the pin count of the FS731 is kept to a minimum. Bi-Directional Buffers is a method of providing an input control signal and an output driver circuit on the same pin. Bi-Directional Buffers is discussed further on page 6. The FS731 has a simple frequency selection table that allows it to operate from 4 MHz to 68 MHz in four separate ranges. The bandwidth of the frequency spread at Modout is determined by the values of the loop filter components. The modulation rate is determined by the input frequency and the input frequency range selected. The bandwidth of the FS731 can be programmed from as little as 0.5% up to as much as 4.0% by selecting the proper loop filter. It is for this reason that the FS731 uses an external loop filter (LF), in contrast to an internal loop filter type device which would severely limit the use of a wide range of bandwidths.

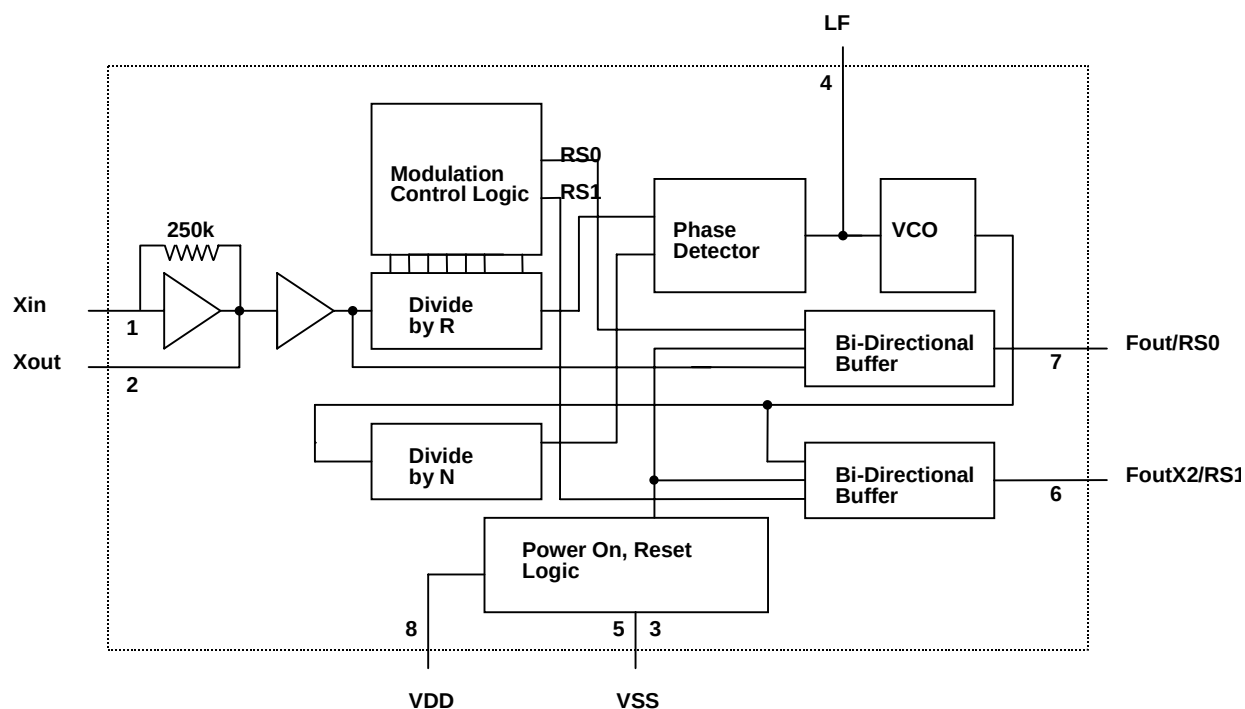


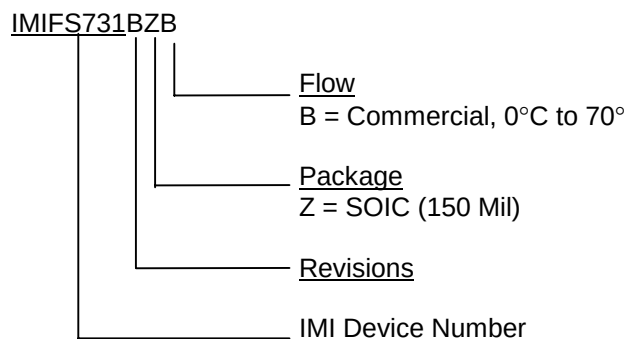
Figure 1. Block Diagram

ORDERING INFORMATION

Part Number	Package Type	Production Flow
IMIFS731BZB	8 Pin SOIC	Commercial, 0°C to 70°C

Marking Example:

IMI Date Code
FS731BZB
Lot Number



CONNECTION DIAGRAM



Figure 2. FS731, SOIC Package Pin Assignment

Pin Description				
Pin No.	Pin Name	I/O	TYPE	Description
1, 2	Xin, Xout	I/O	CMOS/TTL	Pins form an on-chip reference oscillator when connected to terminals of an external parallel resonant crystal. Xin may be connected to TTL/CMOS external clock source. If Xin is connected to an external clock other than a crystal, leave Xout (pin 2) unconnected.
4	LF	O	Analog	Single ended tri-state output of the phase detector. A two pole passive loop filter is connected to LF. See tables on page 7 and 8 for proper values.
3, 5	VSS	-	Ground	Circuit Ground.
6	FoutX2/RS1	I/O	CMOS/TTL	Bi-Directional pin used for range selection input and FoutX2 driver output. During power up, RS1 serves as an input control line for selecting the proper frequency operating range. After RS1 is latched into an internal register, this pin becomes an output for the modulated FoutX2 driver. Refer to page 6 for explanation on Bi-Directional buffers. The center frequency of FoutX2 is 2 times the reference frequency at Xin. FoutX2/RS1 has an internal 250 K Ω pull-up resistor to VDD.
7	Fout/RS0	I/O	CMOS/TTL	Bi-Directional pin used for range selection input and Fout driver output. During power up, RS0 serves as an input control line for selecting the proper frequency operating range. After power has reached VDD/3, RS0 is latched into a register and this pin becomes an output pin for the Fout driver. Fout is a modulated output clock of the reference frequency, Xin, being the center frequency and the modulation bandwidth and rate determined by the applied loop filter. Refer to tables 6 and 7 on pages 7 and 8 respectively. Fout/RS0 has internal 250K ohm pull-up resistor to VDD.
8	VDD	-	Power	Positive Circuit Power Supply.

Table 1

Frequency Range Selection Table		
Xin RANGE	RS1	RS0
4 - 8 MHz	0	0
8 - 16 MHz	0	1
16 - 40 MHz	1	0
40 - 68 MHz	1	1

Table 2

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, precautions should be taken to avoid application of any voltage higher than the absolute maximum rated voltages to this circuit. For proper operation, V_{in} and V_{out} should be constrained to the range, $V_{SS} < (V_{in} \text{ or } V_{out}) < V_{DD}$. All digital inputs are tied high or low internally. Refers to electrical specifications for operating supply range.

Absolute Maximum Ratings				
Item	Symbol	Min.	Max.	Units
Operating Voltage	VDD	3.0	6.0	VDC
Input, relative to VSS	VIRvss	-0.3	VDD +0.3	VDC
Output, relative to VSS	VORvss	-0.3	VDD +0.3	VDC
Temperature, Operating	TOP	0	+ 70	$^{\circ}\text{C}$
Temperature, Storage	TST	- 65	+ 150	$^{\circ}\text{C}$

Table 3

Electrical Characteristics					
Characteristic	Symbol	Min.	Typ.	Max.	Units
Input Low Voltage	VIL	-	-	0.8	VDC
Input High Voltage	VIH	2.0	-	-	VDC
Input Low Current	IIL	-	-	100	μA
Input High Current	IIH	-	-	100	μA
Output Low Voltage IOL= 8mA, VDD = 5V	VOL	-	-	0.4	VDC
Output High Voltage IOH = 8mA, VDD = 5V	VOH	VDD-1.0	-	-	VDC
Output Low Voltage IOL= 5mA, VDD = 3.3V	VOL	-	-	0.4	VDC
Output High Voltage IOH = 3mA, VDD = 3.3V	VOH	2.4	-	-	VDC
Input Capacitance (Pin-1)	Cin1	-	3	4	pF
Output Capacitance (Pin-2)	Cin2	-	5	6	pF
Tri-State Leakage Current (pin 7)	IOZ	-	-	5.0	μA
5 Volt Supply Current @30 MHz, No Load.	Idd	-	20	25	ma
3.3 Volt Supply Current @ 30 MHz, No Load.	Idd	-	9	12	ma
Short Circuit Current (Refout or Modout)	ISC	-	-	25	ma

Test measurements performed at VDD = 3.3V and 5.0V $\pm 10\%$, Xin = 30 MHz, Ta = 0°C to 70°C

Table 4

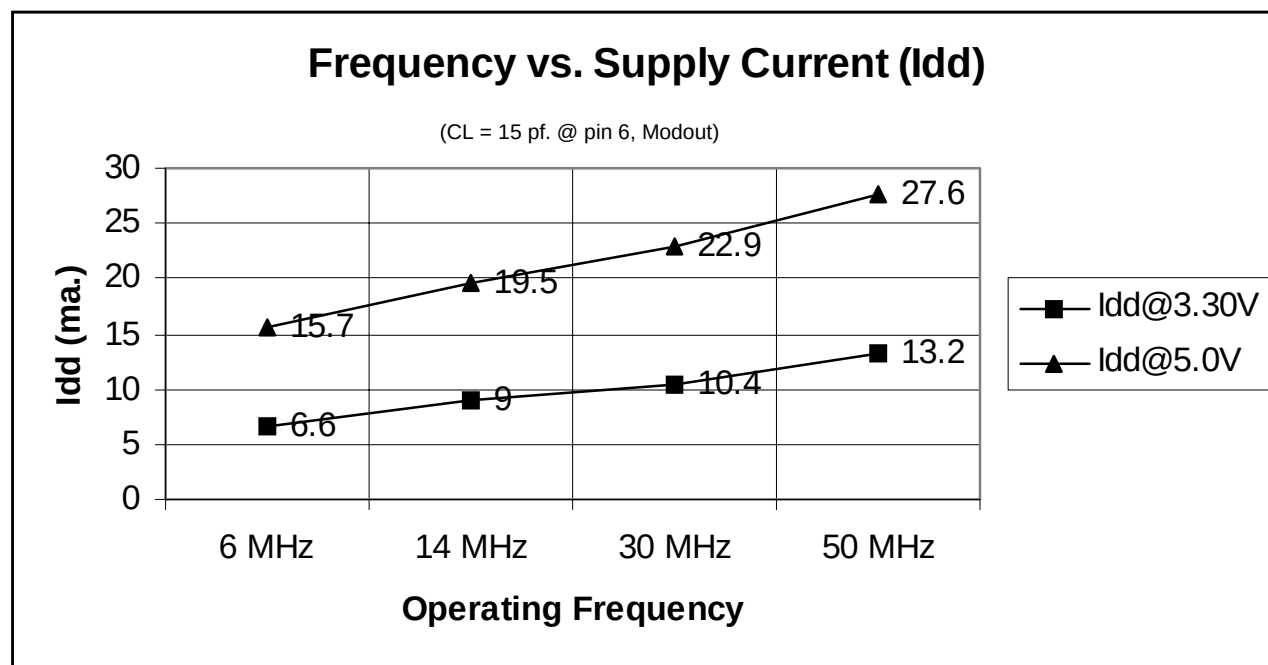


Figure 3. Frequency vs. I_{dd}

Timing Characteristics					
Characteristic	Symbol	Min	Typ	Max	Units
Output Rise Time Measured at 10% - 90% @ 5 VDC	t _{TLH}	4.5	5.1	5.7	ns
Output Fall Time Measured at 10% - 90% @ 5 VDC	t _{THL}	4.0	4.3	4.7	ns
Output Rise Time Measured at 0.8V - 2.0V @ 5 VDC	t _{TLH}	850	900	975	ps
Output Fall Time Measured at 0.8V - 2.0 V @ 5 VDC	t _{THL}	1.3	1.4	1.5	ns
Output Rise Time Measured at 10% - 90% @ 3.3 VDC	t _{TLH}	5.0	5.3	5.9	ns
Output Fall Time Measured at 10% - 90% @ 3.3 VDC	t _{THL}	4.8	5.1	5.4	ns
Output Rise Time Measured at 0.8V - 2.0V @ 3.3 VDC	t _{TLH}	1.8	1.9	2.0	ns
Output Fall Time Measured at 0.8V - 2.0 V @ 3.3 VDC	t _{THL}	2.0	2.2	2.4	ns
Output Duty Cycle	T _{symF1}	45	50	55	%
ccj, Jitter @ 5.0 VDC, 50 MHz	ccj	-	300	350	ps
ccj, Jitter @ 3.3 VDC, 50 MHz	ccj	-	200	250	ps

Measurements performed at VDD = 3.3 and 5.0V ± 10%, Ta = 0°C to 70°C, CL = 15pF, Xin = 30 MHz.

Table 5

BI-DIRECTIONAL BUFFERS

Two pins on the FS731 are connected to Bi-Directional buffers. Using Bi-Directional buffers is a method of sharing an input circuit and an output circuit with the same pin on the IC assembly, thereby reducing the pin count. Each Bi-Directional I/O acts as an input during power up and as an output after power has reached a certain voltage. For the FS731, that voltage is approximately $V_{DD}/3$. At $V_{DD}/3$, the FS731 latches the logic state of the respective line in an internal register for as long as power is applied to the FS731. After $V_{DD}/3$ has been reached and the power on reset has occurred, the respective pin is switched from an input gate to an output driver. This pin remains an output driver for as long as power is applied.

Loop Filters

The FS731 requires an external loop filter to provide the proper operation and bandwidth for a given input frequency. Since the FS731 operates over a wide range of frequencies, the loop filter will change depending on the frequency of operation. The following loop filter values are recommended for best performance and modulation profile at 5.0 volts and 3.3 volts VDD, measured across pin 8 (VDD) and 5 (VSS).

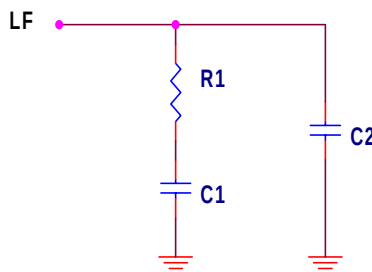


Figure 4.

The tables on pages 7 and 8 contain the loop filter values for the a power supply voltage of 5.0 and 3.3 VDC, +/- 10%. The values in both tables 6 and 7 were bench tested for accuracy and optimal performance. The loop filter values were determined by taking 4 MHz segments of the overall operating range and testing for the optimal performance at

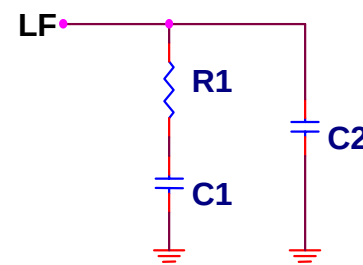
the center frequency of each 4 MHz band. This means that in the first band in the table below, 4 - 8 MHz, the loop filter values shown in the table produce the most optimized performance for 6 MHz. It is possible to deviate slightly from these values for optimal performance at some other center frequency. Also note that the values listed in these tables are all commonly manufactured components.

Recommended Loop Filter Values (VDD = 5.0 VDC, +/- 10%)						
Input (MHz)	RS1	RS0	BW = 1% (+/- .5%)	BW = 2% (+/- 1%)	BW = 3% (+/- 1.5%)	BW = 4% (+/- 2%)
4-8	0	0	R1=2.2K C1=270pF C2=22pF	R1=2.2K C1=120pF C2=22pF	R1=2.2K C1=82pF C2=22pF	R1=2.2K C1=56pF C2=22pF
8-12	0	1	R1=2.2K C1=470pF C2=22pF	R1=2.2K C1=220pF C2=22pF	R1=2.2K C1=150pF C2=22pF	R1=2.2K C1=100pF C2=22pF
12-16	0	1	R1=2.2K C1=180pF C2=22pF	R1=2.2K C1=82pF C2=22pF	R1=2.2K C1=56pF C2=22pF	R1=2.2K C1=33pF C2=22pF
16-20	1	0	R1=2.2K C1=680pF C2=22pF	R1=2.2K C1=330pF C2=22pF	R1=2.2K C1=220pF C2=22pF	R1=2.2K C1=150pF C2=22pF
20-24	1	0	R1=2.2K C1=470pF C2=22pF	R1=2.2K C1=220pF C2=22pF	R1=2.2K C1=150pF C2=22pF	R1=2.2K C1=100pF C2=22pF
24-28	1	0	R1=2.2K C1=220pF C2=22pF	R1=2.2K C1=100pF C2=22pF	R1=2.2K C1=82pF C2=22pF	R1=2.2K C1=56pF C2=22pF
28-32	1	0	R1=4.7K C1=220pF C2=0pF	R1=4.7K C1=100pF C2=0pF	R1=4.7K C1=68pF C2=0pF	R1=4.7K C1=47pF C2=0pF
32-36	1	0	R1=4.7K C1=120pF C2=0pF	R1=4.7K C1=68pF C2=0pF	R1=4.7K C1=47pF C2=7pF	R1=4.7K C1=27pF C2=15pF
36-40	1	0	R1=4.7K C1=100pF C2=0pF	R1=4.7K C1=33pF C2=0pF	R1=4.7K C1=27pF C2=0pF	R1=4.7K C1=18pF C2=0pF
40-44	1	1	R1=2.2K C1=470pF C2=0pF	R1=2.2K C1=180pF C2=22pF	R1=2.2K C1=120pF C2=22pF	R1=2.2K C1=82pF C2=22pF
44-48	1	1	R1=2.2K C1=330pF C2=0pF	R1=2.2K C1=150pF C2=22pF	R1=2.2K C1=120pF C2=16pF	R1=2.2K C1=82pF C2=10pF
48-52	1	1	R1=2.2K C1=270pF C2=0pF	R1=2.2K C1=120pF C2=0pF	R1=2.2K C1=100pF C2=0pF	R1=2.2K C1=68pF C2=0pF
52-56	1	1	R1=2.2K C1=220pF C2=0pF	R1=2.2K C1=100pF C2=0pF	R1=2.2K C1=82pF C2=0pF	R1=2.2K C1=56pF C2=0pF
56-60	1	1	R1=2.2K C1=220pF C2=0pF	R1=2.2K C1=100pF C2=0pF	R1=2.2K C1=68pF C2=0pF	R1=2.2K C1=39pF C2=0pF
60-64	1	1	R1=7.5K C1=120pF C2=33pF	R1=7.5K C1=68pF C2=0pF	R1=7.5K C1=47pF C2=0pF	R1=7.5K C1=33pF C2=0pF
64-68	1	1	R1=7.5K C1=120pF C2=33pF	R1=7.5K C1=68pF C2=0pF	R1=7.5K C1=47pF C2=0pF	R1=7.5K C1=27pF C2=0pF

Note: 0 pF means that the capacitor is removed.

Table 6.

NOTE: When clock frequency is on boundary between two ranges, it is recommended that the higher range be used.

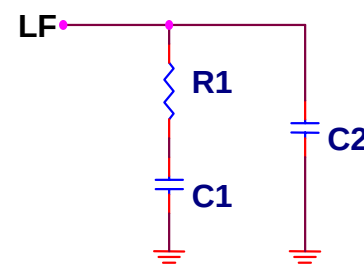


Recommended Loop Filter Values (VDD = 3.3 VDC, +/- 10%)						
Input (MHz)	RS1	RS0	BW = 1% (+/- .5%)	BW = 2% (+/- 1%)	BW = 3% (+/- 1.5%)	BW = 4% (+/- 2%)
4-8	0	0	R1=2.2K C1=220pF C2=22pF	R1=2.2K C1=100pF C2=22pF	R1=2.2K C1=68pF C2=22pF	R1=2.2K C1=39pF C2=22pF
8-12	0	1	R1=2.2K C1=470pF C2=22pF	R1=2.2K C1=220pF C2=22pF	R1=2.2K C1=150pF C2=22pF	R1=2.2K C1=100pF C2=22pF
12-16	0	1	R1=2.2K C1=120pF C2=22pF	R1=2.2K C1=56pF C2=22pF	R1=2.2K C1=39pF C2=22pF	R1=2.2K C1=27pF C2=8pF
16-20	1	0	R1=2.2K C1=680pF C2=22pF	R1=2.2K C1=390pF C2=22pF	R1=2.2K C1=270pF C2=22pF	R1=2.2K C1=180pF C2=22pF
20-24	1	0	R1=2.2K C1=560pF C2=22pF	R1=2.2K C1=220pF C2=22pF	R1=2.2K C1=120pF C2=22pF	R1=2.2K C1=82pF C2=22pF
24-28	1	0	R1=2.2K C1=220pF C2=22pF	R1=2.2K C1=82pF C2=22pF	R1=2.2K C1=56pF C2=22pF	R1=2.2K C1=39pF C2=10pF
28-32	1	0	R1=4.7K C1=180pF C2=0pF	R1=4.7K C1=68pF C2=0pF	R1=4.7K C1=39pF C2=0pF	R1=4.7K C1=27pF C2=0pF
32-36	1	0	R1=4.7K C1=82pF C2=0pF	R1=4.7K C1=33pF C2=0pF	R1=4.7K C1=22pF C2=0pF	R1=4.7K C1=12pF C2=0pF
36-40	1	1	R1=47K C1=1.0uF C2=390pF	R1=47K C1=1.0uF C2=220pF	R1=47K C1=1.0uF C2=150pF	R1=47K C1=1.0uF C2=100pF
40-44	1	1	R1=2.2K C1=680pF C2=0pF	R1=2.2K C1=270pF C2=0pF	R1=2.2K C1=180pF C2=10pF	R1=2.2K C1=120pF C2=10pF
44-48	1	1	R1=2.2K C1=330pF C2=0pF	R1=2.2K C1=180pF C2=0pF	R1=2.2K C1=120pF C2=0pF	R1=2.2K C1=82pF C2=0pF
48-52	1	1	R1=2.2K C1=270pF C2=0pF	R1=2.2K C1=120pF C2=0pF	R1=2.2K C1=82pF C2=0pF	R1=2.2K C1=56pF C2=0pF
52-56	1	1	R1=2.2K C1=220pF C2=0pF	R1=2.2K C1=100pF C2=0pF	R1=2.2K C1=68pF C2=0pF	R1=2.2K C1=33pF C2=0pF
56-60	1	1	R1=2.2K C1=150pF C2=0pF	R1=2.2K C1=68pF C2=5pF	R1=3.3K C1=47pF C2=12pF	R1=4.7K C1=33pF C2=22pF
60-64	1	1	R1=4.7K C1=100pF C1=0pF	R1=4.7K C1=47pF C2=0pF	R1=4.7K C1=27pF C2=0pF	R1=4.7K C1=18pF C1=0pF
64-68	1	1	R1=7.5K C1=68pF C2=0pF	R1=7.5K C1=33pF C2=0pF	R1=7.5K C1=22pF C2=0pF	R1=7.5K C1=15pF C2=0pF

Note: 0 pF means that the capacitor is removed.

Table 7.

NOTE: When clock frequency is on boundary between two ranges, it is recommended that the higher range be used.



SSCG Modulation Profile

The modulation rate of the FS731 is determined by the input frequency and the operating range. The input frequency is divided by a fixed number, depending on the operating range that is selected. The modulation rate of the FS731 can be determined from the chart at the right.

Example: Freq. of X_{in} = 25 MHz
 Operating Range = 16 - 40 MHz
 Modrate = $F_{xin}/240 = 104.166$ KHz.

X_{in} Range	Mod. rate divider
4 - 8 MHz	60
8 - 16 MHz	120
16 - 40 MHz	240
40 - 68 MHz	480

Table 8

With the correct loop filter connected to pin 4, the following profile will provide the best EMI reduction. This profile can be seen on a Time Domain Analyzer.

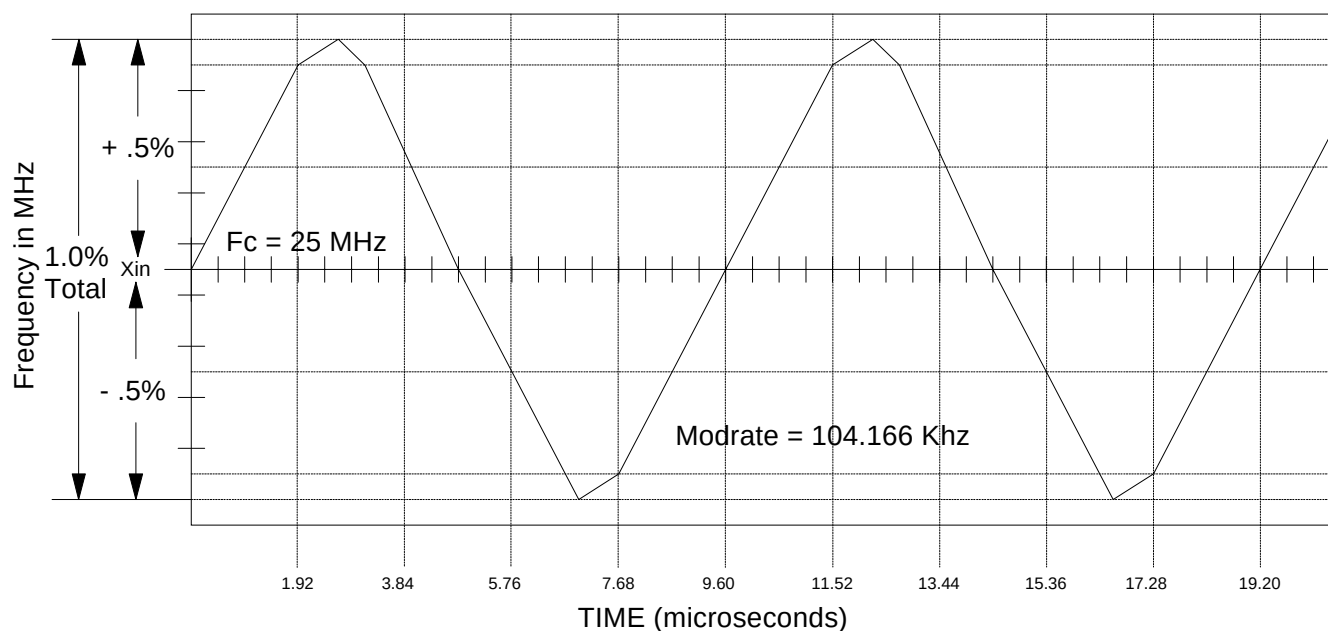


Figure 5. Frequency Profile in Time Domain

THEORY OF OPERATION

The FS731 is a Phase Lock Loop (PLL) type clock generator using Direct Digital Synthesis (DDS). By precisely controlling the bandwidth of the output clock, the FS731 becomes a Low EMI clock generator. The theory and detailed operation of the FS731 will be discussed in the following sections.

EMI

All clocks generate unwanted energy in their harmonics. Conventional digital clocks are square waves with a duty cycle that is very close to 50 %. Because of the 50/50 duty cycle, digital clocks generate most of their harmonic energy in the odd harmonics, i.e.; 3rd, 5th, 7th etc. It is possible to reduce the amount of energy contained in the fundamental and harmonics by increasing the bandwidth of the fundamental clock frequency. Conventional digital clocks have a very high Q factor, which means that all of the energy at that frequency is concentrated in a very narrow bandwidth, consequently, higher energy peaks. Regulatory agencies test electronic equipment by the amount of peak energy radiated from the equipment. By reducing the peak energy at the fundamental and harmonics, the equipment under test is able to satisfy agency requirements for Electro-Magnetic Interference (EMI). Conventional methods of reducing EMI have been to use shielding, filtering, multi-layer PCB's etc. The FS731 uses the approach of reducing the peak energy in the clock by increasing the clock bandwidth, and lowering the Q.

SSCG

The FS731 uses a proprietary technique to modulate the clock over a very narrow bandwidth and controlled rate of change, both peak and cycle to cycle. The FS731 takes a narrow band digital reference clock in the range 4 - 68 MHz and produces a clock that sweeps between a controlled start and stop frequency and precise rate of change. To understand what happens to an SSCG clock, consider that we have a 20 MHz clock with a 50 % duty cycle. From a 20 MHz clock we know the following;

Clock Frequency = $F_c = 20 \text{ MHz}$.
Clock Period = $T_c = 1/20 \text{ MHz} = 50 \text{ ns}$

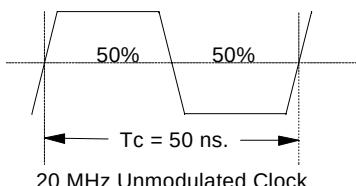


Figure 6.

Consider that this 20 MHz clock is applied to the Xin input of the FS731, either as an externally driven clock or as the result of a parallel resonant crystal connected to pins 1 and 2 of the FS731. Also consider that the FS731 is operating from a 5 Volt DC power supply and the loop filter is set for a total bandwidth spread of 2%. Refer to Table 6 on page 7.

From the above parameters, the output clock at Modout will be sweeping symmetrically around a center frequency of 20 MHz.

The minimum and maximum extremes of this clock will be +200 KHz and -200 KHz.. So, we have a clock that is sweeping from 19.8 MHz to 20.2 MHz and back again. If we were to look at this clock on a spectrum analyzer we would see the picture in figure 7. Keep in mind that this is a drawing of a perfect clock with no noise.

We see that the original 20 MHz reference clock is at the center Frequency, F_c , and the minimum and maximum extremes are positioned symmetrically about the center frequency. This type of modulation is called **Center-Spread**. Figure 7 illustrates this as it is seen on a spectrum analyzer.

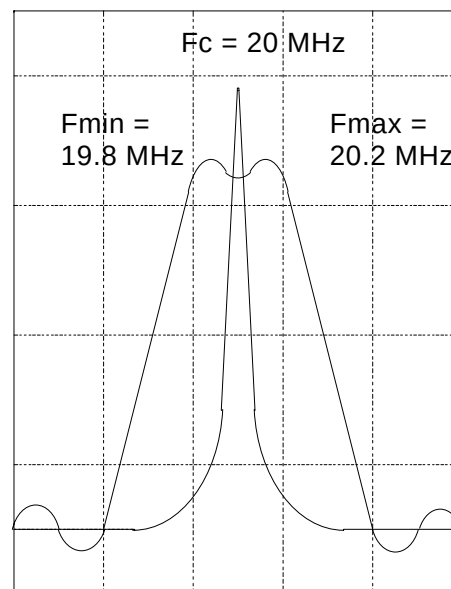


Figure 7.

Figure 8 shows a 20 MHz clock as it would be seen on an oscilloscope. The top trace is the non-modulated reference clock, or the Refout clock at pin 7. The bottom trace is the modulated clock at pin 6. From this comparison chart you can see that the frequency is decreasing and the period of each successive clock increasing. The T_c measurements on the left and right of the bottom trace indicate the max. and min. extremes of the clock. Intermediate clock changes are small and accumulate to achieve the total period deviation. The reverse of this Figure would show the clock going from min. extreme back to the high extreme.

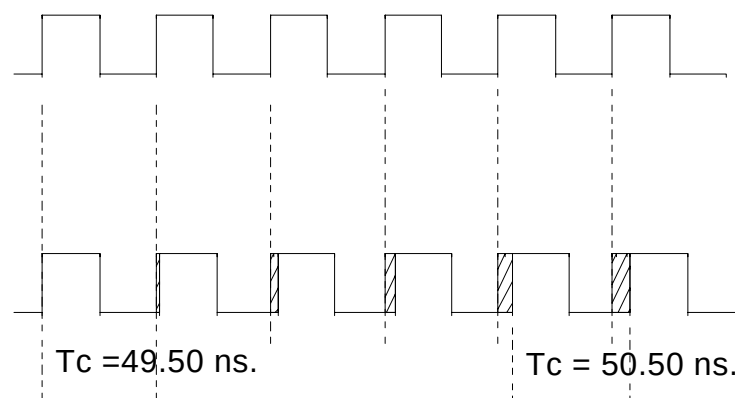


Figure 8. Period Comparison Chart

The FS731 is a center spread clock, meaning that it symmetrically spreads above and below the reference frequency. If a down spread clock is required for a specific application, refer to the datasheets for the SM530 and the SG52x series of Low EMI clock generators.

Looking at figure 7, you will note that the peak amplitude of the 20 MHz non-modulated clock is higher than the wideband modulated clock. This difference in peak amplitudes between modulated and unmodulated clocks is the reason why SSCG clocks are so effective in digital systems. This figure refers to the fundamental frequency of a clock. A very important characteristic of the SSCG clock is that the bandwidth of the harmonics is multiplied by the harmonic number. In other words, if the bandwidth of a 20 MHz clock is 200 KHz, the bandwidth of the 3rd harmonic will be 3 times 200 KHz, or 600 KHz. The amount of bandwidth is relative to the amount of energy in the clock. Consequently, the wider the bandwidth, the greater the energy reduction of the clock.

Approved Product

Low EMI Spectrum Spread Clock

Most applications will not have a problem meeting agency specifications at the fundamental frequency. It is the higher harmonics that usually cause the most problems. With an SSCG clock, the bandwidth and peak energy reduction increases with the harmonic number. Consider that the 11th harmonic of a 20 MHz clock is 220 MHz. With a total spread of 200 KHz at 20 MHz, the spread at the 11th harmonic would be 2.20 MHz which greatly reduces the peak energy content.

The difference in the peak energy of the modulated clock and the non-modulated clock in typical applications will see a 2 - 3 dB reduction at the fundamental and as much as 8 - 10 dB reduction at the intermediate harmonics, 3rd, 5th, 7th etc. At the higher harmonics, it is quite possible to reduce the peak harmonic energy, compared to the unmodulated clock, by as much as 12 to 18 dB.

The following images are actual scans of the FS741. The FS741 is the same part as the FS731 but has a times 2 output instead of the Refout. These scans are from a spectrum analyzer and time domain analyzer of the FS741 at various frequencies running at 3.3 volts DC.

Figure 9 at the right shows a modulated 10 Mhz clock at Modout of the FS741. The following parameters apply to this scan;

Fin = 10 Mhz.
BW = 2% (total)
Vertical scale = 6 dB/div.

From this scan it can be seen the bandwidth of the clock is wider than a conventional clock. Notice the EMI filters displayed at the bottom of the image. This is the same filter settings that are used by regulatory agencies.

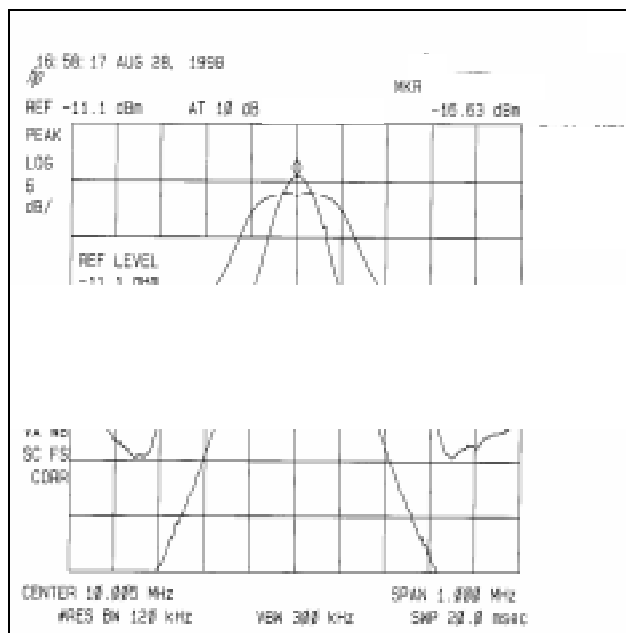


Figure 9.

It is clear from Figure 9, that the peak amplitude of the modulated clock is lower in amplitude than the non-modulated clock. In fact, this image indicates that the difference between the two peaks is approximately 2 dB.



Low EMI Spectrum Spread Clock

17:03:32 AUG 28, 1998

REF -9.9 dBm AT 10 dB MKR -21.98 dBm

PEAK
LOS
S
dB/

SPAN
1.000 MHz

MEAS UNCAL

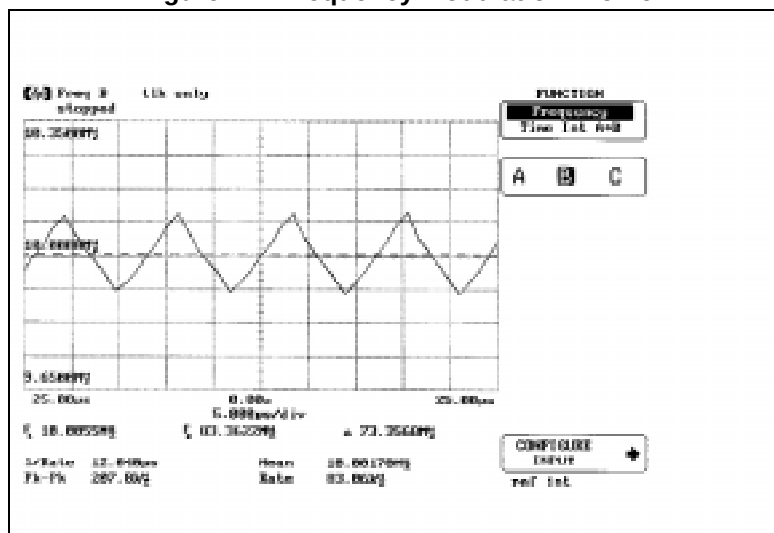
VA WD
SC FC
CORR

CENTER 30.015 MHz
#RES BW 120 kHz VSW 1 kHz

SPAN 1.000 MHz
#SWP 25.8 msec

Modulation Rate

Figure 11. Frequency Modulation Profile

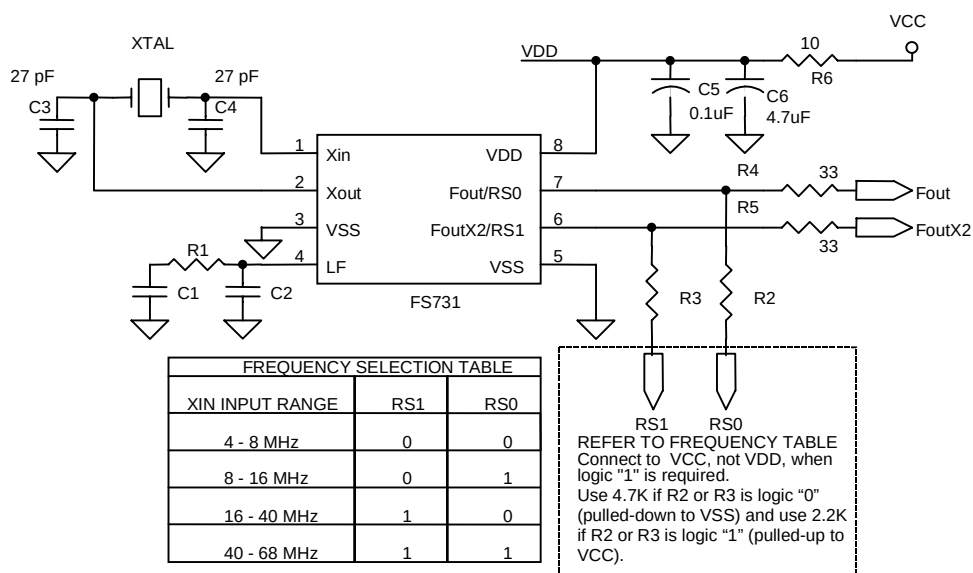


The Xin reference clock determines the modulation frequency but the internal SSCG control logic determines the actual modulation profile. It is very important to note that the Bandwidth of the clock modulation is determined by the values of the loop filter applied to pin 4.

Figure 11 shows the modulation profile of the FS731. This type of test is done with a time domain analyzer. What this shows is the amount of time that the clock spends at any one frequency within its modulation envelope. From this type of picture, the amount of modulation percentage and modulation rate can be determined. This picture shows that the FS731 is modulating 2% around the 10 MHz input and the modulation rate is 83.06 KHz.

APPLICATION NOTES AND SCHEMATICS

The schematic diagram shown below is a simple minimum component application example of an FS731 design. In the case shown below, the control lines are configured for the following parameters;



Note: C3 and C4 values assume a first order crystal with $C_L = 18$ pF.

Figure 12.

The circuit shown below is the equivalent oscillator circuit used in the FS731;

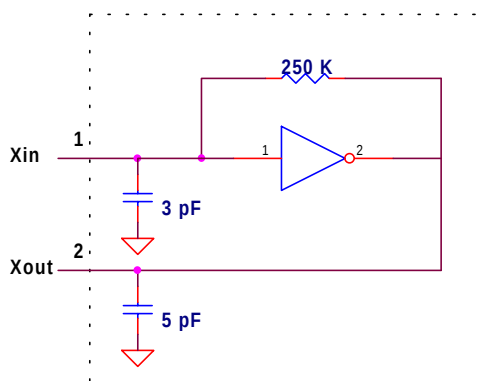


Figure 13.

Calculating dB Reduction

The dB reduction for a give frequency and spread can be calculated using a simple formula. This formula is only helpful in determining a relative dB reduction for a given application. This formula assumes an ideal clock with 50% duty cycle and therefore only predicts the EMI reduction of odd harmonics. Other circumstances such as non-ideal clock and noise will affect the actual dB reduction. The formula is as follows;

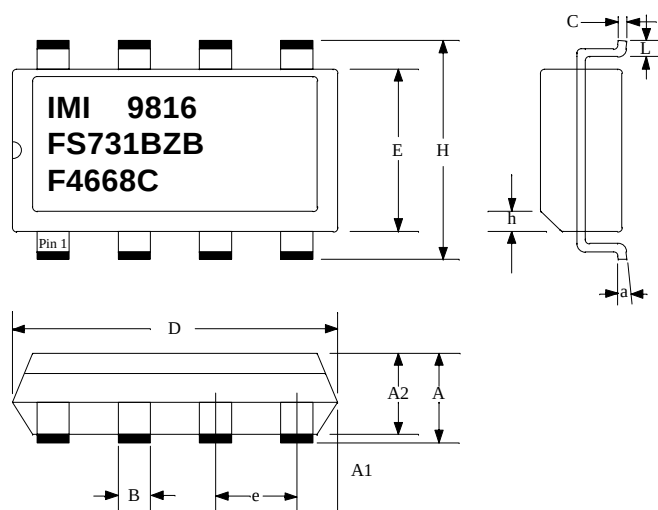
$$\text{dB} = 6.5 + 9(\text{Log}_{10}(\text{F})) + 9(\text{Log}_{10}(\text{P}))$$

Where; F = Frequency in MHz, P = total % spread (2.5% = .025)

Using a 50 Mhz clock with a 2.5% spread, the theoretical dB reduction would be;

$$\begin{aligned} \text{dB @ 50 Mhz (Fund)} &= 6.5 + 15.29 - 14.42 = 7.37 \\ \text{dB @ 150 Mhz (3rd)} &= 6.5 + 19.58 - 14.42 = 11.66 \\ \text{dB @ 550 Mhz (11th)} &= 6.5 + 24.66 - 14.42 = 16.74 \end{aligned}$$

PACKAGE DIMENSIONS AND DRAWINGS



8 PIN SOIC OUTLINE DIMENSIONS						
	INCHES			MILLIMETERS		
SYMBOL	MIN	NOM	MAX	MIN	NOM	MAX
A	0.061	0.064	0.068	1.55	1.63	1.73
A ₁	0.004	0.006	0.0098	0.127	0.150	0.250
A ₂	0.055	0.058	0.061	1.40	1.47	1.55
B	0.0138	0.016	0.0192	0.35	0.41	0.49
C	0.0075	0.008	0.0098	0.19	0.20	0.25
D	0.189	0.194	0.196	4.80	4.93	4.98
E	0.150	0.155	0.157	3.81	3.94	3.99
e	0.050 BSC			1.270 BSC		
H	.230	.236	.244	5.84	5.99	6.20
h	0.010	0.013	0.016	0.25	0.33	0.41
a	0°	5°	8°	0°	5°	8°
L	0.016	0.025	0.035	0.41	0.64	0.89

8 PIN SOIC PACKAGE

NOTES:

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