

MC12093

÷2, ÷4, ÷8 1.1 GHz Low Power Prescaler with Stand-By Mode

Description

The MC12093 is a single modulus prescaler for low power frequency division of a 1.1 GHz high frequency input signal. MOSAIC V™ technology is utilized to achieve low power dissipation of 6.75 mW at a minimum supply voltage of 2.7 V.

On-chip output termination provides output current to drive a 2.0 pF (typical) high impedance load. If additional drive is required for the prescaler output, an external resistor can be added parallel from the OUT pin to GND to increase the output power. Care must be taken not to exceed the maximum allowable current through the output.

Divide ratio control inputs SW1 and SW2 select the required divide ratio of ÷2, ÷4, or ÷8.

Stand-By mode is featured to reduce current drain to 50 µA typical when the standby pin SB is switched LOW disabling the prescaler.

Features

- 1.1 GHz Toggle Frequency
- Supply Voltage 2.7 V to 5.5 Vdc
- Low Power 3.0 mA Typical
- Operating Temperature = -40°C to 85°C
- Divide by 2, 4 or 8 Selected by SW1 and SW2 Pins
- On-Chip Termination
- These Devices are Pb-Free, Halogen Free and are RoHS Compliant

Table 1. FUNCTIONAL TABLE

SW	SW2	Divide Ratio
L	L	8
H	L	4
L	H	4
H	H	2

1. SW1 & SW2: H = (V_{CC} - 0.5 V) to V_{CC}; L = Open.
2. SB: H = 2.0 V to V_{CC}, L = GND to 0.8 V.

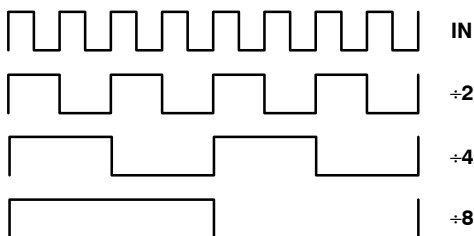


Figure 1. Function Chart

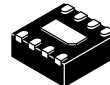


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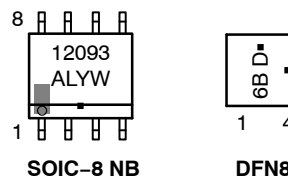


SOIC-8 NB
D SUFFIX
CASE 751-07



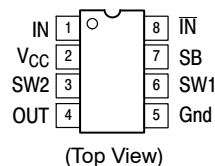
DFN8
MN SUFFIX
CASE 506AA

MARKING DIAGRAM



- A = Assembly Location
- L = Wafer Lot
- Y = Year
- W = Work Week
- = Pb-Free Package

PIN CONNECTIONS



A LOW on the Stand-By Pin 7 disables the device.

ORDERING INFORMATION

Device	Package	Shipping
MC12093DG	SOIC-8 NB (Pb-Free)	98 Units/Tube
MC12093DR2G	SOIC-8 NB (Pb-Free)	2500 Tape & Reel
MC12093MNR4G	DFN8 (Pb-Free)	1000 Tape & Reel

MC12093

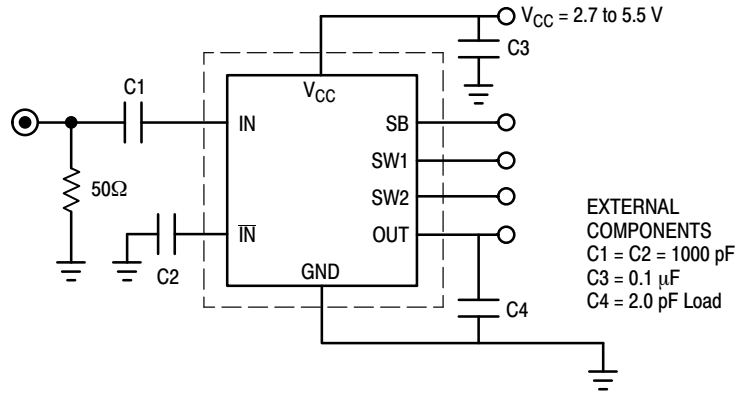


Figure 2. AC Test Circuit

Table 2. ATTRIBUTES

Characteristics	Value
Internal Input Pulldown Resistor	N/A
Internal Input Pullup Resistor	N/A
ESD Protection Human Body Model Machine Model Charged Device Model	> 4 kV > 200 V > 2 kV
Moisture Sensitivity, Indefinite Time Out of Drypack (Note 1)	Pb-Free Pkg
SOIC-8 NB DFN8	Level 1 Level 1
Flammability Rating Oxygen Index: 28 to 34	UL 94 V-0 @ 0.125 in
Transistor Count	125 Devices
Meets or exceeds JEDEC Spec EIA/JESD78 IC Latchup Test	

1. For additional information, see Application Note [AND8003/D](#).

Table 3. MAXIMUM RATINGS

Symbol	Rating	Value	Unit
V_{CC}	Power Supply Voltage, Pin 2	-0.5 to 6.0	Vdc
T_A	Operating Temperature Range	-40 to 85	°C
T_{stg}	Storage Temperature Range	-65 to 150	°C
I_O	Maximum Output Current, Pin 4	4.0	mA
θ_{JC}	Thermal Resistance (Junction-to-Case) (Note 1) DFN8	35 to 40	°C/W

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

NOTE: ESD data available upon request.

1. JEDEC standard multilayer board – 2S2P (2 signal, 2 power). For DFN8 only, thermal exposed pad must be connected to a sufficient thermal conduit. Electrically connect to the most negative supply (GND) or leave unconnected, floating open.

MC12093

Table 4. ELECTRICAL CHARACTERISTICS ($V_{CC} = 2.7$ to 5.5 V; $T_A = -40$ to 85°C)

Symbol	Characteristic	Min	Typ	Max	Unit
f_t	Toggle Frequency (Sine Wave)	0.1	1.4	1.1	GHz
I_{CC}	Supply Current	–	3.0	4.5	mA
ISB	Stand-By Current	–	120	200	μA
V_{IH1}	Stand-By Input HIGH (SB)	2.0	–	V_{CC}	V
V_{IL1}	Stand-By Input LOW (SB)	Gnd	–	0.8	V
V_{IH2}	Divide Ratio Control Input HIGH (SW1 & SW2)	$V_{CC} - 0.5$	V_{CC}	$V_{CC} + 0.5$	V
V_{IL2}	Divide Ratio Control Input LOW (SW1 & SW2)	OPEN	OPEN	OPEN	
V_{OUT}	Output Voltage Swing (2.0 pF Load)				V_{pp}
	Output Frequency 12.5–350 MHz (Note 1)	0.6	0.80	–	
	Output Frequency 350–400 MHz (Note 2)	0.5	0.70	–	
	Output Frequency 400–450 MHz (Note 3)	0.4	0.55	–	
V_{IN}	Output Frequency 450–550 MHz (Note 4)	0.3	0.45	–	mVpp
	Input Voltage Sensitivity				
	250–1100 MHz	100	–	1000	
	100–250 MHz	400	–	1000	

1. Input frequency 1.1 GHz, ± 8 , minimum output frequency of 12.5 MHz.

2. Input frequency 700–800 MHz, ± 2 .

3. Input frequency 800–900 MHz, ± 2 .

4. Input frequency 900–1100 MHz, ± 2 .

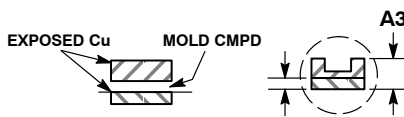
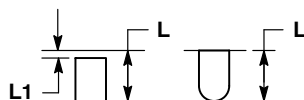
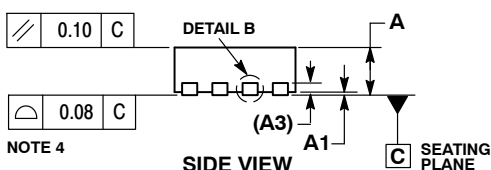
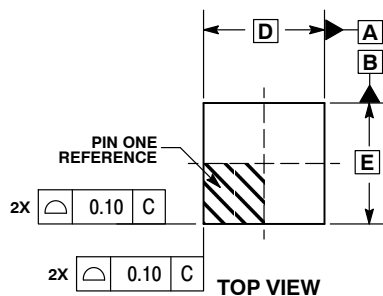
MECHANICAL CASE OUTLINE PACKAGE DIMENSIONS



SCALE 4:1

DFN8 2x2, 0.5P
CASE 506AA
ISSUE F

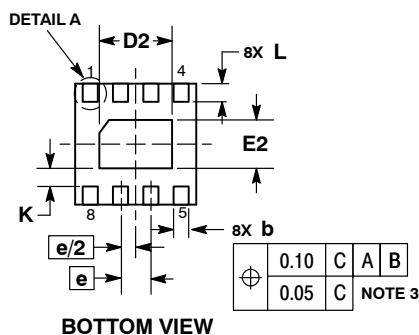
DATE 04 MAY 2016



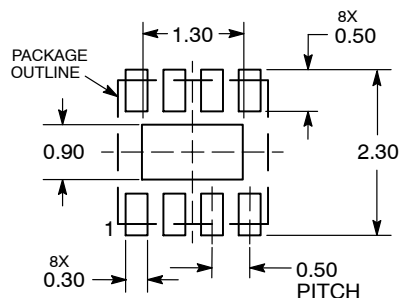
NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.20 MM FROM TERMINAL TIP.
4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.

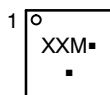
MILLIMETERS		
DIM	MIN	MAX
A	0.80	1.00
A1	0.00	0.05
A3	0.20	REF
b	0.20	0.30
D	2.00	BSC
D2	1.10	1.30
E	2.00	BSC
E2	0.70	0.90
e	0.50	BSC
K	0.30	REF
L	0.25	0.35
L1		0.10



RECOMMENDED SOLDERING FOOTPRINT*



GENERIC MARKING DIAGRAM*



XX = Specific Device Code
M = Date Code
▪ = Pb-Free Device

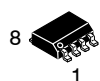
*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "▪", may or may not be present. Some products may not follow the Generic Marking.

*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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DESCRIPTION:	DFN8, 2.0X2.0, 0.5MM PITCH	PAGE 1 OF 1

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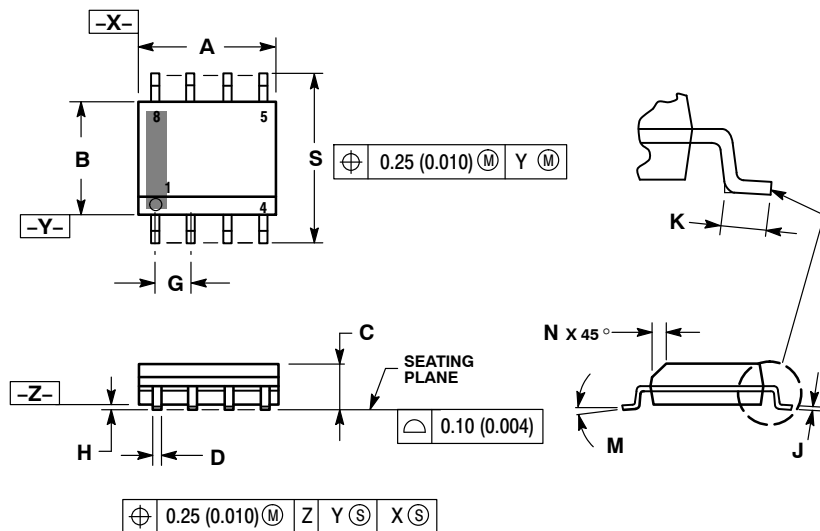
MECHANICAL CASE OUTLINE PACKAGE DIMENSIONS



SCALE 1:1

SOIC-8 NB
CASE 751-07
ISSUE AK

DATE 16 FEB 2011

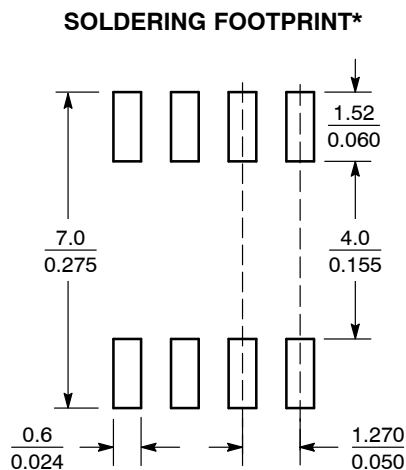


NOTES:

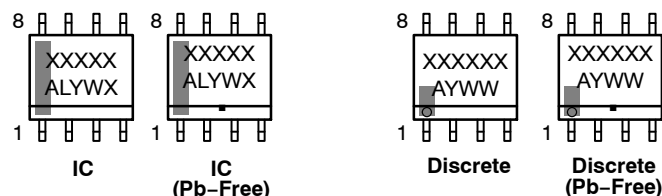
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. 751-01 THRU 751-06 ARE OBSOLETE. NEW STANDARD IS 751-07.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	4.80	5.00	0.189	0.197
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.053	0.069
D	0.33	0.51	0.013	0.020
G	1.27 BSC		0.050 BSC	
H	0.10	0.25	0.004	0.010
J	0.19	0.25	0.007	0.010
K	0.40	1.27	0.016	0.050
M	0°	8°	0°	8°
N	0.25	0.50	0.010	0.020
S	5.80	6.20	0.228	0.244

GENERIC MARKING DIAGRAM*



SCALE 6:1 (mm/inches)



XXXXXX = Specific Device Code
A = Assembly Location
L = Wafer Lot
Y = Year
W = Work Week
■ = Pb-Free Package

XXXXXX = Specific Device Code
A = Assembly Location
Y = Year
WW = Work Week
■ = Pb-Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "■", may or may not be present. Some products may not follow the Generic Marking.

*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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SOIC-8 NB
CASE 751-07
ISSUE AK

DATE 16 FEB 2011

STYLE 1: PIN 1. EMITTER 2. COLLECTOR 3. COLLECTOR 4. EMITTER 5. EMITTER 6. BASE 7. BASE 8. EMITTER	STYLE 2: PIN 1. COLLECTOR, DIE, #1 2. COLLECTOR, #1 3. COLLECTOR, #2 4. COLLECTOR, #2 5. BASE, #2 6. EMITTER, #2 7. BASE, #1 8. EMITTER, #1	STYLE 3: PIN 1. DRAIN, DIE #1 2. DRAIN, #1 3. DRAIN, #2 4. DRAIN, #2 5. GATE, #2 6. SOURCE, #2 7. GATE, #1 8. SOURCE, #1	STYLE 4: PIN 1. ANODE 2. ANODE 3. ANODE 4. ANODE 5. ANODE 6. ANODE 7. ANODE 8. COMMON CATHODE
STYLE 5: PIN 1. DRAIN 2. DRAIN 3. DRAIN 4. DRAIN 5. GATE 6. GATE 7. SOURCE 8. SOURCE	STYLE 6: PIN 1. SOURCE 2. DRAIN 3. DRAIN 4. SOURCE 5. SOURCE 6. GATE 7. GATE 8. SOURCE	STYLE 7: PIN 1. INPUT 2. EXTERNAL BYPASS 3. THIRD STAGE SOURCE 4. GROUND 5. DRAIN 6. GATE 3 7. SECOND STAGE Vd 8. FIRST STAGE Vd	STYLE 8: PIN 1. COLLECTOR, DIE #1 2. BASE, #1 3. BASE, #2 4. COLLECTOR, #2 5. COLLECTOR, #2 6. EMITTER, #2 7. EMITTER, #1 8. COLLECTOR, #1
STYLE 9: PIN 1. EMITTER, COMMON 2. COLLECTOR, DIE #1 3. COLLECTOR, DIE #2 4. EMITTER, COMMON 5. EMITTER, COMMON 6. BASE, DIE #2 7. BASE, DIE #1 8. EMITTER, COMMON	STYLE 10: PIN 1. GROUND 2. BIAS 1 3. OUTPUT 4. GROUND 5. GROUND 6. BIAS 2 7. INPUT 8. GROUND	STYLE 11: PIN 1. SOURCE 1 2. GATE 1 3. SOURCE 2 4. GATE 2 5. DRAIN 2 6. DRAIN 2 7. DRAIN 1 8. DRAIN 1	STYLE 12: PIN 1. SOURCE 2. SOURCE 3. SOURCE 4. GATE 5. DRAIN 6. DRAIN 7. DRAIN 8. DRAIN
STYLE 13: PIN 1. N.C. 2. SOURCE 3. SOURCE 4. GATE 5. DRAIN 6. DRAIN 7. DRAIN 8. DRAIN	STYLE 14: PIN 1. N-SOURCE 2. N-GATE 3. P-SOURCE 4. P-GATE 5. P-DRAIN 6. P-DRAIN 7. N-DRAIN 8. N-DRAIN	STYLE 15: PIN 1. ANODE 1 2. ANODE 1 3. ANODE 1 4. ANODE 1 5. CATHODE, COMMON 6. CATHODE, COMMON 7. CATHODE, COMMON 8. CATHODE, COMMON	STYLE 16: PIN 1. EMITTER, DIE #1 2. BASE, DIE #1 3. EMITTER, DIE #2 4. BASE, DIE #2 5. COLLECTOR, DIE #2 6. COLLECTOR, DIE #2 7. COLLECTOR, DIE #1 8. COLLECTOR, DIE #1
STYLE 17: PIN 1. VCC 2. V2OUT 3. V1OUT 4. TXE 5. RXE 6. VEE 7. GND 8. ACC	STYLE 18: PIN 1. ANODE 2. ANODE 3. SOURCE 4. GATE 5. DRAIN 6. DRAIN 7. CATHODE 8. CATHODE	STYLE 19: PIN 1. SOURCE 1 2. GATE 1 3. SOURCE 2 4. GATE 2 5. DRAIN 2 6. MIRROR 2 7. DRAIN 1 8. MIRROR 1	STYLE 20: PIN 1. SOURCE (N) 2. GATE (N) 3. SOURCE (P) 4. GATE (P) 5. DRAIN 6. DRAIN 7. DRAIN 8. DRAIN
STYLE 21: PIN 1. CATHODE 1 2. CATHODE 2 3. CATHODE 3 4. CATHODE 4 5. CATHODE 5 6. COMMON ANODE 7. COMMON ANODE 8. CATHODE 6	STYLE 22: PIN 1. I/O LINE 1 2. COMMON CATHODE/VCC 3. COMMON CATHODE/VCC 4. I/O LINE 3 5. COMMON ANODE/GND 6. I/O LINE 4 7. I/O LINE 5 8. COMMON ANODE/GND	STYLE 23: PIN 1. LINE 1 IN 2. COMMON ANODE/GND 3. COMMON ANODE/GND 4. LINE 2 IN 5. LINE 2 OUT 6. COMMON ANODE/GND 7. COMMON ANODE/GND 8. LINE 1 OUT	STYLE 24: PIN 1. BASE 2. EMITTER 3. COLLECTOR/ANODE 4. COLLECTOR/ANODE 5. CATHODE 6. CATHODE 7. COLLECTOR/ANODE 8. COLLECTOR/ANODE
STYLE 25: PIN 1. VIN 2. N/C 3. REXT 4. GND 5. IOUT 6. IOUT 7. IOUT 8. IOUT	STYLE 26: PIN 1. GND 2. dv/dt 3. ENABLE 4. ILIMIT 5. SOURCE 6. SOURCE 7. SOURCE 8. VCC	STYLE 27: PIN 1. ILIMIT 2. OVLO 3. UVLO 4. INPUT+ 5. SOURCE 6. SOURCE 7. SOURCE 8. DRAIN	STYLE 28: PIN 1. SW_TO_GND 2. DASIC_OFF 3. DASIC_SW_DET 4. GND 5. V_MON 6. VBULK 7. VBULK 8. VIN
STYLE 29: PIN 1. BASE, DIE #1 2. EMITTER, #1 3. BASE, #2 4. EMITTER, #2 5. COLLECTOR, #2 6. COLLECTOR, #2 7. COLLECTOR, #1 8. COLLECTOR, #1	STYLE 30: PIN 1. DRAIN 1 2. DRAIN 1 3. GATE 2 4. SOURCE 2 5. SOURCE 1/DRAIN 2 6. SOURCE 1/DRAIN 2 7. SOURCE 1/DRAIN 2 8. GATE 1		

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