85C72/82/92

1K/2K/4K 5.0V I²C™ Serial EEPROM

FEATURES

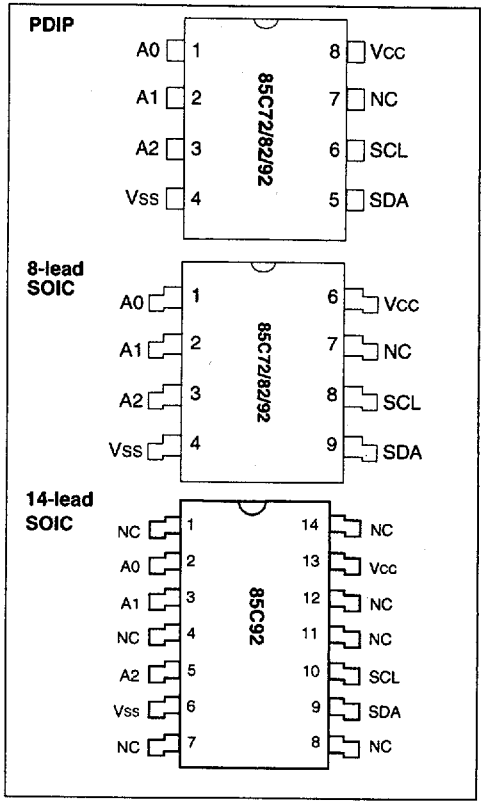
- Low power CMOS technology
- 2-wire serial interface bus, I²C™ compatible
- 5 volt only operation
- Self-timed write cycle (including auto-erase)
- Page-write buffer
- 1ms write cycle time for single byte
- 1,000,000 erase/write cycles guaranteed
- Data retention >200 years
- 8-pin DIP or SOIC package
- Available for extended temperature ranges
  - Commercial (C): 0°C to 70°C
  - Industrial (I): -40°C to +85°C
  - Automotive (E): -40°C to +125°C

	85C72	85C82	85C92
Organization	128 x 8	256 x 8	2 x 256 x 8
Page Write Buffer	2 Bytes	2 Bytes	8 Bytes

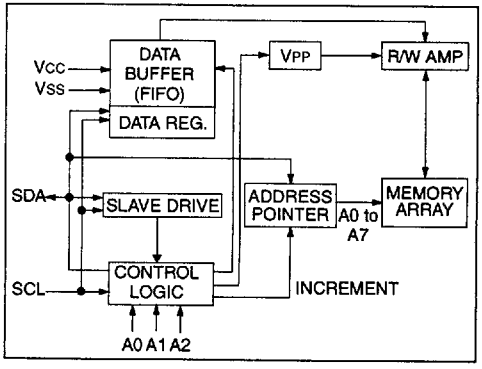
DESCRIPTION

The Microchip Technology Inc. 85C72/82/92 is a 1K/2K/4K bit Electrically Erasable PROM. The device is organized as shown with a 2-wire serial interface. Advanced CMOS technology allows a significant reduction in power over NMOS serial devices. The 85C72/82/92 also has a page-write capability for up to 8 bytes of data (see chart). Up to eight 85C72/82/92s may be connected to the two wire bus. The 85C72/82/92 is available in standard 8-pin DIP and surface mount SOIC packages.

PACKAGE TYPES



BLOCK DIAGRAM



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1.0 ELECTRICAL CHARACTERISTICS

1.1 Maximum Ratings*

VCC.....7.0V
All inputs and outputs w.r.t. VSS .....-0.6V to VCC +1.0V
Storage temperature .....-65°C to +150°C
Ambient temp. with power applied.....-65°C to +125°C
Soldering temperature of leads (10 seconds) .....+300°C
ESD protection on all pins.....4 kV

*Notice: Stresses above those listed under "Maximum ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operational listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

TABLE 1-1: PIN FUNCTION TABLE

Name	Function
A0, A1, A2	Chip Address Inputs
VSS	Ground
SDA	Serial Address/Data Input/Output
SCL	Serial Clock
NC	No Connect
VCC	+5V Power Supply

TABLE 1-2: DC CHARACTERISTICS

VCC = +5V (10%)			Commercial (C): Tamb = 0°C to +70°C Industrial (I): Tamb = -40°C to +85°C Automotive (E): Tamb = -40°C to 125°C		
Parameter	**Symbol**	**Min**	**Max**	**Units**	**Conditions**
VCC detector threshold	VTH	2.8	4.5	V	
SCL and SDA pins:					
High level input voltage	VIH	VCC x 0.7	VCC + 1	V	
Low level input voltage	VIL	-0.3	VCC x 0.3	V	
Low level output voltage	VOL		0.4	V	IOL = 3.2 mA (SDA Only)
A0, A1 & A2 pins:					
HIgh level input voltage	VIH	VCC - 0.5	VCC + 0.5	V	
Low level input voltage	VIL	-0.3	0.5	V	
Input leakage current	ILI	—	10	µA	VIN = 0V TO VCC
Output leakage current	ILO	—	10	µA	VOUT = 0V TO VCC
Pin capacitance (all inputs/outputs)	CIN, COUT	—	7.0	pF	VIN/VOUT = 0V (Note 1) Tamb = +25°C, f = 1 MHz
Operating current	ICCO	—	3.5	mA	FCLK = 100 kHz, program cycle time = 1 ms, VCC = 5V, Tamb = 0°C to +70°C
			4.25	mA	FCLK = 100 kHz, program cycle time = 1 ms, VCC = 5V, Tamb = (I) and (E)
read cycle	ICCR	—	750	µA	VCC = 5V, Tamb = (C), (I) and (E)
Standby current	ICCS	—	100	µA	SDA=SCL=VCC=5V (no PROGRAM active)

Note: This parameter is periodically sampled and not 100% tested.

FIGURE 1-1: BUS TIMING START/STOP

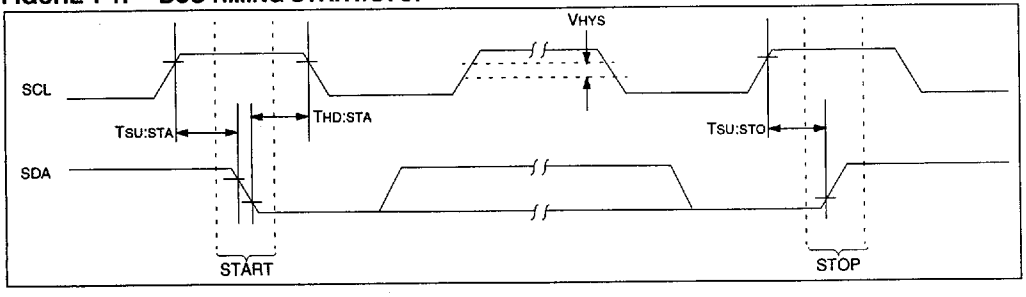


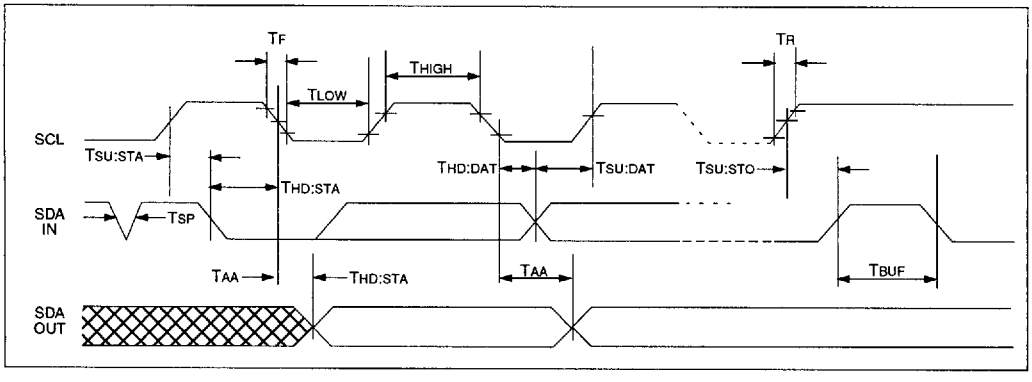
TABLE 1-3: AC CHARACTERISTICS

Parameter	Symbol	Min	Typ	Max	Units	Remarks
Clock frequency	FCLK	—	—	100	kHz	
Clock high time	THIGH	4000	—	—	ns	
Clock low time	TLOW	4700	—	—	ns	
SDA and SCL rise time	TR	—	—	1000	ns	
SDA and SCL fall time	TF	—	—	300	ns	
START condition hold time	THD:STA	4000	—	—	ns	After this period the first clock pulse is generated
START condition setup time	TSU:STA	4700	—	—	ns	Only relevant for repeated START condition
Data input hold time	THD:DAT	0	—	—	ns	
Data input setup time	TSU:DAT	250	—	—	ns	
Data output delay time	TPD	300	—	3500	ns	(Note 1)
STOP condition setup time	TSU:STO	4700	—	—	ns	
Bus free time	TBUF	4700	—	—	ns	Time the bus must be free before a new transmission can start
Input filter time constant (SDA and SCL pins)	TI	—	—	100	ns	
Program cycle time	TWC	—	.4 .4N	1 N	ms ms	Byte Mode Page Mode, N = # of bytes to be written
Endurance	—	1M	—	—	cycles	25°C, Vcc = 5.0V, Block Mode (Note 2)

Note 1: As transmitter the device must provide this internal minimum delay time to bridge the undefined region (minimum 300 ns) of the falling edge of SCL to avoid unintended generation of START or STOP conditions.

2: This application is not tested but guaranteed by characterization. For endurance estimates in a specific application, please consult the Total Endurance Model which can be obtained on our BBS or website.

FIGURE 1-2: BUS TIMING DATA



2.0 FUNCTIONAL DESCRIPTION

The 85C72/82/92 supports a bidirectional two wire bus and data transmission protocol. A device that sends data onto the bus is defined as transmitter, and a device receiving data as receiver. The bus has to be controlled by a master device which generates the serial clock (SCL), controls the bus access, and generates the START and STOP conditions, while the 85C72/82/92 works as slave. Both, master and slave can operate as transmitter or receiver, but the master device determines which mode is activated.

Up to eight 85C72/82/92s can be connected to the bus, selected by the A0, A1 and A2 chip address inputs. Other devices can be connected to the bus, but require different device codes than the 85C72/82/92 (refer to section Slave Address).

3.0 BUS CHARACTERISTICS

The following **bus protocol** has been defined:

- Data transfer may be initiated only when the bus is not busy.
- During data transfer, the data line must remain stable whenever the clock line is HIGH. Changes in the data line while the clock line is HIGH will be interpreted as a START or STOP condition.

Accordingly, the following bus conditions have been defined (Figure 3-1).

3.1 Bus not Busy (A)

Both data and clock lines remain HIGH.

3.2 Start Data Transfer (B)

A HIGH to LOW transition of the SDA line while the clock (SCL) is HIGH determines a START condition. All commands must be preceded by a START condition.

3.3 Stop Data Transfer (C)

A LOW to HIGH transition of the SDA line while the clock (SCL) is HIGH determines a STOP condition. All operations must be ended with a STOP condition.

3.4 Data Valid (D)

The state of the data line represents valid data when, after a start condition, the data line is stable for the duration of the HIGH period of the clock signal.

The data on the line must be changed during the LOW period of the clock signal. There is one clock pulse per bit of data.

Each data transfer is initiated with a START condition and terminated with a STOP condition. The number of the data bytes transferred between the START and STOP conditions is determined by the master device and is theoretically unlimited.

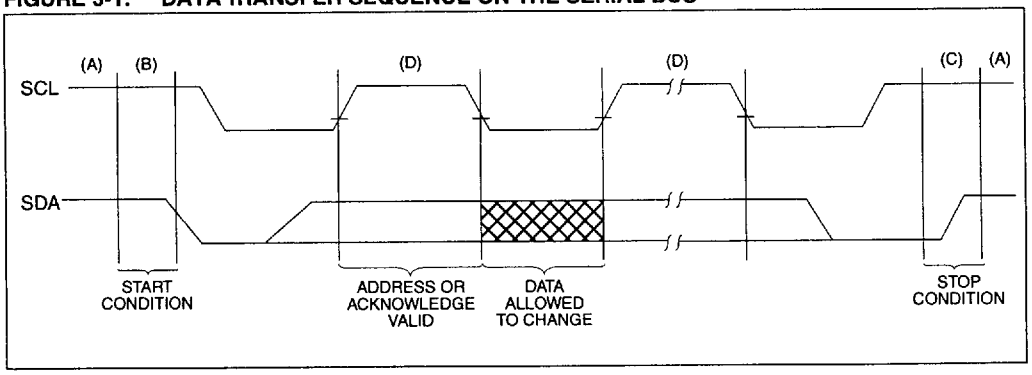
3.5 Acknowledge

Each receiving device, when addressed, is obliged to generate an acknowledge after the reception of each byte. The master device must generate an extra clock pulse which is associated with this acknowledge bit.

Note: The 85C72/82/92 does not generate any acknowledge bits if an internal programming cycle is in progress.

The device that acknowledges, has to pull down the SDA line during the acknowledge clock pulse in such a way that the SDA line is stable LOW during the HIGH period of the acknowledge related clock pulse. Of course, setup and hold times must be taken into account. A master must signal an end of data to the slave by not generating an acknowledge bit on the last byte that has been clocked out of the slave. In this case the slave must leave the data line HIGH to enable the master to generate the STOP condition

FIGURE 3-1: DATA TRANSFER SEQUENCE ON THE SERIAL BUS



4.0 SLAVE ADDRESS

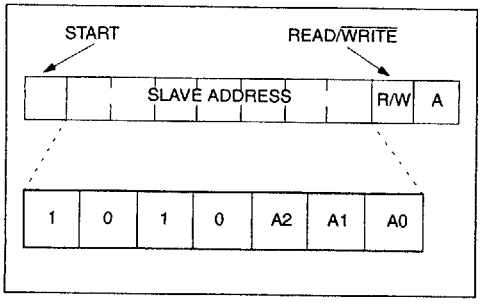
The chip address inputs A0, A1 and A2 of each 85C72/82/92 must be externally connected to either Vcc or ground (Vss), assigning to each 85C72/82/92 a unique 3-bit address. Up to eight 85C72/82/92s may be connected to the bus. Chip selection is then accomplished through software by setting the bits A0, A1 and A2 of the transmitted slave address to the corresponding hardwired logic levels of the selected 85C72/82/92.

After generating a START condition, the bus master transmits the slave address consisting of a 4-bit device code (1010) for the 85C72/82/92, followed by the chip address bits A0, A1 and A2. In the 85C92 the seventh bit of that byte (BA) is used to select the upper block (addresses 100 - 1FF) or the lower block (000 - FFF) of the array.

The eighth bit of slave address determines if the master device wants to read or write to the 85C72/82/92 (Figure 4-1).

The 85C72/82/92 monitors the bus for its corresponding slave address all the time. It generates an acknowledge bit if the slave address was true and it is not in a programming mode.

FIGURE 4-1: SLAVE ADDRESS ALLOCATION



5.0 BYTE PROGRAM MODE

In this mode, the master sends addresses and one data byte to the 85C72/82/92.

Following the START condition, the device code (4-bit), the slave address (3-bit), and the R/$\overline{W}$ bit, which is logic LOW, are placed onto the bus by the master. This indicates to the addressed 85C72/82/92 that a byte with a word address will follow after it has generated an acknowledge bit. Therefore, the next byte transmitted by the master is the word address and will be written into the address pointer of the 85C72/82/92. After receiving the acknowledge of the 85C72/82/92, the master device transmits the data word to be written into the addressed memory location. The 85C72/82/92 acknowledges again and the master generates a STOP condition. This initiates the internal programming cycle of the 85C72/82/92 (Figure 6-1).

6.0 PAGE PROGRAM MODE

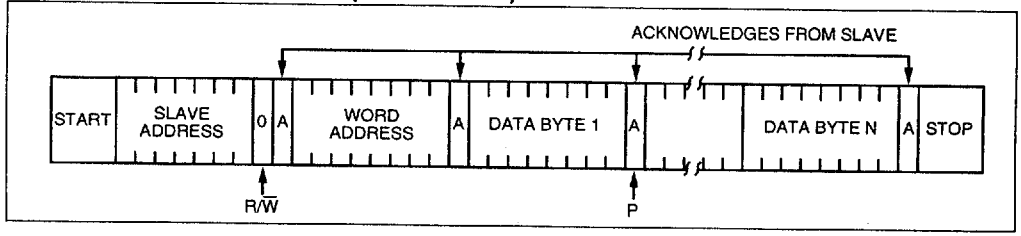
To program the 85C72/82/92, the master sends addresses and data to the 85C72/82/92 which is the slave (Figure 6-1). This is done by supplying a START condition followed by the 4-bit device code, the 3-bit slave address, and the R/$\overline{W}$ bit which is defined as a logic LOW for a write. This indicates to the addressed slave that a word address will follow so the slave outputs the acknowledge pulse to the master during the ninth clock pulse. When the word address is received by the 85C72/82/92, it places it in the lower 8 bits of the address pointer defining which memory location is to be written. The 85C72/82/92 will generate an acknowledge after every 8 bits received and store them consecutively in a 2-byte RAM until a stop condition is detected which initiates the internal programming cycle. If more than 2 bytes are transmitted by the master, the 85C72/82/92 will terminate the write cycle. This does not affect erase/write cycles of the EEPROM array.

If the master generates a STOP condition after transmitting the first data word (Point 'P' on Figure 6-1), byte programming mode is entered.

The internal, completely self-timed PROGRAM cycle starts after the STOP condition has been generated by the master and all received (up to two) data bytes will be written in a serial manner.

The PROGRAM cycle takes N milliseconds, whereby N is the number of received data bytes (N max = 2).

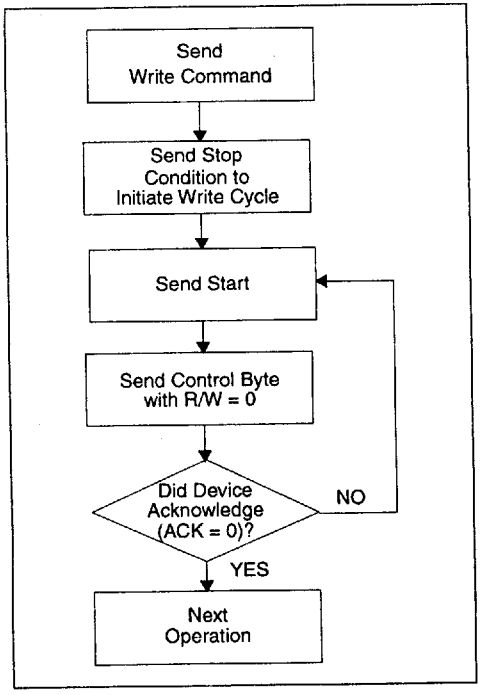
FIGURE 6-1: PROGRAM MODE (ERASE/WRITE)



7.0 ACKNOWLEDGE POLLING

Since the device will not acknowledge during a write cycle, this can be used to determine when the cycle is complete (this feature can be used to maximize bus throughput). Once the stop condition for a write command has been issued from the master, the device initiates the internally timed write cycle. ACK polling can be initiated immediately. This involves the master sending a start condition followed by the control byte for a write command ($R/\overline{W} = 0$). If the device is still busy with the write cycle, then no ACK will be returned. If the cycle is complete, then the device will return the ACK and the master can then proceed with the next read or write command. See Figure 7-1 for flow diagram.

FIGURE 7-1: ACKNOWLEDGE POLLING FLOW



8.0 READ MODE

This mode illustrates master device reading data from the 85C72/82/92.

As can be seen from Figure 8-1, the master first sets up the slave and word addresses by doing a write.

Note: Although this is a read mode, the address pointer must be written to.

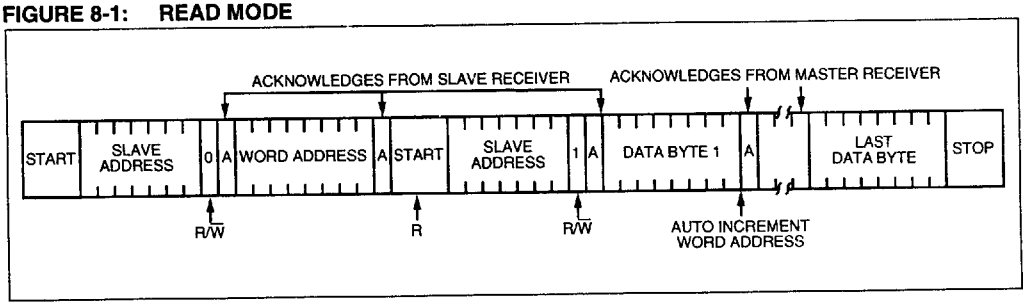
During this period the 85C72/82/92 generates the necessary acknowledge bits as defined in the appropriate section.

The master now generates another START condition and transmits the slave address again, except this time the read/write bit is set into the read mode. After the slave generates the acknowledge bit, it then outputs the data from the addressed location on to the SDA pin, increments the address pointer and, if it receives an acknowledge from the master, will transmit the next consecutive byte. This autoincrement sequence is only aborted when the master sends a STOP condition instead of an acknowledge.

Note 1: If the master knows where the address pointer is, it can begin the read sequence at point 'R' indicated on Figure 8-1 and save time transmitting the slave and word addresses.

Note 2: In all modes, the address pointer will automatically increment from the end of the memory block (256 byte) back to the first location in that block.

FIGURE 8-1: READ MODE



9.0 PIN DESCRIPTION

9.1 A0, A1 and A2 Chip Address Inputs

The levels on these inputs are compared with the corresponding bits in the slave address. The chip is selected if the compare is true. For 85C92, A0 is no function.

Up to eight 85C72/82s or four 85C92s can be connected to the bus.

These inputs must be connected to either VSS or VCC.

9.2 SDA Serial Address/Data Input/Output

This is a bidirectional pin used to transfer addresses and data into and data out of the device. It is an open drain terminal, therefore the SDA bus requires a pullup resistor to VCC (typical 10KW). For normal data transfer SDA is allowed to change only during SCL LOW. Changes during SCL HIGH are reserved for indicating the START and STOP conditions.

9.3 SCL Serial Clock

This input is used to synchronize the data transfer from and to the device.

9.4 NC No Connect

This pin can be left open or used as a tie point.

Note 1: A "page" is defined as the maximum number of bytes that can be programmed in a single write cycle. The 85C72/82 page is 2 bytes long and the 85C92 page is 8 bytes long.

Note 2: A "block" is defined as a continuous area of memory with distinct boundaries. The address pointer can not cross the boundary from one block to another. It will, however, wrap around from the end of a block to the first location in the same block. The 85C72/82 has only one block (256 bytes), while the 85C92 has two blocks of 256 bytes each.

85C72/82/92 Product Identification System

To order or to obtain information, e.g., on pricing or delivery, please use the listed part numbers, and refer to the factory or the listed sales offices.