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# Field Effect Transistor - N-Channel, Enhancement Mode

## 2N7002DW

### Features

- Dual N-Channel MOSFET
- Low On-Resistance
- Low Gate Threshold Voltage
- Low Input Capacitance
- Fast Switching Speed
- Low Input/Output Leakage
- Ultra-Small Surface Mount Package
- These Devices are Pb-Free, Halogen Free/BFR Free and are RoHS Compliant

### ABSOLUTE MAXIMUM RATINGS ( $T_A = 25^\circ\text{C}$ unless otherwise noted)

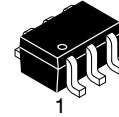
| Symbol         | Parameter                                                | Ratings                           | Units            |
|----------------|----------------------------------------------------------|-----------------------------------|------------------|
| $V_{DSS}$      | Drain-Source Voltage                                     | 60                                | V                |
| $V_{DGR}$      | Drain-Gate Voltage ( $R_{GS} \leq 1.0 \text{ M}\Omega$ ) | 60                                | V                |
| $V_{GSS}$      | Gate-Source Voltage                                      | Continuous                        | $\pm 20$         |
|                |                                                          | Pulsed                            | $\pm 40$         |
| $I_D$          | Drain Current                                            | Continuous                        | 115              |
|                |                                                          | Continuous at $100^\circ\text{C}$ | 73               |
|                |                                                          | Pulsed                            | 800              |
| $T_J, T_{STG}$ | Junction and Storage Temperature Range                   | $-55$ to $+150$                   | $^\circ\text{C}$ |

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

### THERMAL CHARACTERISTICS ( $T_A = 25^\circ\text{C}$ unless otherwise noted)

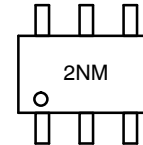
| Symbol          | Parameter                                        | Ratings | Unit                 |
|-----------------|--------------------------------------------------|---------|----------------------|
| $P_D$           | Total Device Dissipation                         | 200     | mW                   |
|                 | Derate Above $T_A = 25^\circ\text{C}$            | 1.6     | mW/ $^\circ\text{C}$ |
| $R_{\theta JA}$ | Thermal Resistance, Junction-to-Ambient (Note 1) | 415     | $^\circ\text{C/W}$   |

1. Device mounted on FR-4 PCB, 1 inch x 0.85 inch x 0.062 inch. Minimum land pad size.



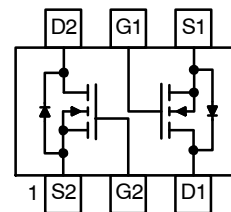
SC-88/SC70-6/SOT-363  
CASE 419B-02

### MARKING DIAGRAM



2N = Specific Device Code  
M = Assembly Operation Month

### PIN CONNECTIONS



### ORDERING INFORMATION

See detailed ordering and shipping information on page 2 of this data sheet.

## ORDERING INFORMATION

| Part Number | Top Mark | Package             | Shipping <sup>†</sup> |
|-------------|----------|---------------------|-----------------------|
| 2N7002DW    | 2N       | SC70-6<br>(Pb-Free) | 3000 / Tape & Reel    |

<sup>†</sup>For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

ELECTRICAL CHARACTERISTICS ( $T_A = 25^\circ\text{C}$  unless otherwise noted)

| Symbol | Parameter | Test Conditions | Min | Typ | Max | Unit |
|--------|-----------|-----------------|-----|-----|-----|------|
|--------|-----------|-----------------|-----|-----|-----|------|

## OFF CHARACTERISTICS (Note 2)

|            |                                 |                                                                      |    |       |          |               |
|------------|---------------------------------|----------------------------------------------------------------------|----|-------|----------|---------------|
| $BV_{DSS}$ | Drain-Source Breakdown Voltage  | $V_{GS} = 0\text{ V}, I_D = 10\text{ }\mu\text{A}$                   | 60 | 78    | –        | V             |
| $I_{DSS}$  | Zero Gate Voltage Drain Current | $V_{DS} = 60\text{ V}, V_{GS} = 0\text{ V}$                          | –  | 0.001 | 1.0      | $\mu\text{A}$ |
|            |                                 | $V_{DS} = 60\text{ V}, V_{GS} = 0\text{ V}, T_J = 125^\circ\text{C}$ | –  | 7     | 500      |               |
| $I_{GSS}$  | Gate-Body Leakage               | $V_{GS} = \pm 20\text{ V}, V_{DS} = 0\text{ V}$                      | –  | 0.2   | $\pm 10$ | nA            |

## ON CHARACTERISTICS (Note 2)

|              |                                   |                                                                     |      |       |      |          |
|--------------|-----------------------------------|---------------------------------------------------------------------|------|-------|------|----------|
| $V_{GS(th)}$ | Gate Threshold Voltage            | $V_{DS} = V_{GS}, I_D = 250\text{ }\mu\text{A}$                     | 1.00 | 1.76  | 2.0  | V        |
| $R_{DS(on)}$ | Static Drain-Source On-Resistance | $V_{GS} = 5\text{ V}, I_D = 0.05\text{ A}$                          | –    | 1.6   | 7.5  | $\Omega$ |
|              |                                   | $V_{GS} = 10\text{ V}, I_D = 0.5\text{ A}$                          | –    | –     | 2.0  |          |
|              |                                   | $V_{GS} = 10\text{ V}, I_D = 0.5\text{ A}, T_J = 125^\circ\text{C}$ | –    | 2.53  | 13.5 |          |
|              |                                   |                                                                     |      |       |      |          |
| $I_{D(on)}$  | On-State Drain Current            | $V_{GS} = 10\text{ V}, V_{DS} = 7.5\text{ V}$                       | 0.50 | 1.43  | –    | A        |
| $g_{FS}$     | Forward Transconductance          | $V_{DS} = 10\text{ V}, I_D = 0.2\text{ A}$                          | 80.0 | 356.5 | –    | mS       |

## DYNAMIC CHARACTERISTICS

|           |                              |                                                                 |   |      |    |    |
|-----------|------------------------------|-----------------------------------------------------------------|---|------|----|----|
| $C_{iss}$ | Input Capacitance            | $V_{DS} = 25\text{ V}, V_{GS} = 0\text{ V}, f = 1.0\text{ MHz}$ | – | 37.8 | 50 | pF |
| $C_{oss}$ | Output Capacitance           |                                                                 | – | 12.4 | 25 | pF |
| $C_{rss}$ | Reverse Transfer Capacitance |                                                                 | – | 6.5  | 7  | pF |

## SWITCHING CHARACTERISTICS (Note 2)

|              |                     |                                                                                                                        |   |      |    |    |
|--------------|---------------------|------------------------------------------------------------------------------------------------------------------------|---|------|----|----|
| $t_{D(ON)}$  | Turn-On Delay Time  | $V_{DD} = 30\text{ V}, I_D = 0.2\text{ A}, V_{GEN} = 10\text{ V}, R_L = 150\text{ }\Omega, R_{GEN} = 25\text{ }\Omega$ | – | 5.85 | 20 | ns |
| $t_{D(OFF)}$ | Turn-Off Delay Time |                                                                                                                        | – | 12.5 | 20 | ns |

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

2. Short duration test pulse used to minimize self-heating effect.

## TYPICAL PERFORMANCE CHARACTERISTICS

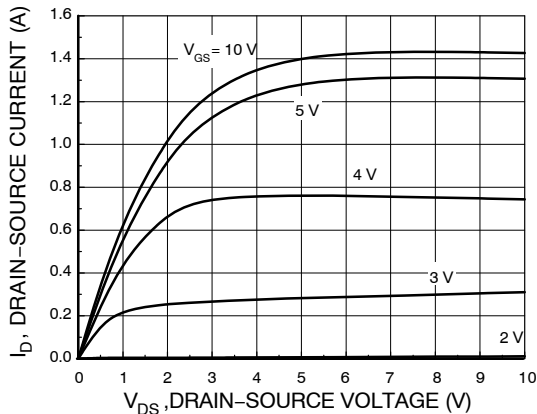


Figure 1. On-Region Characteristics

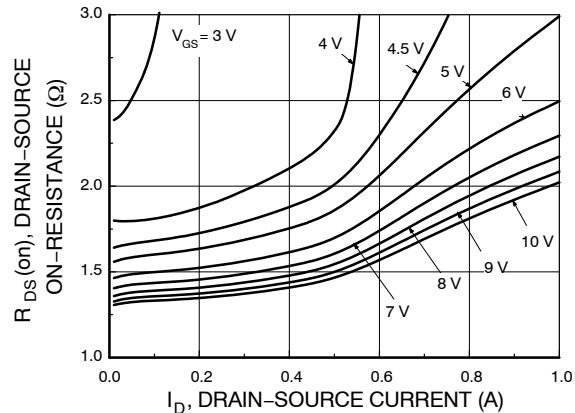


Figure 2. On-Resistance Variation with Gate Voltage and Drain Current

TYPICAL PERFORMANCE CHARACTERISTICS (continued)

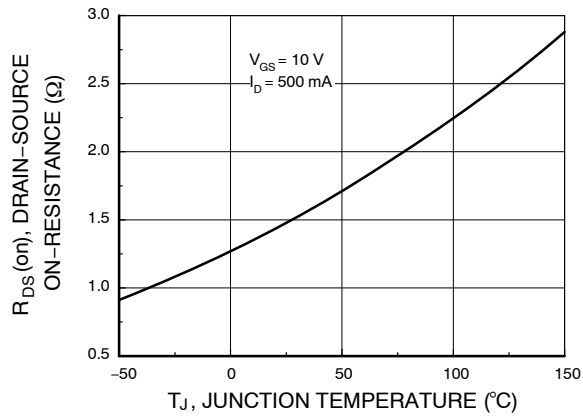


Figure 3. On-Resistance Variation with Temperature

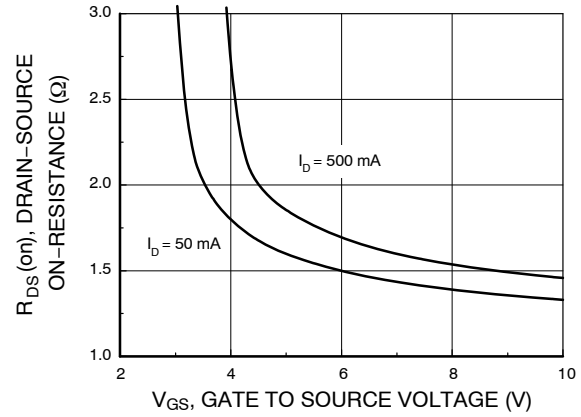


Figure 4. On-Resistance Variation with Gate-Source Voltage

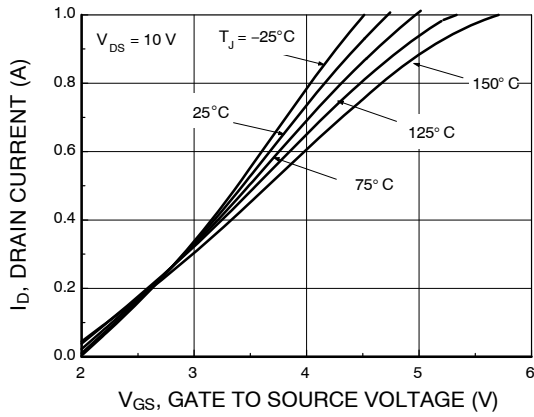


Figure 5. Transfer Characteristics

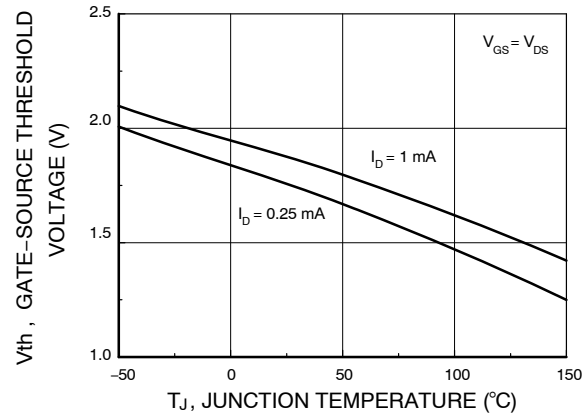


Figure 6. Gate Threshold Variation with Temperature

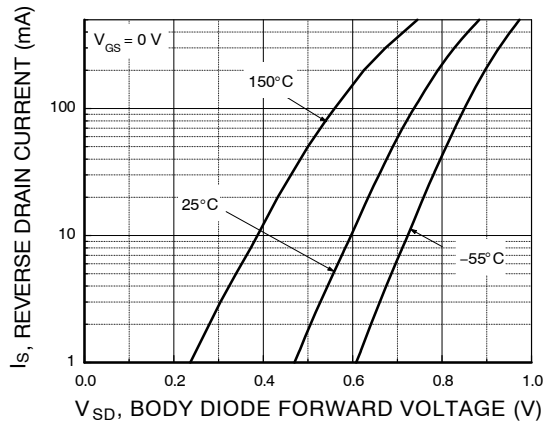


Figure 7. Reverse Drain Current Variation with Diode Forward Voltage and Temperature

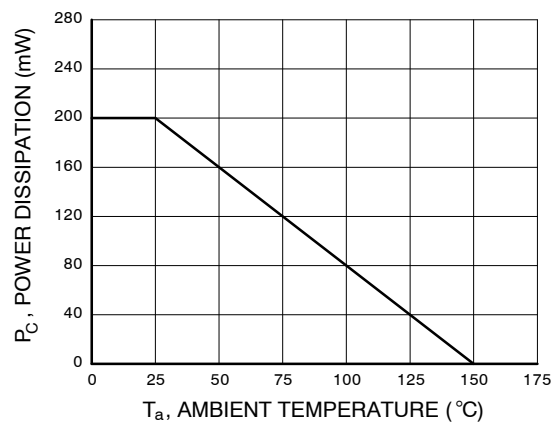


Figure 8. Power Derating



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NOTES:

1. DIMENSIONING AND TOLERANCING CONFORM TO ASME Y14.5-2018.
2. ALL DIMENSION ARE IN MILLIMETERS.
3. DIMENSIONS D AND E1 DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS. MOLD FLASH, PROTRUSIONS, OR GATE BURRS SHALL NOT EXCEED 0.20 PER END.
4. DIMENSIONS D AND E1 AT THE OUTERMOST EXTREMES OF THE PLASTIC BODY AND DATUM H.
5. DATUMS A AND B ARE DETERMINED AT DATUM H.
6. DIMENSIONS b AND c APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN 0.08 AND 0.15 FROM THE TIP.
7. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 TOTAL IN EXCESS OF DIMENSION b AT MAXIMUM MATERIAL CONDITION. THE DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OF THE FOOT.



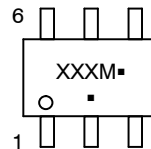
| DIM | MILLIMETERS |      |      |
|-----|-------------|------|------|
|     | MIN.        | NOM. | MAX. |
| A   | ---         | ---  | 1.10 |
| A1  | 0.00        | ---  | 0.10 |
| A2  | 0.70        | 0.90 | 1.00 |
| b   | 0.15        | 0.20 | 0.25 |
| c   | 0.08        | 0.15 | 0.22 |
| D   | 2.00 BSC    |      |      |
| E   | 2.10 BSC    |      |      |
| E1  | 1.25 BSC    |      |      |
| e   | 0.65 BSC    |      |      |
| L   | 0.26        | 0.36 | 0.46 |
| L2  | 0.15 BSC    |      |      |
| aaa | 0.15        |      |      |
| bbb | 0.30        |      |      |
| ccc | 0.10        |      |      |
| ddd | 0.10        |      |      |



RECOMMENDED MOUNTING FOOTPRINT\*

\* FOR ADDITIONAL INFORMATION ON OUR Pb-FREE STRATEGY AND SOLDERING DETAILS, PLEASE DOWNLOAD THE ONSEMI SOLDERING AND MOUNTING TECHNIQUES REFERENCE MANUAL, SOLDERRM/D.

GENERIC  
MARKING DIAGRAM\*



XXX = Specific Device Code  
M = Date Code\*  
▪ = Pb-Free Package

(Note: Microdot may be in either location)

\*Date Code orientation and/or position may vary depending upon manufacturing location.

\*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "▪", may or may not be present. Some products may not follow the Generic Marking.

STYLES ON PAGE 2

|                  |                             |                                                                                                                                                                                  |
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|                                                                                                            |                                                                                                        |                                                                                                             |                                                                                                             |                                                                                                             |                                                                                                       |
|------------------------------------------------------------------------------------------------------------|--------------------------------------------------------------------------------------------------------|-------------------------------------------------------------------------------------------------------------|-------------------------------------------------------------------------------------------------------------|-------------------------------------------------------------------------------------------------------------|-------------------------------------------------------------------------------------------------------|
| STYLE 1:<br>PIN 1. EMITTER 2<br>2. BASE 2<br>3. COLLECTOR 1<br>4. EMITTER 1<br>5. BASE 1<br>6. COLLECTOR 2 | STYLE 2:<br>CANCELLED                                                                                  | STYLE 3:<br>CANCELLED                                                                                       | STYLE 4:<br>PIN 1. CATHODE<br>2. CATHODE<br>3. COLLECTOR<br>4. EMITTER<br>5. BASE<br>6. ANODE               | STYLE 5:<br>PIN 1. ANODE<br>2. ANODE<br>3. COLLECTOR<br>4. EMITTER<br>5. BASE<br>6. CATHODE                 | STYLE 6:<br>PIN 1. ANODE 2<br>2. N/C<br>3. CATHODE 1<br>4. ANODE 1<br>5. N/C<br>6. CATHODE 2          |
| STYLE 7:<br>PIN 1. SOURCE 2<br>2. DRAIN 2<br>3. GATE 1<br>4. SOURCE 1<br>5. DRAIN 1<br>6. GATE 2           | STYLE 8:<br>CANCELLED                                                                                  | STYLE 9:<br>PIN 1. EMITTER 2<br>2. EMITTER 1<br>3. COLLECTOR 1<br>4. BASE 1<br>5. BASE 2<br>6. COLLECTOR 2  | STYLE 10:<br>PIN 1. SOURCE 2<br>2. SOURCE 1<br>3. GATE 1<br>4. DRAIN 1<br>5. DRAIN 2<br>6. GATE 2           | STYLE 11:<br>PIN 1. CATHODE 2<br>2. CATHODE 2<br>3. ANODE 1<br>4. CATHODE 1<br>5. CATHODE 1<br>6. ANODE 2   | STYLE 12:<br>PIN 1. ANODE 2<br>2. ANODE 2<br>3. CATHODE 1<br>4. ANODE 1<br>5. ANODE 1<br>6. CATHODE 2 |
| STYLE 13:<br>PIN 1. ANODE<br>2. N/C<br>3. COLLECTOR<br>4. EMITTER<br>5. BASE<br>6. CATHODE                 | STYLE 14:<br>PIN 1. VREF<br>2. GND<br>3. GND<br>4. IOUT<br>5. VEN<br>6. VCC                            | STYLE 15:<br>PIN 1. ANODE 1<br>2. ANODE 2<br>3. ANODE 3<br>4. CATHODE 3<br>5. CATHODE 2<br>6. CATHODE 1     | STYLE 16:<br>PIN 1. BASE 1<br>2. EMITTER 2<br>3. COLLECTOR 2<br>4. BASE 2<br>5. EMITTER 1<br>6. COLLECTOR 1 | STYLE 17:<br>PIN 1. BASE 1<br>2. EMITTER 1<br>3. COLLECTOR 2<br>4. BASE 2<br>5. EMITTER 2<br>6. COLLECTOR 1 | STYLE 18:<br>PIN 1. VIN1<br>2. VCC<br>3. VOUT2<br>4. VIN2<br>5. GND<br>6. VOUT1                       |
| STYLE 19:<br>PIN 1. I OUT<br>2. GND<br>3. GND<br>4. V CC<br>5. V EN<br>6. V REF                            | STYLE 20:<br>PIN 1. COLLECTOR<br>2. COLLECTOR<br>3. BASE<br>4. EMITTER<br>5. COLLECTOR<br>6. COLLECTOR | STYLE 21:<br>PIN 1. ANODE 1<br>2. N/C<br>3. ANODE 2<br>4. CATHODE 2<br>5. N/C<br>6. CATHODE 1               | STYLE 22:<br>PIN 1. D1 (i)<br>2. GND<br>3. D2 (i)<br>4. D2 (c)<br>5. VBUS<br>6. D1 (c)                      | STYLE 23:<br>PIN 1. Vn<br>2. CH1<br>3. Vp<br>4. N/C<br>5. CH2<br>6. N/C                                     | STYLE 24:<br>PIN 1. CATHODE<br>2. ANODE<br>3. CATHODE<br>4. CATHODE<br>5. CATHODE<br>6. CATHODE       |
| STYLE 25:<br>PIN 1. BASE 1<br>2. CATHODE<br>3. COLLECTOR 2<br>4. BASE 2<br>5. EMITTER<br>6. COLLECTOR 1    | STYLE 26:<br>PIN 1. SOURCE 1<br>2. GATE 1<br>3. DRAIN 2<br>4. SOURCE 2<br>5. GATE 2<br>6. DRAIN 1      | STYLE 27:<br>PIN 1. BASE 2<br>2. BASE 1<br>3. COLLECTOR 1<br>4. EMITTER 1<br>5. EMITTER 2<br>6. COLLECTOR 2 | STYLE 28:<br>PIN 1. DRAIN<br>2. DRAIN<br>3. GATE<br>4. SOURCE<br>5. DRAIN<br>6. DRAIN                       | STYLE 29:<br>PIN 1. ANODE<br>2. ANODE<br>3. COLLECTOR<br>4. EMITTER<br>5. BASE/ANODE<br>6. CATHODE          | STYLE 30:<br>PIN 1. SOURCE 1<br>2. DRAIN 2<br>3. DRAIN 2<br>4. SOURCE 2<br>5. GATE 1<br>6. DRAIN 1    |

Note: Please refer to datasheet for style callout. If style type is not called out in the datasheet refer to the device datasheet pinout or pin assignment.

|                  |                             |                                                                                                                                                                                     |
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