

TS5A22362 0.65-Ω 2-channel SPDT Analog Switches With Negative Signaling Capability

1 Features

- Specified break-before-make switching
- Negative signaling capability: maximum swing from -2.75 V to 2.75 V ($V_{CC} = 2.75\text{ V}$)
- Low ON-state resistance ($0.65\text{ }\Omega$ typical)
- Low charge injection
- Excellent ON-state resistance matching
- 2.3-V to 5.5-V Power supply (V_{CC})
- Latch-Up performance exceeds 100 mA Per JESD 78, Class II
- ESD Performance tested per JESD 22
 - 2500-V Human-body model (A114-B, class II)
 - 1500-V Charged-device model (C101)
 - 200-V Machine model (A115-A)

2 Applications

- Cell phones
- Personal digital assistant (PDAs)
- Portable instrumentation
- Audio routing
- Medical imaging

3 Description

The TS5A22362 is a bidirectional, 2-channel single-pole double-throw (SPDT) analog switch designed to operate from 2.3 V to 5.5 V. The device features negative signal swing capability that allows signals below ground to pass through the switch without distortion. The break-before-make feature prevents signal distortion during the transferring of a signal from one path to another. Low ON-state resistance, excellent channel-to-channel ON-state resistance matching, and minimal total harmonic distortion (THD) performance are ideal for audio applications. The 3.00 mm × 3.00 mm DRC package is also available as a nonmagnetic package for medical imaging application.

Device Information⁽¹⁾

PART NUMBER	PACKAGE	BODY SIZE (NOM)
TS5A22362	VSON (10)	3.00 mm × 3.00 mm
	DSBGA (10)	1.86 mm × 1.36 mm
	VSSOP (10)	3.00 mm × 3.00 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Typical Application Schematic

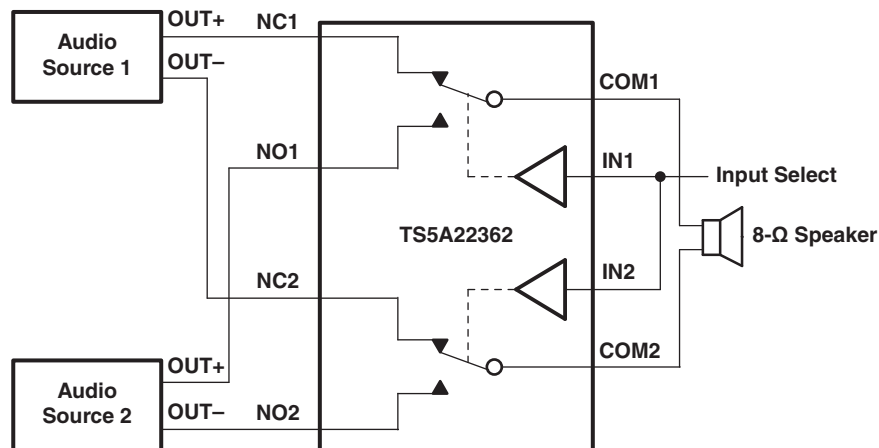


Table of Contents

1 Features	1	8.2 Functional Block Diagram	15
2 Applications	1	8.3 Feature Description	15
3 Description	1	8.4 Device Functional Modes	15
4 Revision History	2	9 Application and Implementation	16
5 Pin Configuration and Functions	3	9.1 Application Information	16
6 Specifications	4	9.2 Typical Application	16
6.1 Absolute Maximum Ratings	4	10 Power Supply Recommendations	18
6.2 ESD Ratings	4	11 Layout	18
6.3 Recommended Operating Conditions	4	11.1 Layout Guidelines	18
6.4 Thermal Information	5	11.2 Layout Example	18
6.5 Electrical Characteristics for 2.5-V Supply	5	12 Device and Documentation Support	19
6.6 Electrical Characteristics for 3.3-V Supply	6	12.1 Receiving Notification of Documentation Updates	19
6.7 Electrical Characteristics for 5-V Supply	7	12.2 Community Resources	19
6.8 Typical Characteristics	9	12.3 Trademarks	19
7 Parameter Measurement Information	11	12.4 Electrostatic Discharge Caution	19
8 Detailed Description	15	12.5 Glossary	19
8.1 Overview	15	13 Mechanical, Packaging, and Orderable Information	19

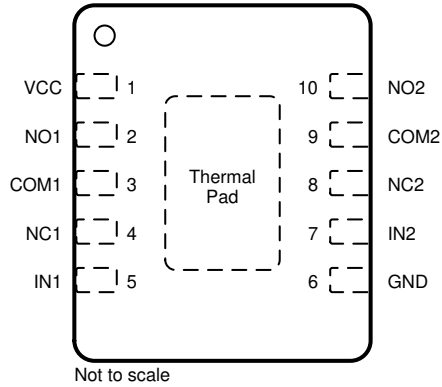
4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision D (March 2018) to Revision E	Page
• Changed the YZP Package view From: Top View To: Bottom View	3
Changes from Revision C (June 2017) to Revision D	Page
• Changed the YZP Package From: Laser Marketing View and Bump View To: Top View	3
• Changed the Q _C TYP value From: 10 pC To: 150 pC in the <i>Electrical Characteristics for 5-V Supply</i> table	8
Changes from Revision B (September 2015) to Revision C	Page
• Changed the V _{IN} MAX value From: V _{CC} To: 5.5 V in the <i>Recommended Operating Conditions</i> table	4
Changes from Revision A (August 2015) to Revision B	Page
• Changed C _L TEST CONDITION value for all THD PARAMETERS from 15 pf to 35 pf.	6
Changes from Original (June 2015) to Revision A	Page
• Changed the Functional Block Diagram.	15

5 Pin Configuration and Functions

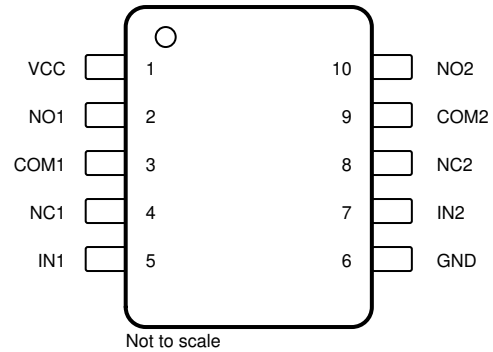
**DRC Package
10-Pin VSON
Top View**



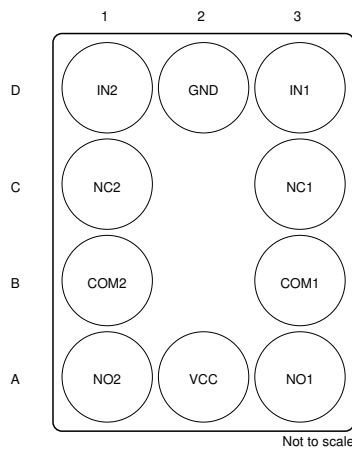
The exposed center pad, if used, must be

connected as a secondary GND or left electrically open.

**DGS Package
10-Pin VSSOP
Top View**



**YZP Package
10-Pin DSBGA
Bottom View**



Pin Functions

PIN				TYPE	DESCRIPTION
NAME	VSON	VSSOP	DSBGA		
VCC	1	1	A2	—	Power Supply
NO1	2	2	A3	I/O	Normally Open (NO) signal path, Switch 1
COM1	3	3	B3	I/O	Common signal path, Switch 1
NC1	4	4	C3	I/O	Normally Closed (NC) signal path, Switch 1
IN1	5	5	D3	I	Digital control pin , Switch 1
GND	6	6	D2	—	Ground
IN2	7	7	D1	I	Digital control pin, Switch 2
NC2	8	8	C1	I/O	Normally Closed (NC) signal path, Switch 2
COM2	9	9	B1	I/O	Common signal path, Switch 2
NO2	10	10	A1	I/O	Normally Open (NO) signal Path, Switch 2

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted) ⁽¹⁾

			MIN	MAX	UNIT
V _{CC} ⁽²⁾	Supply voltage ⁽³⁾		−0.5	6	V
V _{NC} V _{NO} V _{COM}	Analog voltage ⁽³⁾ ⁽⁴⁾ ⁽⁵⁾		V _{CC} − 6	V _{CC} + 0.5	V
I _{I/OK}	Analog port diode current	V _{NC} , V _{NO} , V _{COM} < 0 or V _{NC} , V _{NO} , V _{COM} > V _{CC}	−50	50	mA
I _{NC} I _{NO} I _{COM}	ON-state switch current	V _{NC} , V _{NO} , V _{COM} = 0 to V _{CC}	−150	150	mA
	ON-state peak switch current ⁽⁶⁾		−300	300	
I _{NC} ⁽³⁾ ⁽⁷⁾ ⁽⁸⁾ I _{NO} ⁽³⁾ ⁽⁷⁾ ⁽⁸⁾ I _{COM} ⁽³⁾ ⁽⁷⁾ ⁽⁸⁾	ON-state switch current	V _{NC} , V _{NO} , V _{COM} = 0 to V _{CC}	−350	350	mA
	ON-state peak switch current ⁽⁶⁾		−500	500	
V _I	Digital input voltage		−0.5	6.5	V
I _{IK}	Digital input clamp current ⁽³⁾ ⁽⁴⁾	V _I < 0	−50	50	mA
I _{CC} I _{GND}	Continuous current through V _{CC} or GND		−100	100	mA
T _{std}	Storage temperature		−65	150	°C

- (1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) The algebraic convention, whereby the most negative value is a minimum and the most positive value is a maximum
- (3) All voltages are with respect to ground, unless otherwise specified.
- (4) The input and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
- (5) This value is limited to 5.5 V maximum.
- (6) Pulse at 1-ms duration < 10% duty cycle.
- (7) $V_{CC} = 3.0$ V to 5.0 V, $T_A = -40^{\circ}\text{C}$ to 85°C .
- (8) For YZP package only.

6.2 ESD Ratings

		VALUE	UNIT
$V_{(ESD)}$ Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 ⁽¹⁾	±2500	V
	Charged-device model (CDM), per JEDEC specification JESD22-C101 ⁽²⁾	±1500	

- (1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
- (2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
V_{CC}	Supply voltage	2.3	5.5	V
V_{NC} V_{NO} V_{COM}	Signal path voltage	$V_{CC} - 5.5$	V_{CC}	V
V_{IN}	Digital control	GND	5.5	V

6.4 Thermal Information

THERMAL METRIC ⁽¹⁾		TS5A22362			UNIT
		DGS (VSSOP)	DRC (VSON)	YZP (DSBGA)	
		10 PINS	10 PINS	10 PINS	
R _{θJA}	Junction-to-ambient thermal resistance	163.3	44.3	90.9	°C/W
R _{θJC(top)}	Junction-to-case (top) thermal resistance	56.4	70.1	0.3	°C/W
R _{θJB}	Junction-to-board thermal resistance	83.1	19.3	8.3	°C/W
ψ _{JT}	Junction-to-top characterization parameter	6.8	2.0	3.2	°C/W
ψ _{JB}	Junction-to-board characterization parameter	81.8	19.4	8.3	°C/W

(1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics](#) application report.

6.5 Electrical Characteristics for 2.5-V Supply

V_{CC} = 2.3 V to 2.7 V, T_A = –40°C to 85°C (unless otherwise noted) ⁽¹⁾

PARAMETER	TEST CONDITIONS	T _A	V _{CC}	MIN	TYP	MAX	UNIT
Analog Switch							
V _{COM} , V _{NO} , V _{NC}	Analog signal range			V _{CC} – 5.5		V _{CC}	V
R _{on}	ON-state resistance	V _{NC} or V _{NO} = V _{CC} , 1.5 V, V _{CC} – 5.5 V I _{COM} = –100 mA, COM to NO or NC, see Figure 13	25°C Full	2.7 V	0.65 1.3	0.94	Ω
ΔR _{on}	ON-state resistance match between channels	V _{NC} or V _{NO} = 1.5 V, I _{COM} = –100 mA, COM to NO or NC, see Figure 13	25°C Full	2.7 V	0.023 0.15	0.11	Ω
R _{on(flat)}	ON-state resistance flatness	V _{NC} or V _{NO} = V _{CC} , 1.5 V, V _{CC} – 5.5 V I _{COM} = –100 mA, COM to NO or NC, see Figure 13	25°C Full	2.7 V	0.18 0.5	0.46	Ω
I _{NC(OFF)} , I _{NO(OFF)}	NC, NO OFF leakage current	V _{NC} = 2.25 V, V _{CC} – 5.5 V V _{COM} = V _{CC} – 5.5 V, 2.25 V V _{NO} = Open COM to NO or V _{NO} = 2.25 V, V _{CC} – 5.5 V, V _{COM} = V _{CC} – 5.5 V, 2.25 V V _{NC} = Open COM to NC	25°C Full	2.7 V	–50 –375	50 375	nA
I _{COM(ON)}	COM ON leakage current	V _{NC} and V _{NO} = Floating, V _{COM} = V _{CC} , V _{CC} – 5.5 V	25°C Full	2.7 V	–50 –375	50 375	nA
Digital Control Inputs (IN) ⁽²⁾							
V _{IH}	Input logic high		Full		1.4	5.5	V
V _{IL}	Input logic low					0.6	
I _{IH} , I _{IL}	Input leakage current	V _{IN} = V _{CC} or 0	25°C Full	2.7 V	–250 –250	250 250	nA
Dynamic							
t _{ON}	Turnon time	V _{COM} = V _{CC} , R _L = 300 Ω, C _L = 35 pF, see Figure 17	25°C Full	2.5 V 2.3 V to 2.7 V	44 120	80	ns
t _{OFF}	Turnoff time	V _{COM} = V _{CC} , R _L = 300 Ω, C _L = 35 pF, see Figure 17	25°C Full	2.5 V 2.3 V to 2.7 V	22 70	70	ns
t _{BBM}	Break-before-make time	See Figure 18	25°C	2.5 V	1	7	ns
Q _C	Charge injection	V _{GEN} = 0, R _{GEN} = 0, C _L = 1 nF, see Figure 22	25°C	2.5 V	150		pC
C _{NC(OFF)} , C _{NO(OFF)}	NC, NO OFF capacitance	V _{NC} or V _{NO} = V _{CC} or GND, See Figure 16	25°C	2.5 V	70		pF

(1) The algebraic convention, whereby the most negative value is a minimum and the most positive value is a maximum

(2) All unused digital inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, [Implications of Slow or Floating CMOS Inputs](#), [SCBA004](#).

Electrical Characteristics for 2.5-V Supply (continued)

 $V_{CC} = 2.3 \text{ V to } 2.7 \text{ V}$, $T_A = -40^\circ\text{C to } 85^\circ\text{C}$ (unless otherwise noted) ⁽¹⁾

PARAMETER	TEST CONDITIONS	T_A	V_{CC}	MIN	TYP	MAX	UNIT
$C_{COM(ON)}$	NC, NO, COM ON capacitance $V_{COM} = V_{CC}$ or GND, Switch ON, $f = 10 \text{ MHz}$ See Figure 16	25°C	2.5 V		370		pF
C_i	Digital input capacitance $V_i = V_{CC}$ or GND See Figure 16	25°C	2.5 V		2.6		pF
BW	Bandwidth $R_L = 50 \Omega$, -3 dB See Figure 18	25°C	2.5 V		17		MHz
O_{ISO}	OFF isolation $R_L = 50 \Omega$ $f = 100 \text{ kHz}$, see Figure 20	25°C	2.5 V		-66		dB
X_{TALK}	Crosstalk $R_L = 50 \Omega$ $f = 100 \text{ kHz}$, see Figure 21	25°C	2.5 V		-75		dB
THD	Total harmonic distortion $R_L = 600 \Omega$, $C_L = 35 \text{ pF}$ $f = 20 \text{ Hz to } 20 \text{ kHz}$, see Figure 23	25°C	2.5 V		0.01%		
Supply							
I_{CC}	Positive supply current V_{COM} and $V_{IN} = V_{CC}$ or GND, V_{NC} and $V_{NO} = \text{Floating}$	25°C	2.7 V		0.2	1.1	μA
		Full				1.3	
I_{CC}	Positive supply current $V_{COM} = V_{CC} - 5.5 \text{ V}$, $V_{IN} = V_{CC}$ or GND, V_{NC} and $V_{NO} = \text{Floating}$	Full	2.7 V			3.3	μA

6.6 Electrical Characteristics for 3.3-V Supply

 $V_{CC} = 3 \text{ V to } 3.6 \text{ V}$, $T_A = -40^\circ\text{C to } 85^\circ\text{C}$ (unless otherwise noted) ⁽¹⁾

PARAMETER		TEST CONDITIONS		T _A	V _{CC}	MIN	TYP	MAX	UNIT
ANALOG SWITCH									
V _{COM} , V _{NO} , V _{NC}	Analog signal range					V _{CC} – 5.5		V _{CC}	V
R _{on}	ON-state resistance	V _{NC} or V _{NO} ≤ V _{CC} , 1.5 V, V _{CC} – 5.5 V, I _{COM} = –100 mA	COM to NO or NC, see Figure 13	25°C	3 V	0.61		0.87	Ω
				Full		0.97			
ΔR _{on}	ON-state resistance match between channels	V _{NC} or V _{NO} = 1.5 V, I _{COM} = –100 mA,	COM to NO or NC, see Figure 13	25°C	3 V	0.024		0.13	Ω
				Full		0.13			
R _{on(flat)}	ON-state resistance flatness	V _{NC} or V _{NO} ≤ V _{CC} , 1.5 V, V _{CC} – 5.5 V, I _{COM} = –100 mA	COM to NO or NC, see Figure 13	25°C	3 V	0.12		0.46	Ω
				Full		0.5			
I _{NC(OFF)} , I _{NO(OFF)}	NC, NO OFF leakage current	V _{NC} = 3 V, V _{CC} – 5.5 V V _{COM} = V _{CC} – 5.5 V, 3 V V _{NO} = Open COM to NO or V _{NO} = 3 V, V _{CC} – 5.5 V, V _{COM} = V _{CC} – 5.5 V, 3 V V _{NC} = Open COM to NC	See Figure 14	25°C	3.6 V	–50		50	nA
				Full		–375		375	
I _{COM(ON)}	COM ON leakage current	V _{NC} and V _{NO} = Floating, V _{COM} = V _{CC} , V _{CC} – 5.5 V	COM to NO or NC, see Figure 15	25°C	3.6 V	–50		50	nA
				Full		–375		375	
DIGITAL CONTROL INPUTS (IN) ⁽²⁾									
V _{IH}	Input logic high			Full		1.4		5.5	V
V _{IL}	Input logic low					0.8			
I _{IH} , I _{IL}	Input leakage current	V _{IN} = V _{CC} or 0		25°C	3.6 V	–250		250	nA
				Full		–250		250	

(1) The algebraic convention, whereby the most negative value is a minimum and the most positive value is a maximum

(2) All unused digital inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number [SCBA004](#).

Electrical Characteristics for 3.3-V Supply (continued)

 $V_{CC} = 3\text{ V to }3.6\text{ V}$, $T_A = -40^\circ\text{C to }85^\circ\text{C}$ (unless otherwise noted) ⁽¹⁾

PARAMETER	TEST CONDITIONS	T_A	V_{CC}	MIN	TYP	MAX	UNIT
DYNAMIC							
t_{ON} Turnon time	$V_{COM} = V_{CC}$, $R_L = 300\ \Omega$ $C_L = 35\text{ pF}$, see Figure 17	25°C	3.3 V		34	80	ns
		Full	3 V to 3.6 V			120	
t_{OFF} Turnoff time	$V_{COM} = V_{CC}$, $R_L = 300\ \Omega$ $C_L = 35\text{ pF}$, see Figure 17	25°C	3.3 V		19	70	ns
		Full	3 V to 3.6 V			70	
t_{BBM} Break-before-make time	See Figure 18	25°C	3.3 V	1	7		ns
Q_C Charge injection	$V_{GEN} = 0$, $R_{GEN} = 0$ $C_L = 1\text{ nF}$, see Figure 22	25°C	3.3 V		150		pC
$C_{NC(OFF)}$, $C_{NO(OFF)}$ NC, NO OFF capacitance	V_{NC} or $V_{NO} = V_{CC}$ or $V_{CC} - 5.5\text{ V}$ See Figure 16	25°C	3.3 V		70		pF
$C_{COM(ON)}$ NC, NO, COM ON capacitance	$V_{COM} = V_{CC}$ or GND, $f = 10\text{ MHz}$ See Figure 16	25°C	3.3 V		370		pF
C_I Digital input capacitance	$V_I = V_{CC}$ or GND See Figure 16	25°C	3.3 V		2.6		pF
BW Bandwidth	$R_L = 50\ \Omega$, -3 dB Switch ON, see Figure 18	25°C	3.3 V		17.5		MHz
O_{ISO} OFF isolation	$R_L = 50\ \Omega$ $f = 100\text{ kHz}$, see Figure 20	25°C	3.3 V		-68		dB
X_{TALK} Crosstalk	$R_L = 50\ \Omega$ $f = 100\text{ kHz}$, see Figure 21	25°C	3.3 V		-76		dB
THD Total harmonic distortion	$R_L = 600\ \Omega$, $C_L = 35\text{ pF}$ $f = 20\text{ Hz to }20\text{ kHz}$, see Figure 23	25°C	3.3 V		0.008%		
SUPPLY							
I_{CC} Positive supply current	V_{COM} and $V_{IN} = V_{CC}$ or GND, V_{NC} and $V_{NO} = \text{Floating}$	25°C	3.6 V		0.1	1.2	μA
		Full				1.3	
	$V_{COM} = V_{CC} - 5.5\text{ V}$, $V_{IN} = V_{CC}$ or GND, V_{NC} and $V_{NO} = \text{Floating}$	Full	3.6 V			3.4	μA

6.7 Electrical Characteristics for 5-V Supply

 $V_{CC} = 4.5\text{ V to }5.5\text{ V}$, $T_A = -40^\circ\text{C to }85^\circ\text{C}$ (unless otherwise noted) ⁽¹⁾

PARAMETER	TEST CONDITIONS	T_A	V_{CC}	MIN	TYP	MAX	UNIT
ANALOG SWITCH							
V_{COM} , V_{NO} , V_{NC} Analog signal range				$V_{CC} - 5.5$		V_{CC}	V
R_{on} ON-state resistance	V_{NC} or $V_{NO} = V_{CC}$, 1.6 V, $V_{CC} = -5.5\text{ V}$, $I_{COM} = -100\text{ mA}$ COM to NO or NC, see Figure 13	25°C	4.5 V		0.52	0.74	Ω
		Full				0.83	
ΔR_{on} ON-state resistance match between channels	V_{NC} or $V_{NO} = 1.6\text{ V}$, $I_{COM} = -100\text{ mA}$ COM to NO or NC, see Figure 13	25°C	4.5 V		0.04	0.23	Ω
		Full				0.30	
$R_{on(Flat)}$ ON-state resistance flatness	V_{NC} or $V_{NO} = V_{CC}$, 1.6 V, $V_{CC} = -5.5\text{ V}$, $I_{COM} = -100\text{ mA}$ COM to NO or NC, see Figure 13	25°C	4.5 V		0.076	0.46	Ω
		Full				0.5	
$I_{NC(OFF)}$, $I_{NO(OFF)}$ NC, NO OFF leakage current	$V_{NC} = 4.5\text{ V}$, $V_{CC} - 5.5\text{ V}$, $V_{COM} = V_{CC} - 5.5\text{ V}$, 4.5 V, $V_{NO} = \text{Open}$, COM to NO or $V_{NO} = 4.5\text{ V}$, $V_{CC} - 5.5\text{ V}$, $V_{COM} = V_{CC} - 5.5\text{ V}$, 4.5 V, $V_{NC} = \text{Open}$, COM to NC See Figure 14	25°C	5.5 V	-50		50	nA
		Full		-375		375	
$I_{COM(ON)}$ COM ON leakage current	V_{NC} and $V_{NO} = \text{Floating}$, $V_{COM} = V_{CC}$, $V_{CC} - 5.5\text{ V}$ See Figure 15	25°C	5.5 V	-50		50	nA
		Full		-375		375	

(1) The algebraic convention, whereby the most negative value is a minimum and the most positive value is a maximum

Electrical Characteristics for 5-V Supply (continued)

 $V_{CC} = 4.5 \text{ V to } 5.5 \text{ V}$, $T_A = -40^\circ\text{C to } 85^\circ\text{C}$ (unless otherwise noted) ⁽¹⁾

PARAMETER		TEST CONDITIONS		T _A	V _{CC}	MIN	TYP	MAX	UNIT
DIGITAL CONTROL INPUTS (IN) ⁽²⁾									
V _{IH}	Input logic high			Full		2.4		5.5	V
V _{IL}	Input logic low							0.8	
I _{IH} , I _{IL}	Input leakage current	V _{IN} = V _{CC} or 0	25°C	5.5 V		−250		250	nA
			Full			−250		250	
DYNAMIC									
t _{ON}	Turnon time	V _{COM} = V _{CC} , R _L = 300 Ω	C _L = 35 pF, see Figure 17	25°C	5 V	27		80	ns
				Full	4.5 V to 5.5 V			80	
t _{OFF}	Turnoff time	V _{COM} = V _{CC} , R _L = 300 Ω	C _L = 35 pF, see Figure 17	25°C	5 V	13		70	ns
				Full	4.5 V to 5.5 V			70	
t _{BBM}	Break-before-make time	V _{NC} = V _{NO} = V _{CC} /2 R _L = 300 Ω	C _L = 35 pF, see Figure 18	25°C	5 V	1	3.5		ns
Q _C	Charge injection	V _{GEN} = 0, R _{GEN} = 0	C _L = 1 nF, see Figure 22	25°C	5 V		150		pC
C _{NC(OFF)} , C _{NO(OFF)}	NC, NO OFF capacitance	V _{NC} or V _{NO} = V _{CC} or V _{CC} − 5.5 V	See Figure 16	25°C	5 V		70		pF
C _{COM(ON)}	NC, NO, COM ON capacitance	V _{COM} = V _{CC} or GND,	See Figure 16	25°C	5 V		370		pF
C _I	Digital input capacitance	V _I = V _{CC} or GND	See Figure 16	25°C	5 V		2.6		pF
BW	Bandwidth	R _L = 50 Ω	See Figure 18	25°C	5 V		18.3		MHz
O _{ISO}	OFF isolation	R _L = 50 Ω	f = 100 kHz, see Figure 20	25°C	5 V		−70		dB
X _{TALK}	Crosstalk	R _L = 50 Ω	f = 100 kHz, see Figure 21	25°C	5 V		−78		dB
THD	Total harmonic distortion	R _L = 600 Ω, C _L = 35 pF	f = 20 Hz to 20 kHz, see Figure 23	25°C	5 V		0.009%		
SUPPLY									
I _{CC}	Positive supply current	V _{COM} and V _{IN} = V _{CC} or GND, V _{NC} and V _{NO} = Floating	25°C	5.5 V		0.2		1.3	μA
			Full				3.5		
		V _{COM} = V _{CC} − 5.5 V, V _{IN} = V _{CC} or GND, V _{NC} and V _{NO} = Floating	Full				5		

(2) All unused digital inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, [SCBA004](#).

6.8 Typical Characteristics

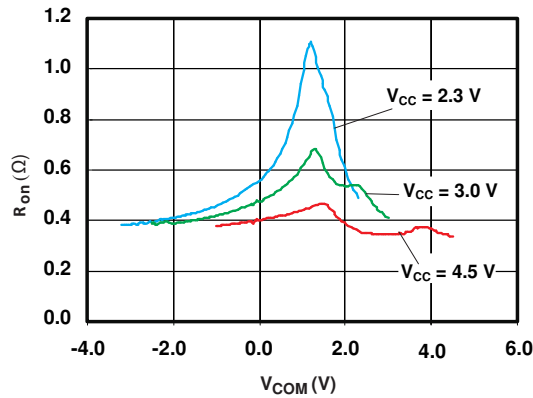


Figure 1. R_{on} vs V_{COM}

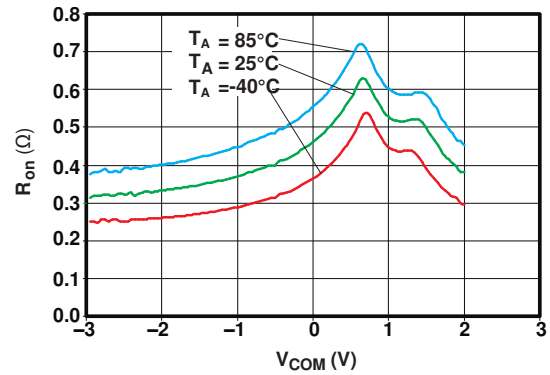


Figure 2. R_{on} vs V_{COM} ($V_{CC} = 2.7$ V)

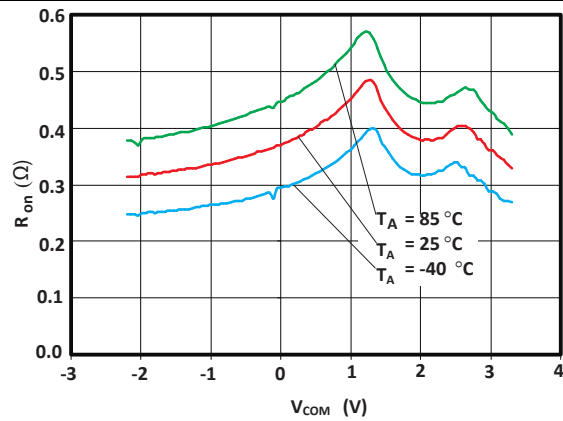


Figure 3. R_{on} vs V_{COM} ($V_{CC} = 3.3$ V)

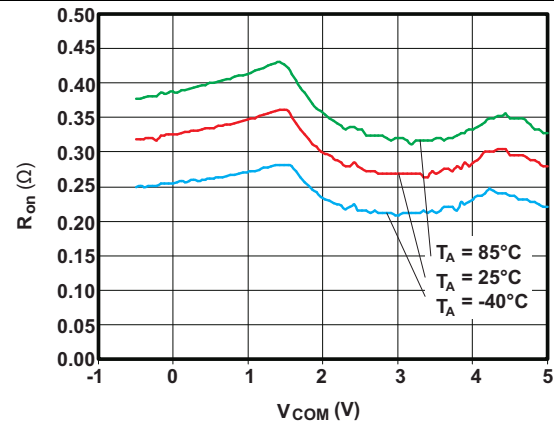


Figure 4. R_{on} vs V_{COM} ($V_{CC} = 5$ V)

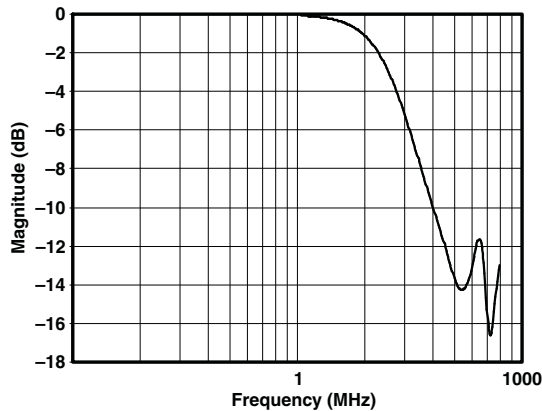


Figure 5. Insertion Loss

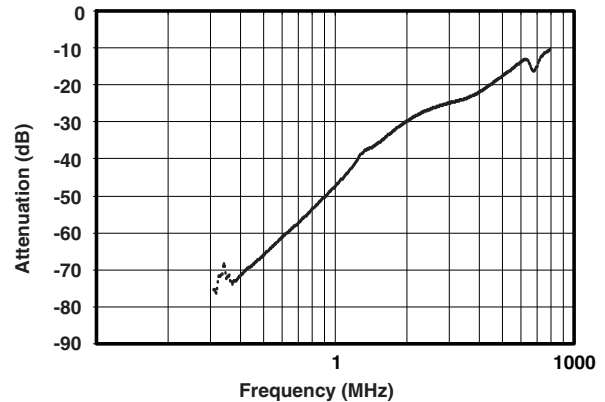


Figure 6. Off Isolation vs Frequency

Typical Characteristics (continued)

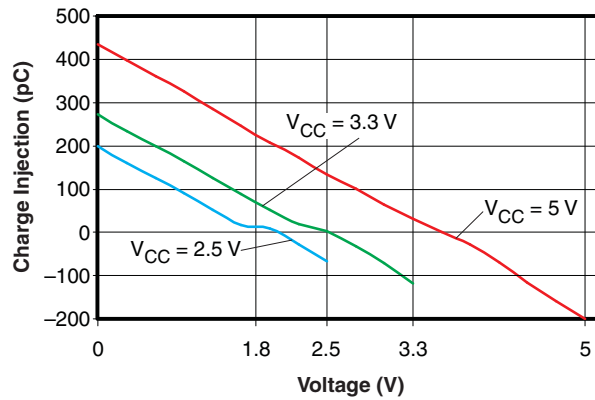


Figure 7. Charge Injection (Q_c) vs V_{COM}

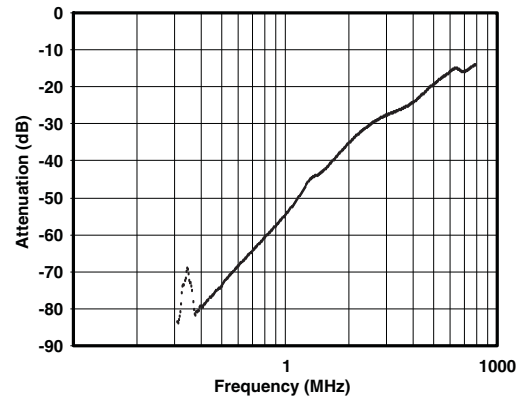


Figure 8. Crosstalk ($V_{CC} = 3.3\text{ V}$)

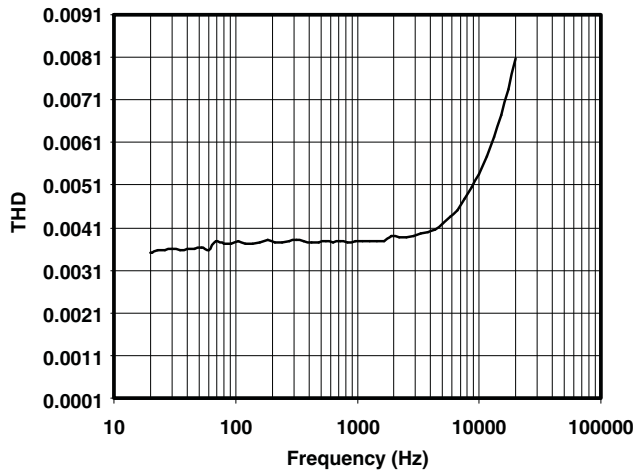


Figure 9. Total Harmonic Distortion vs Frequency

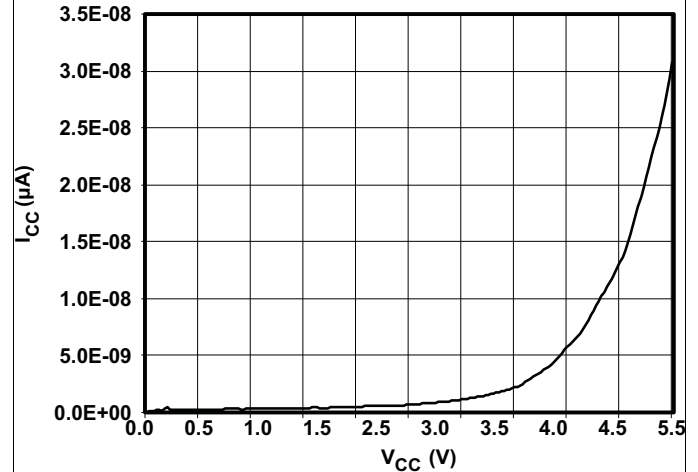


Figure 10. Power-Supply Current vs V_{CC}

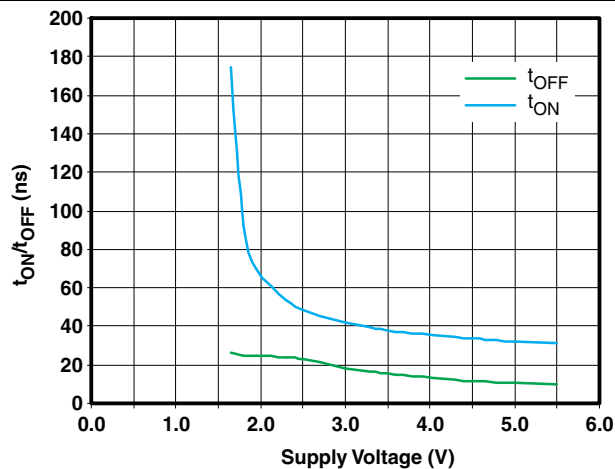


Figure 11. t_{ON} And t_{OFF} vs Supply Voltage

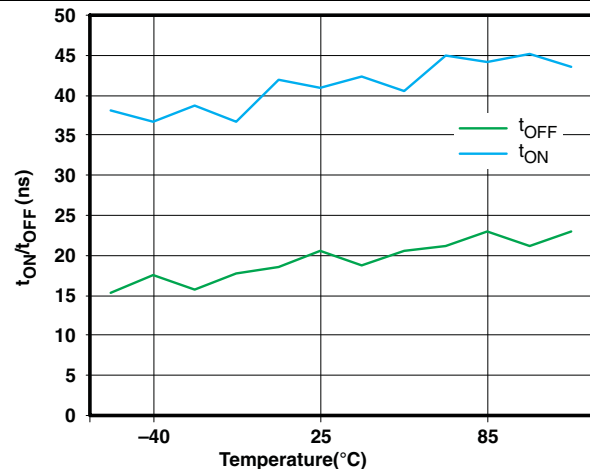


Figure 12. t_{ON} And t_{OFF} vs Temperature (2.5-V Supply)

7 Parameter Measurement Information

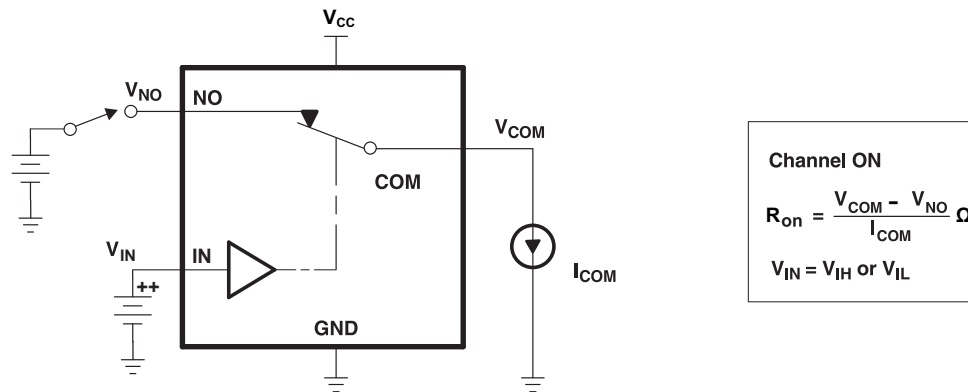


Figure 13. ON-state resistance (R_{on})

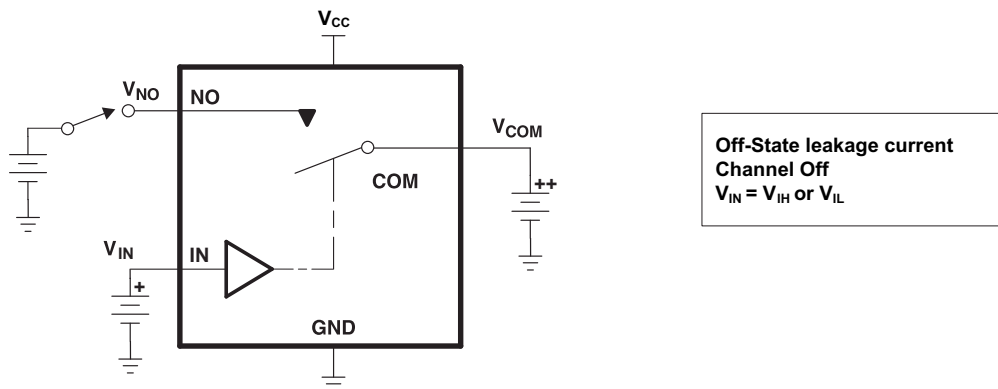


Figure 14. OFF-state leakage current ($I_{COM(OFF)}$, $I_{NO(OFF)}$)

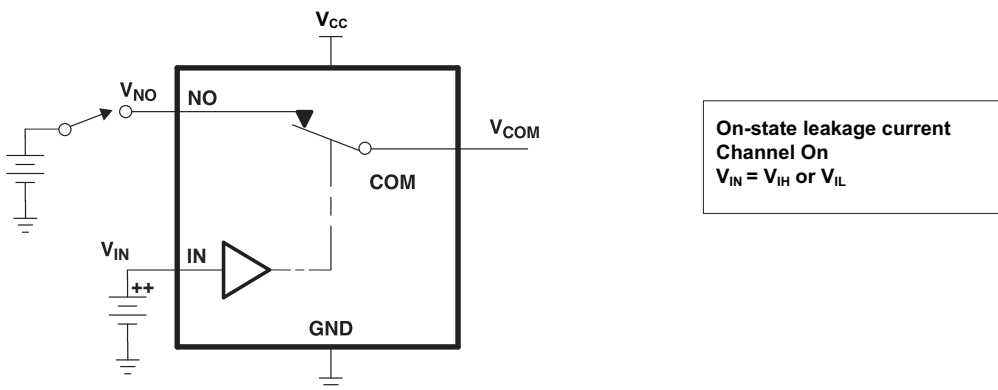


**Figure 15. ON-state leakage current
($I_{COM(ON)}$, $I_{NO(ON)}$)**

Parameter Measurement Information (continued)

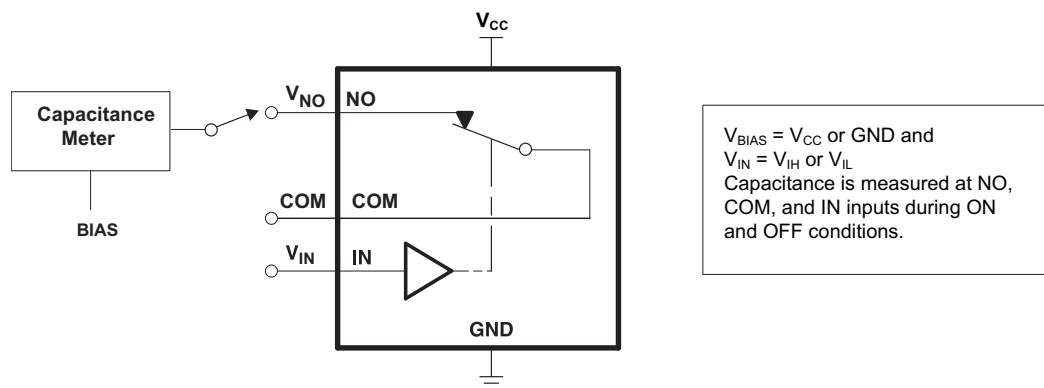
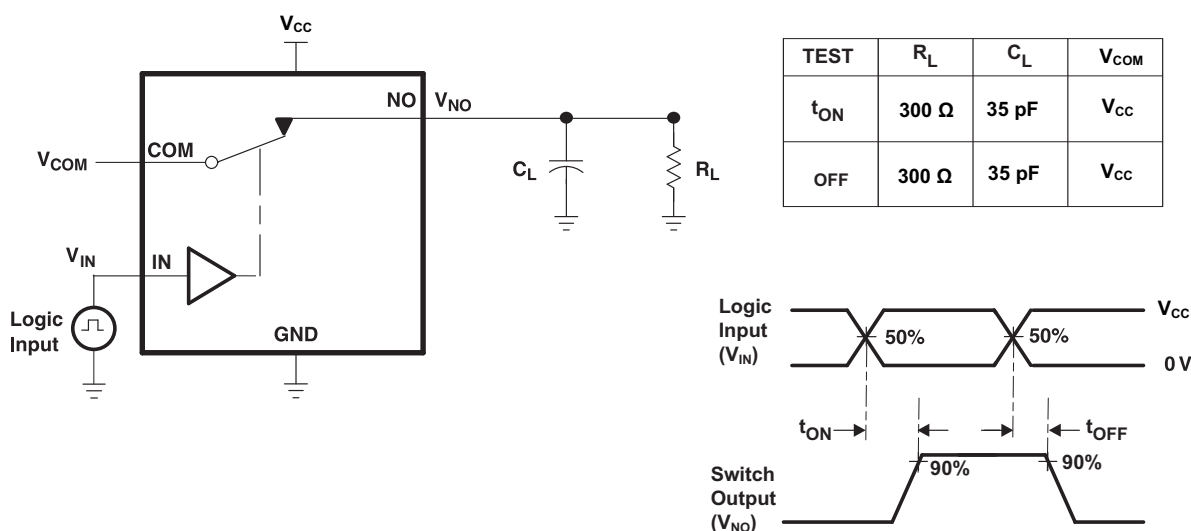


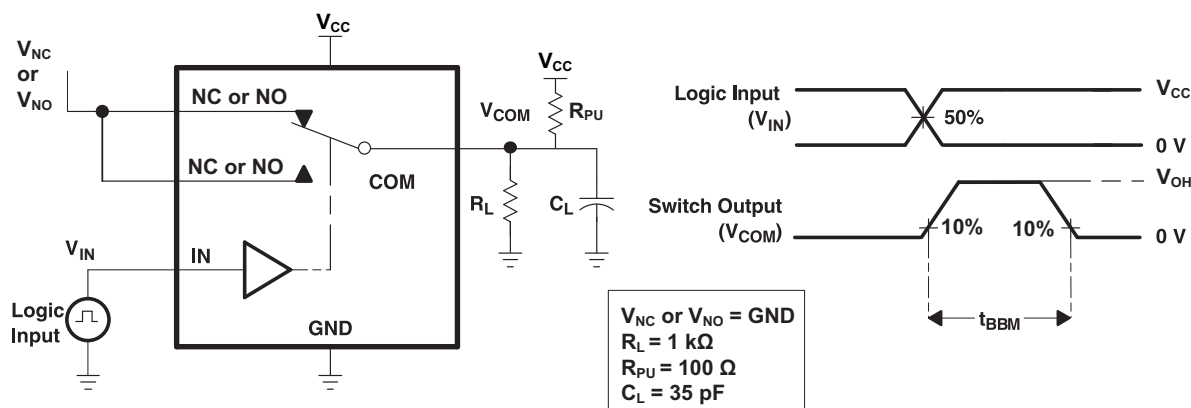
Figure 16. Capacitance
(C_I , $C_{COM(OFF)}$, $C_{COM(ON)}$, $C_{NO(OFF)}$, $C_{NO(ON)}$)



- A. All input pulses are supplied by generators having the following characteristics: PRR $\leq$ 10 MHz, $Z_O = 50 \Omega$, $t_r < 5$ ns, $t_f < 5$ ns.
- B. C_L includes probe and jig capacitance.

Figure 17. Turnon (t_{ON}) and Turnoff time (t_{OFF})

Parameter Measurement Information (continued)



- A. C_L includes probe and jig capacitance.
- B. All input pulses are supplied by generators having the following characteristics: $PRR \leq 10\text{ MHz}$, $Z_O = 50\text{ }\Omega$, $t_r < 5\text{ ns}$, $t_f < 5\text{ ns}$.

Figure 18. Break-Before-Make Time (t_{BBM})

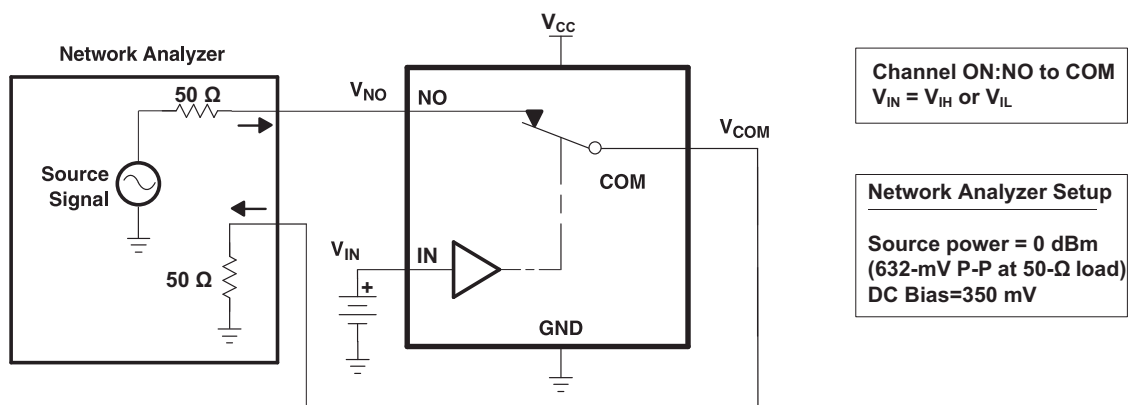


Figure 19. Bandwidth (BW)

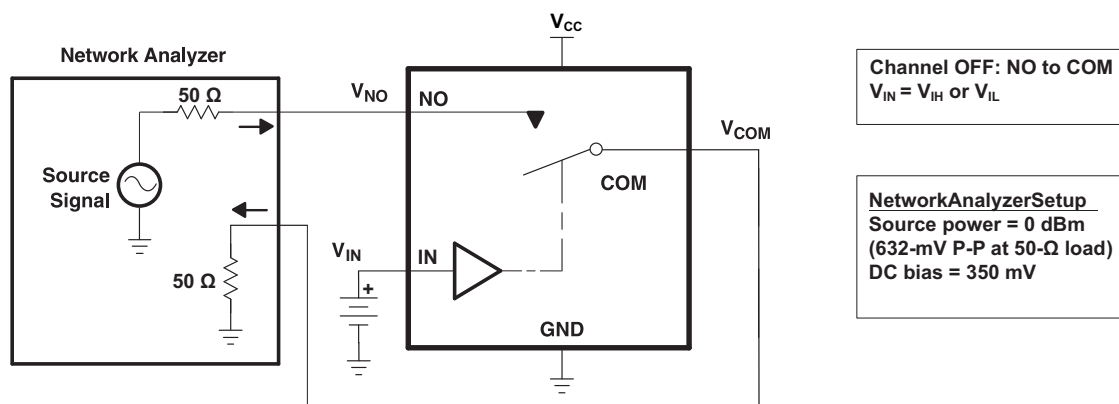


Figure 20. OFF isolation (O_{Iso})

Parameter Measurement Information (continued)

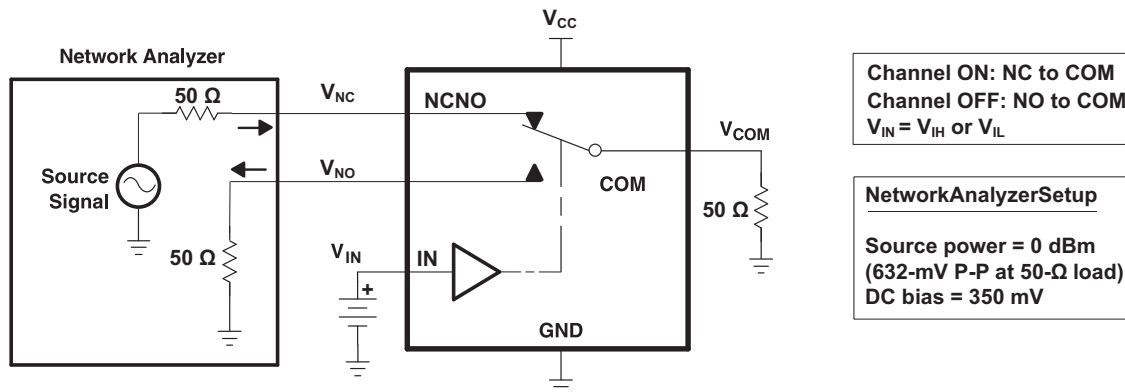
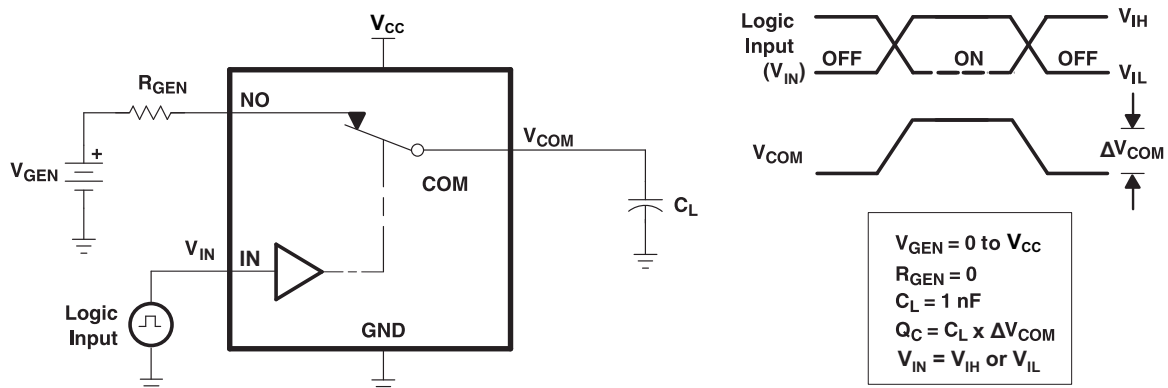


Figure 21. Crosstalk (X_{TALK})



- All input pulses are supplied by generators having the following characteristics: $PRR \leq 10$ MHz, $Z_O = 50$ Ω, $t_r < 5$ ns, $t_f < 5$ ns.
- C_L includes probe and jig capacitance.

Figure 22. Charge injection (Q_C)

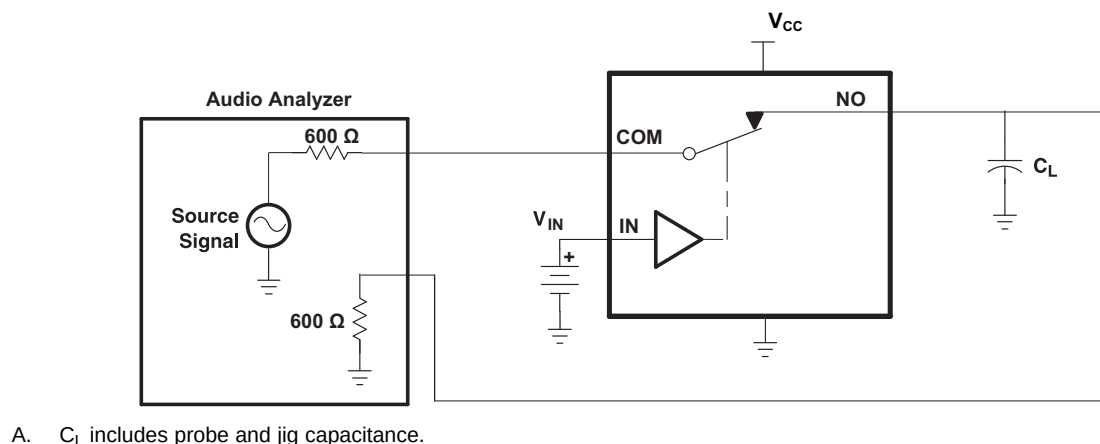
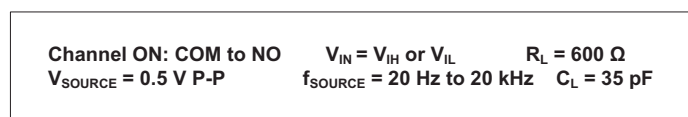


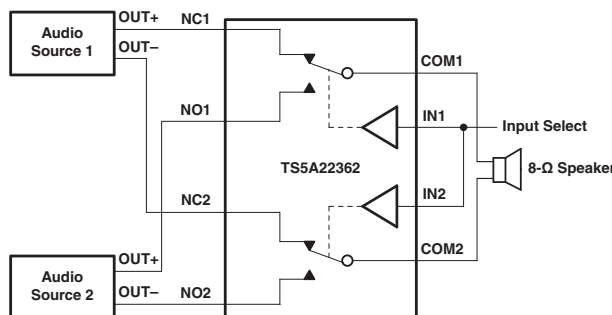
Figure 23. Total Harmonic Distortion (THD)

8 Detailed Description

8.1 Overview

The TS5A22362 is a bidirectional, 2-channel single-pole double-throw (SPDT) analog switches designed to operate from 2.3 V to 5.5 V. The devices feature negative signal capability that allows signals below ground to pass through the switch without distortion. The break-before-make feature prevents signal distortion during the transferring of a signal from one path to another. Low ON-state resistance, excellent channel-to-channel ON-state resistance matching, and minimal total harmonic distortion (THD) performance are ideal for audio applications.

8.2 Functional Block Diagram



8.3 Feature Description

8.3.1 Negative Signaling Capacity

The TS5A22362 dual SPDT switches feature negative signal capability that allows signals below ground to pass through without distortion. These analog switches operate from a single +2.3-V to +5.5-V supply. The input and output signal swing of the device is dependant of the supply voltage V_{CC} : the devices pass signals as high as V_{CC} and as low as $V_{CC} - 5.5$ V, including signals below ground with minimal distortion.

Table 1 shows the input/output signal swing the user can get with different supply voltages.

Table 1. Input/Output signal swing

SUPPLY VOLTAGE, V_{CC}	MINIMUM (V_{NC} , V_{NO} , V_{COM}) = $V_{CC} - 5.5$	MAXIMUM (V_{NC} , V_{NO} , V_{COM}) = V_{CC}
5.5 V	0 V	5.5 V
4.5 V	–1.9 V	4.5 V
3.6 V	–2.5 V	3.6 V
3.0 V	–2.5 V	3.0 V
2.7 V	–2.8 V	2.7 V
2.3 V	–3.2 V	2.3 V

8.4 Device Functional Modes

The function table for TS5A22362 is shown in Table 2

Table 2. Function Table

IN	NC TO COM, COM TO NC	NO TO COM, COM TO NO
L	ON	OFF
H	OFF	ON

9 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

Ensure that the device is powered up with a supply voltage on VCC before a voltage can be applied to the signal paths NC and NO.

Tie the digitally controlled inputs select pins IN1 and IN2 to VCC or GND to avoid unwanted switch states that could result if the logic control pins are left floating.

All unused digital inputs of the device must be held at VCC or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, [SCBA004](#).

9.2 Typical Application

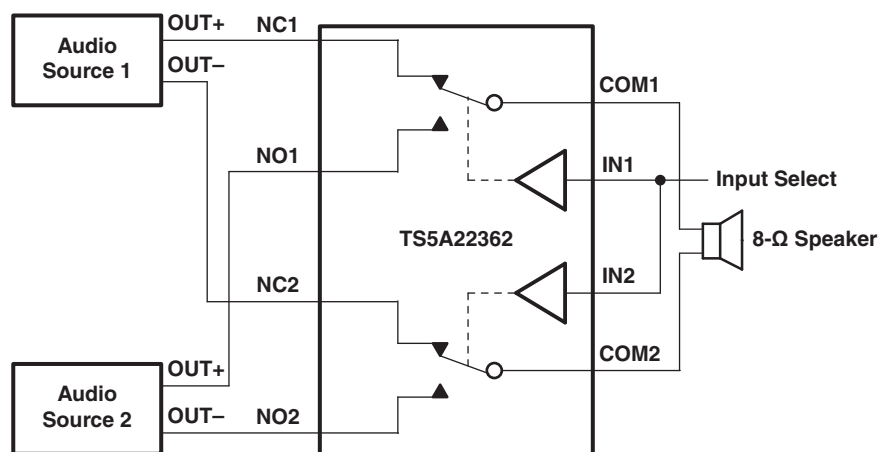


Figure 24. Typical Application

9.2.1 Design Requirements

Tie the digitally controlled inputs select pins IN1 and IN2 to VCC or GND to avoid unwanted switch states that could result if the logic control pins are left floating.

9.2.2 Detailed Design Procedure

Select the appropriate supply voltage to cover the entire voltage swing of the signal passing through the switch because the TS5A22362 operates from a single +2.3-V to +5.5-V supply and the input/output signal swing of the device is dependant of the supply voltage VCC. The device will pass signals as high as VCC and as low as VCC – 5.5 V. Use table 2 as a guide for selecting supply voltage based on the signal passing through the switch.

Ensure that the device is powered up with a supply voltage on VCC before a voltage can be applied to the signal paths NC and NO.

Typical Application (continued)

9.2.3 Application Curve

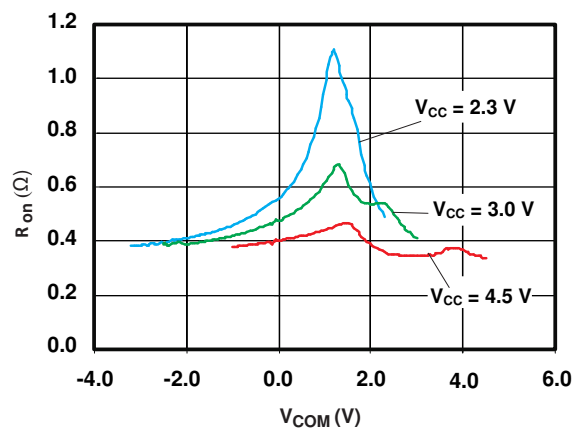


Figure 25. R_{on} vs V_{COM}

10 Power Supply Recommendations

The TS5A22362 operates from a single 2.3-V to 5.5-V supply. The device must be powered up with a supply voltage on VCC before a voltage can be applied to the signal paths NC and NO. It is recommended to include a 100- μ s delay after VCC is at voltage before applying a signal on NC and NO paths

It is also good practice to place a 0.1- μ F bypass capacitor on the supply pin VCC to GND to smooth out lower frequency noise to provide better load regulation across the frequency spectrum.

11 Layout

11.1 Layout Guidelines

TI recommends placing a bypass capacitor as close to the supply pin VCC as possible to help smooth out lower frequency noise to provide better load regulation across the frequency spectrum.

Minimize trace lengths and vias on the signal paths in order to preserve signal integrity.

11.2 Layout Example

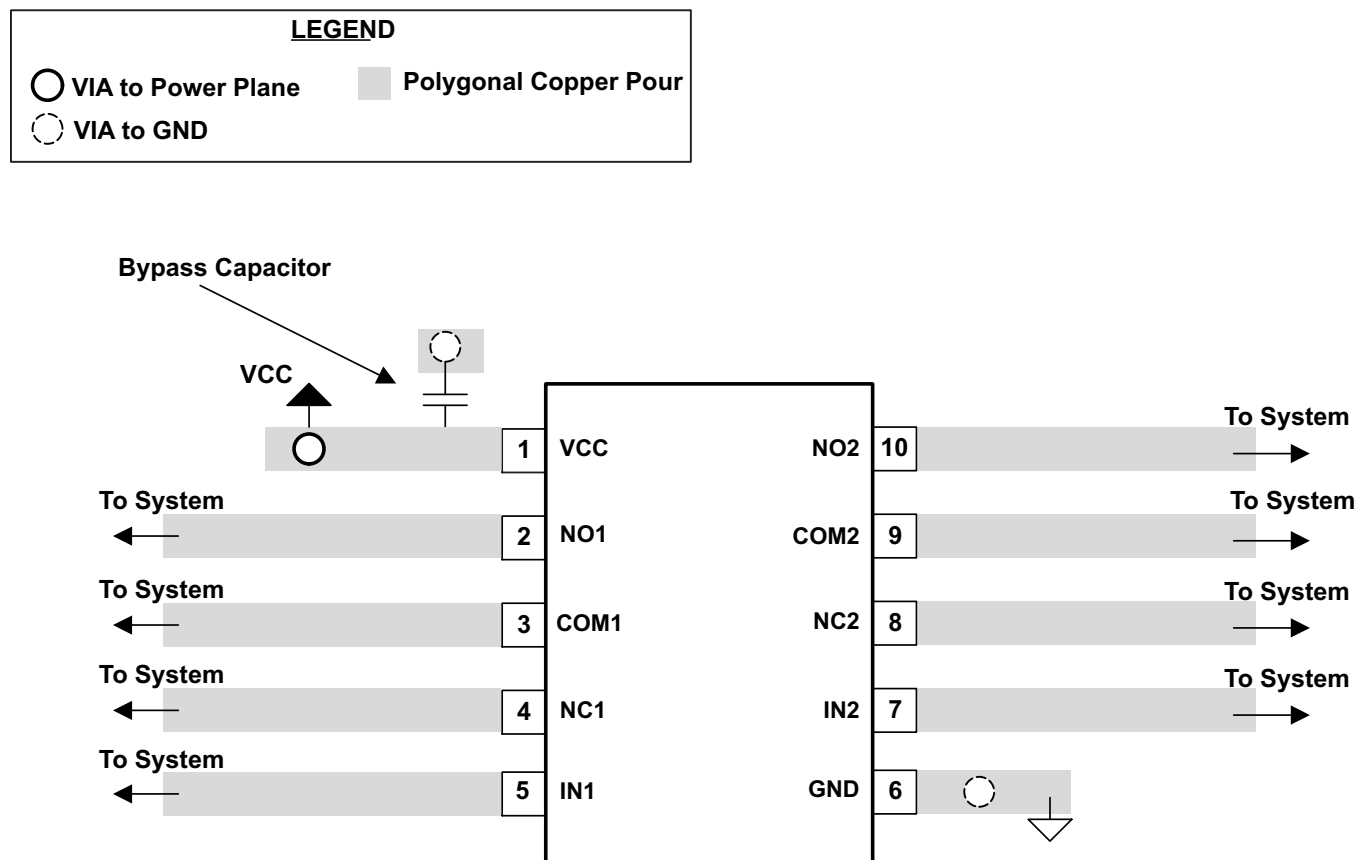


Figure 26. Layout example of TS5A22362

12 Device and Documentation Support

12.1 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

12.2 Community Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's [Terms of Use](#).

12.3 Trademarks

E2E is a trademark of Texas Instruments.

All other trademarks are the property of their respective owners.

12.4 Electrostatic Discharge Caution



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

12.5 Glossary

[SLYZ022](#) — TI Glossary.

This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package Pins	Package qty Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TS5A22362DGSR	Active	Production	VSSOP (DGS) 10	2500 LARGE T&R	Yes	NIPDAU SN	Level-1-260C-UNLIM	-40 to 85	39R
TS5A22362DGSR.B	Active	Production	VSSOP (DGS) 10	2500 LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 85	39R
TS5A22362DRCR	Active	Production	VSON (DRC) 10	3000 LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	ZVG
TS5A22362DRCR.B	Active	Production	VSON (DRC) 10	3000 LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	ZVG
TS5A22362DRCRG4	Active	Production	VSON (DRC) 10	3000 LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	ZVG
TS5A22362DRCRG4.B	Active	Production	VSON (DRC) 10	3000 LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	ZVG
TS5A22362YZPR	Active	Production	DSBGA (YZP) 10	3000 LARGE T&R	Yes	SNAGCU	Level-1-260C-UNLIM	-40 to 85	(39, 392)
TS5A22362YZPR.B	Active	Production	DSBGA (YZP) 10	3000 LARGE T&R	Yes	SNAGCU	Level-1-260C-UNLIM	-40 to 85	(39, 392)

⁽¹⁾ **Status:** For more details on status, see our [product life cycle](#).

⁽²⁾ **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

⁽³⁾ **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

⁽⁴⁾ **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

⁽⁵⁾ **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

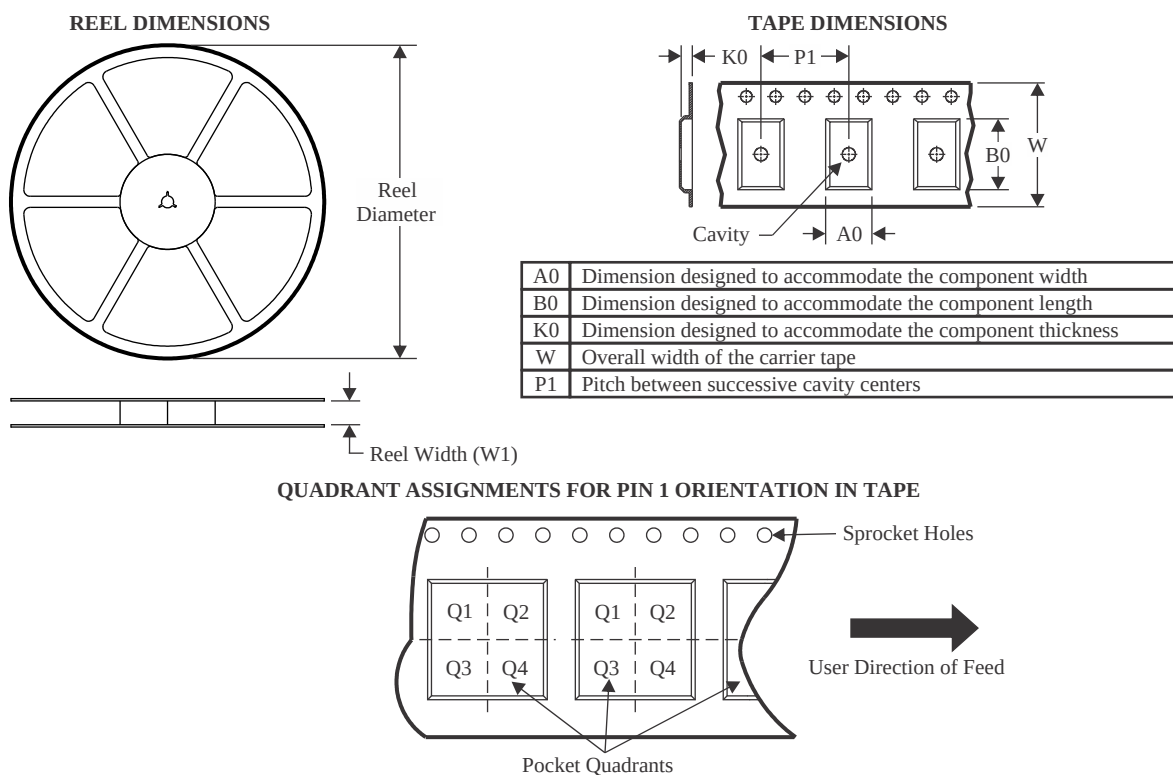
⁽⁶⁾ **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

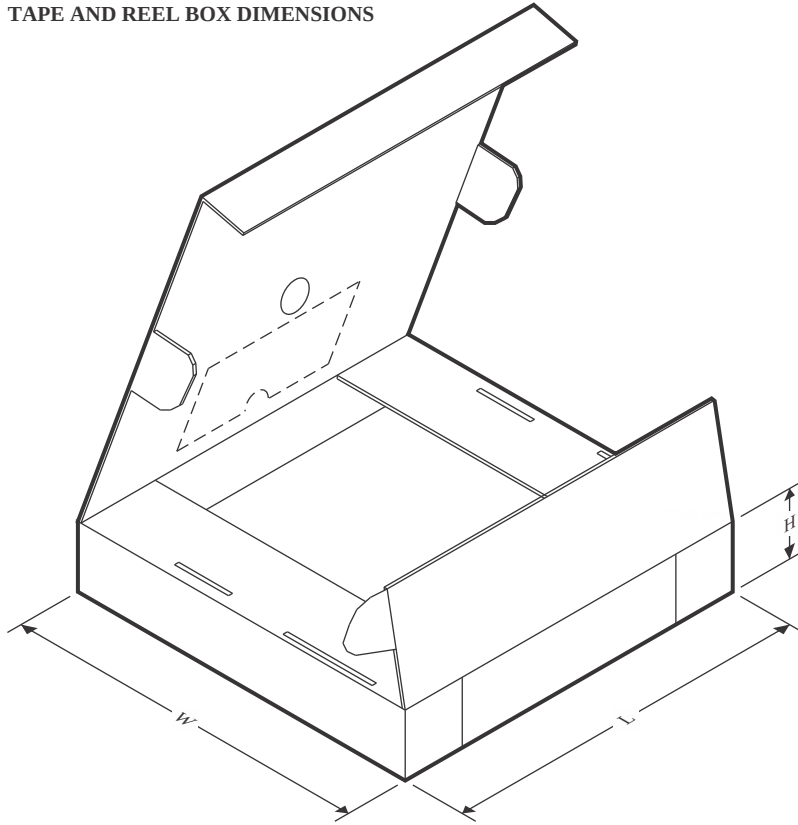
TAPE AND REEL INFORMATION



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TS5A22362DGSR	VSSOP	DGS	10	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
TS5A22362DRCR	VSON	DRC	10	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
TS5A22362DRCRG4	VSON	DRC	10	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
TS5A22362YZPR	DSBGA	YZP	10	3000	178.0	9.2	1.49	1.99	0.63	4.0	8.0	Q2

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

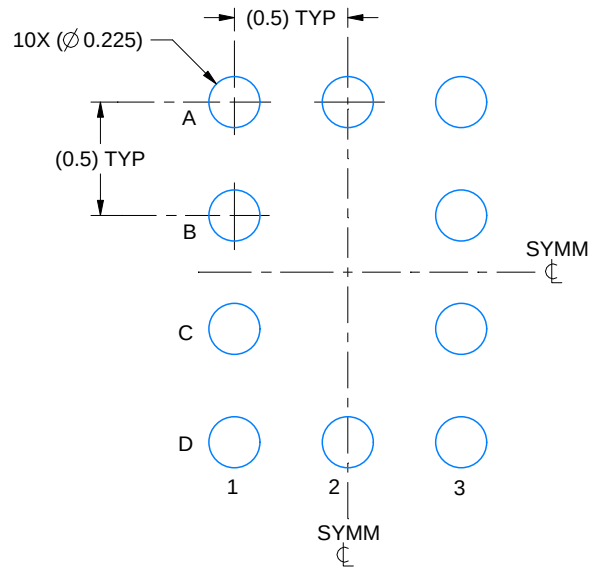
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TS5A22362DGSR	VSSOP	DGS	10	2500	358.0	335.0	35.0
TS5A22362DRCR	VSON	DRC	10	3000	353.0	353.0	32.0
TS5A22362DRCRG4	VSON	DRC	10	3000	353.0	353.0	32.0
TS5A22362YZPR	DSBGA	YZP	10	3000	220.0	220.0	35.0

EXAMPLE BOARD LAYOUT

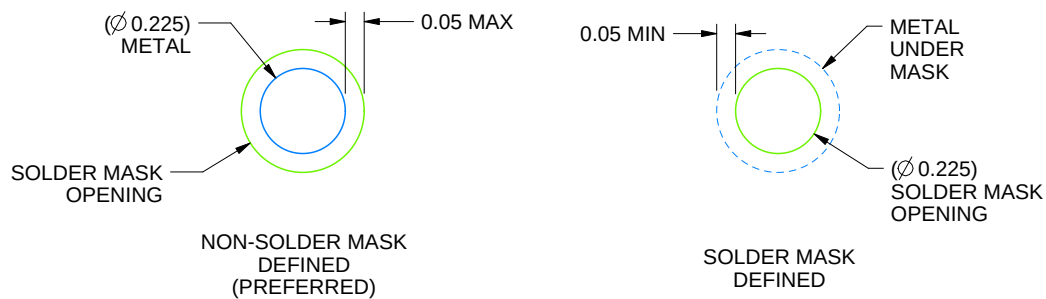
YZP0010

DSBGA - 0.5 mm max height

DIE SIZE BALL GRID ARRAY



LAND PATTERN EXAMPLE
SCALE:30X



SOLDER MASK DETAILS
NOT TO SCALE

4219350/B 11/2017

NOTES: (continued)

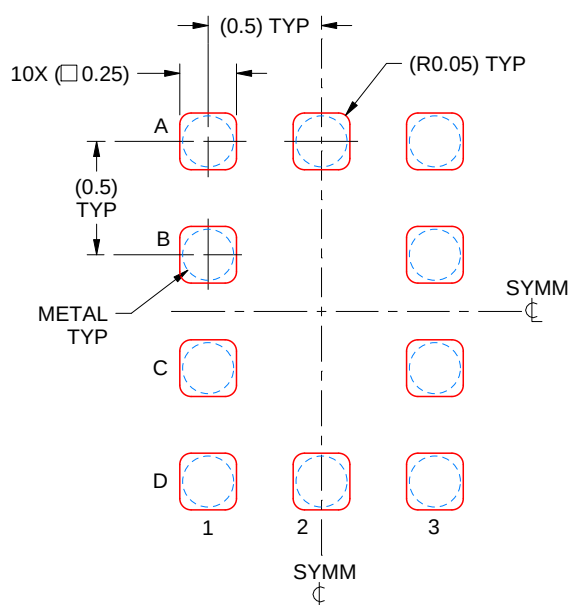
- Final dimensions may vary due to manufacturing tolerance considerations and also routing constraints. For more information, see Texas Instruments literature number SBVA017 (www.ti.com/lit/sbva017).

EXAMPLE STENCIL DESIGN

YZP0010

DSBGA - 0.5 mm max height

DIE SIZE BALL GRID ARRAY



SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICK STENCIL
SCALE:30X

4219350/B 11/2017

NOTES: (continued)

4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release.

GENERIC PACKAGE VIEW

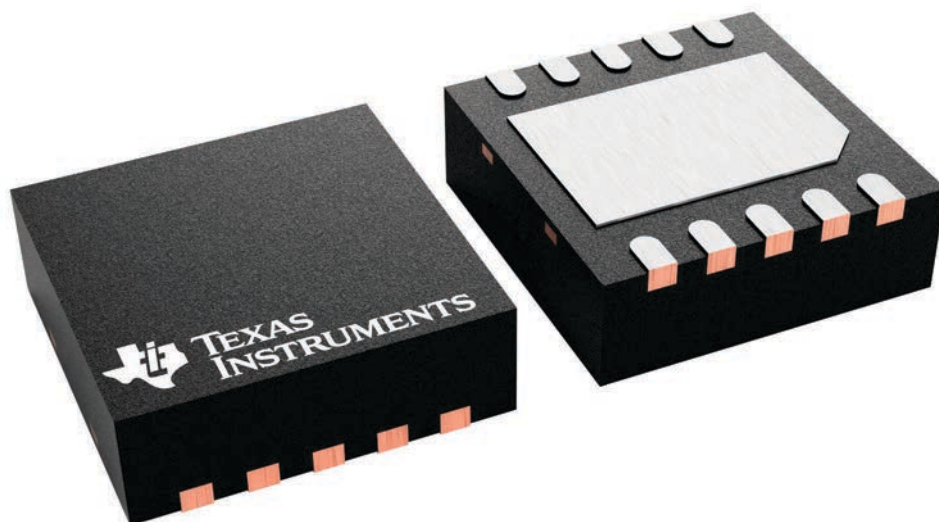
DRC 10

VSON - 1 mm max height

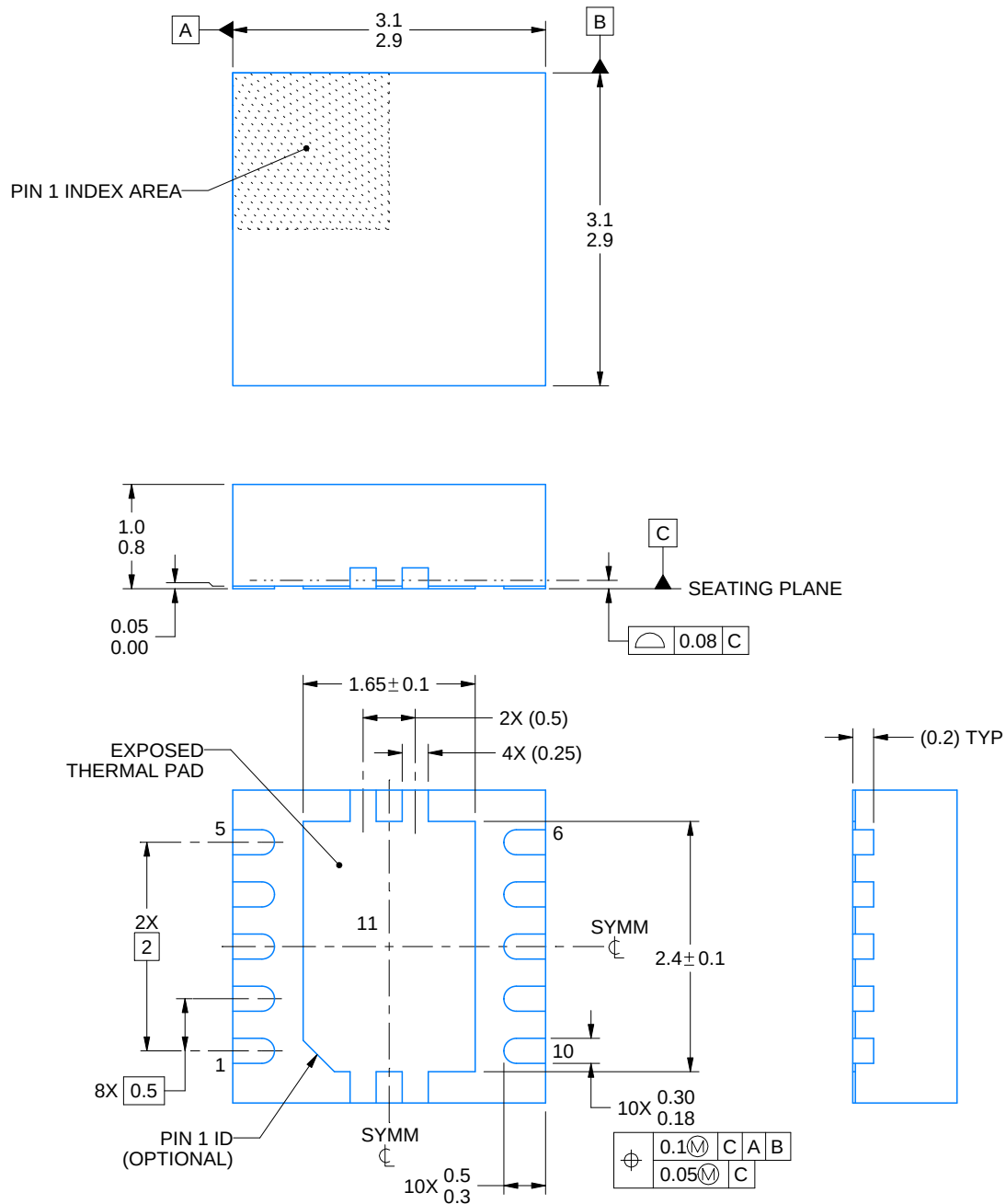
3 x 3, 0.5 mm pitch

PLASTIC SMALL OUTLINE - NO LEAD

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



4226193/A



4218878/B 07/2018

NOTES:

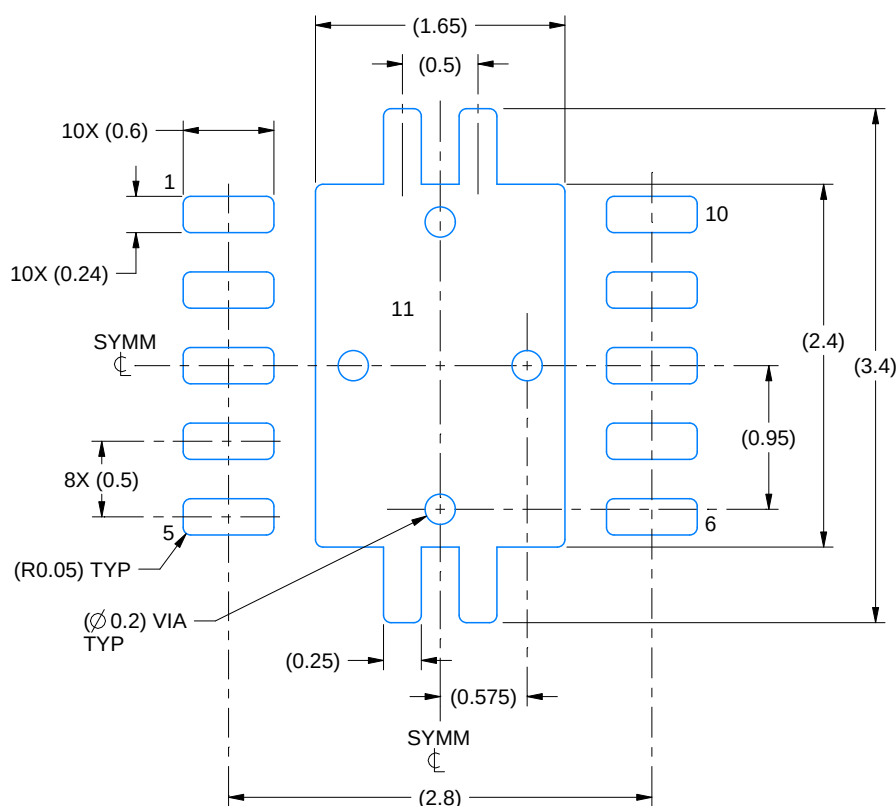
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for optimal thermal and mechanical performance.

EXAMPLE BOARD LAYOUT

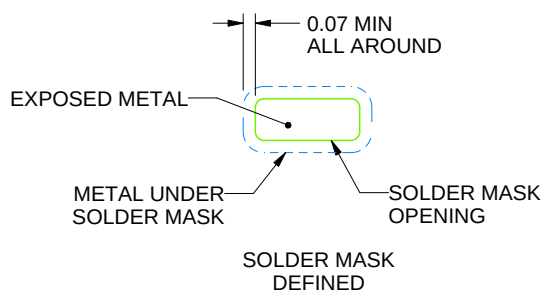
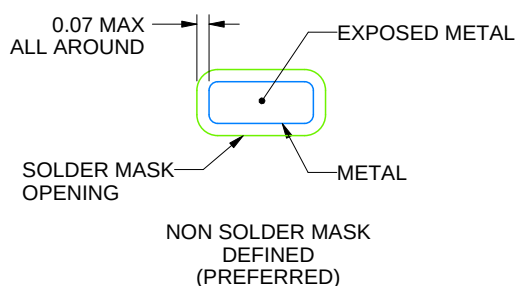
DRC0010J

VSON - 1 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:20X



SOLDER MASK DETAILS

4218878/B 07/2018

NOTES: (continued)

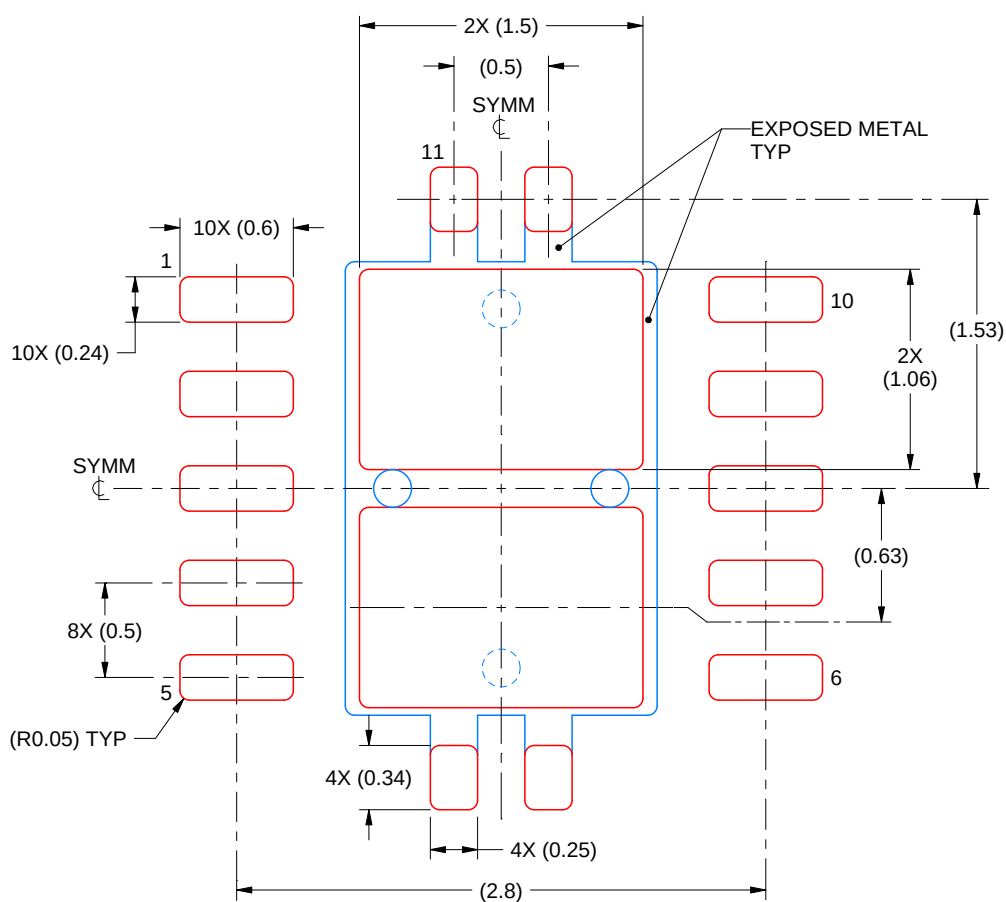
4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/sluea271).

5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.

DRC0010J

VSON - 1 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



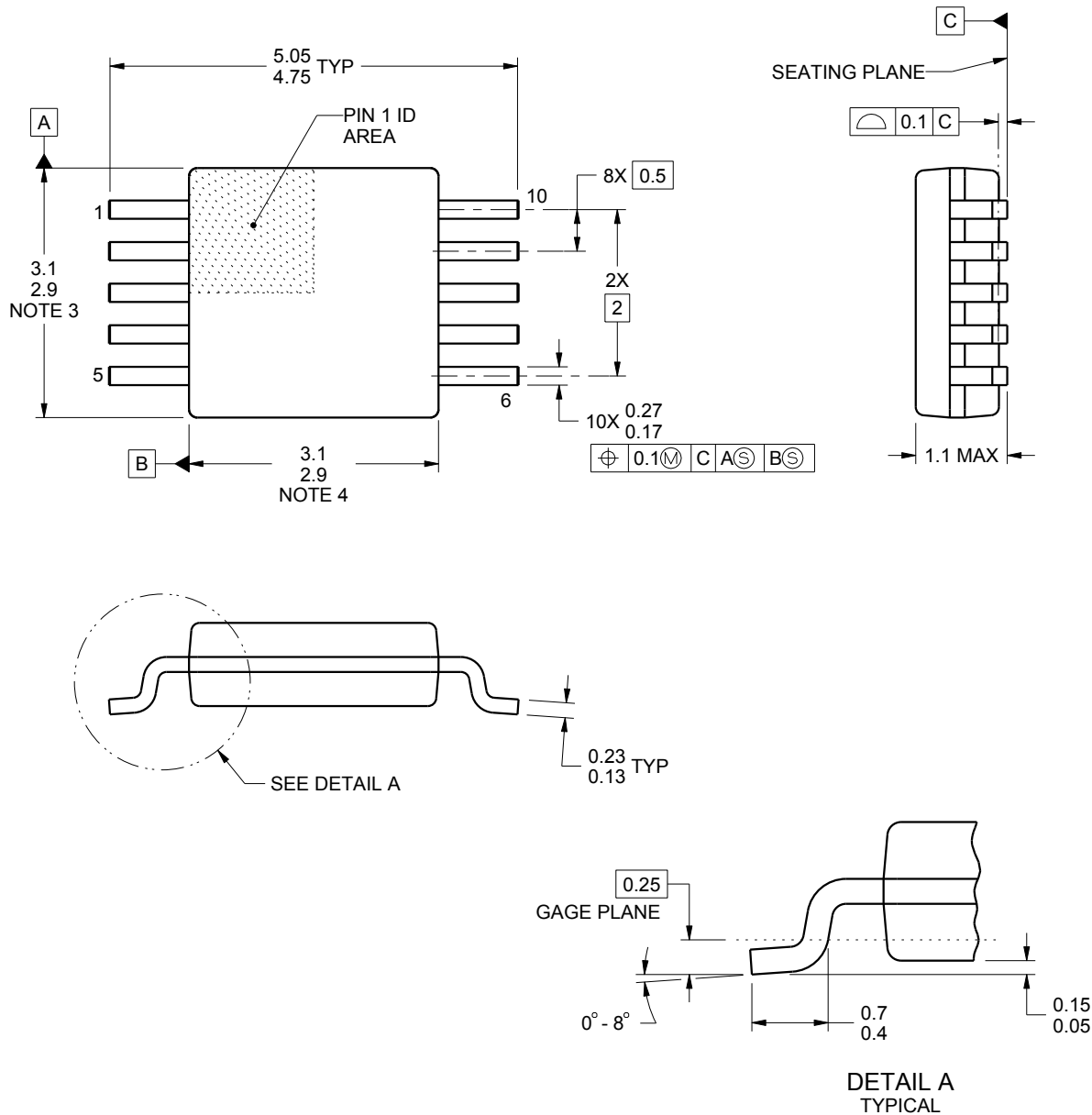
SOLDER PASTE EXAMPLE BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 11:
80% PRINTED SOLDER COVERAGE BY AREA
SCALE:25X

4218878/B 07/2018

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.



4221984/A 05/2015

NOTES:

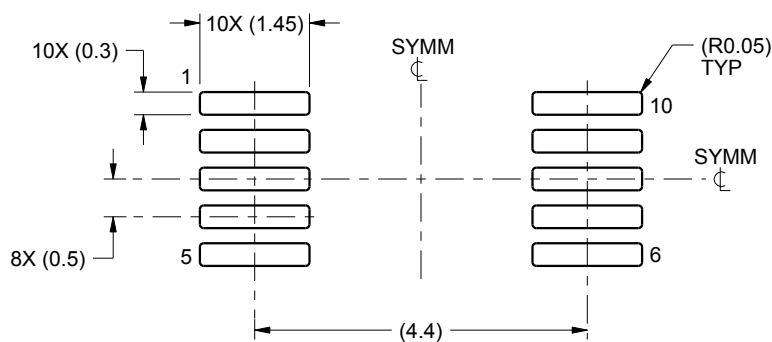
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-187, variation BA.

EXAMPLE BOARD LAYOUT

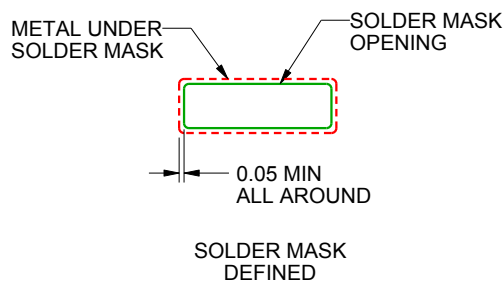
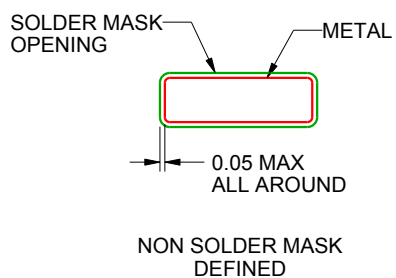
DGS0010A

VSSOP - 1.1 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE
SCALE:10X



SOLDER MASK DETAILS
NOT TO SCALE

4221984/A 05/2015

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

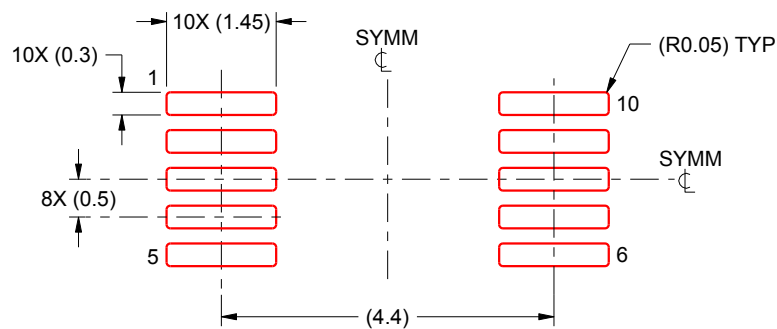
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DGS0010A

VSSOP - 1.1 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:10X

4221984/A 05/2015

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATASHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES "AS IS" AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, regulatory or other requirements.

These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you fully indemnify TI and its representatives against any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI's products are provided subject to [TI's Terms of Sale](#), [TI's General Quality Guidelines](#), or other applicable terms available either on [ti.com](#) or provided in conjunction with such TI products. TI's provision of these resources does not expand or otherwise alter TI's applicable warranties or warranty disclaimers for TI products. Unless TI explicitly designates a product as custom or customer-specified, TI products are standard, catalog, general purpose devices.

TI objects to and rejects any additional or different terms you may propose.

Copyright © 2025, Texas Instruments Incorporated

Last updated 10/2025