

FQB9N25C/FQI9N25C

250V N-Channel MOSFET

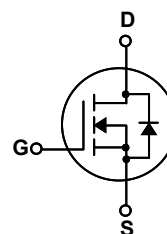
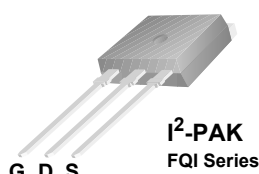
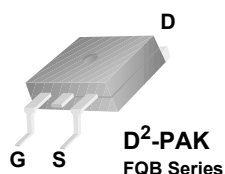
General Description

These N-Channel enhancement mode power field effect transistors are produced using Fairchild's proprietary, planar stripe, DMOS technology.

This advanced technology has been especially tailored to minimize on-state resistance, provide superior switching performance, and withstand high energy pulse in the avalanche and commutation mode. These devices are well suited for high efficiency switched mode power supplies, active power factor correction, electronic lamp ballasts based on half bridge topology.

Features

- 8.8A, 250V, $R_{DS(on)} = 0.43\Omega$ @ $V_{GS} = 10V$
- Low gate charge (typical 26.5 nC)
- Low C_{rss} (typical 45.5 pF)
- Fast switching
- 100% avalanche tested
- Improved dv/dt capability



Absolute Maximum Ratings $T_C = 25^\circ\text{C}$ unless otherwise noted

Symbol	Parameter	FQB9N25C / FQI9N25C	Units
V_{DSS}	Drain-Source Voltage	250	V
I_D	Drain Current - Continuous ($T_C = 25^\circ\text{C}$)	8.8	A
	- Continuous ($T_C = 100^\circ\text{C}$)	5.6	A
I_{DM}	Drain Current - Pulsed (Note 1)	35.2	A
V_{GSS}	Gate-Source Voltage	± 30	V
E_{AS}	Single Pulsed Avalanche Energy (Note 2)	285	mJ
I_{AR}	Avalanche Current (Note 1)	8.8	A
E_{AR}	Repetitive Avalanche Energy (Note 1)	7.4	mJ
dv/dt	Peak Diode Recovery dv/dt (Note 3)	5.5	V/ns
P_D	Power Dissipation ($T_A = 25^\circ\text{C}$)*	3.13	W
	Power Dissipation ($T_C = 25^\circ\text{C}$)	74	W
	- Derate above 25°C	0.59	W/ $^\circ\text{C}$
T_J, T_{STG}	Operating and Storage Temperature Range	-55 to +150	$^\circ\text{C}$
T_L	Maximum lead temperature for soldering purposes, 1/8" from case for 5 seconds	300	$^\circ\text{C}$

Thermal Characteristics

Symbol	Parameter	Typ	Max	Units
$R_{\theta JC}$	Thermal Resistance, Junction-to-Case	--	1.69	$^\circ\text{C}/\text{W}$
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient*	--	40	$^\circ\text{C}/\text{W}$
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient	--	62.5	$^\circ\text{C}/\text{W}$

* When mounted on the minimum pad size recommended (PCB Mount)

Electrical Characteristics

$T_C = 25^\circ\text{C}$ unless otherwise noted

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
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Off Characteristics

BV_{DSS}	Drain-Source Breakdown Voltage	$V_{GS} = 0\text{ V}, I_D = 250\text{ }\mu\text{A}$	250	--	--	V
$\Delta BV_{DSS} / \Delta T_J$	Breakdown Voltage Temperature Coefficient	$I_D = 250\text{ }\mu\text{A}$, Referenced to 25°C	--	0.30	--	V/ $^\circ\text{C}$
I_{DSS}	Zero Gate Voltage Drain Current	$V_{DS} = 250\text{ V}, V_{GS} = 0\text{ V}$	--	--	10	μA
		$V_{DS} = 200\text{ V}, T_C = 125^\circ\text{C}$	--	--	100	μA
I_{GSSF}	Gate-Body Leakage Current, Forward	$V_{GS} = 30\text{ V}, V_{DS} = 0\text{ V}$	--	--	100	nA
I_{GSSR}	Gate-Body Leakage Current, Reverse	$V_{GS} = -30\text{ V}, V_{DS} = 0\text{ V}$	--	--	-100	nA

On Characteristics

$V_{GS(th)}$	Gate Threshold Voltage	$V_{DS} = V_{GS}, I_D = 250\text{ }\mu\text{A}$	2.0	--	4.0	V
$R_{DS(on)}$	Static Drain-Source On-Resistance	$V_{GS} = 10\text{ V}, I_D = 4.4\text{ A}$	--	0.35	0.43	Ω
g_{FS}	Forward Transconductance	$V_{DS} = 40\text{ V}, I_D = 4.4\text{ A}$ (Note 4)	--	7.0	--	S

Dynamic Characteristics

C_{iss}	Input Capacitance	$V_{DS} = 25\text{ V}, V_{GS} = 0\text{ V},$ $f = 1.0\text{ MHz}$	--	545	710	pF
C_{oss}	Output Capacitance		--	115	150	pF
C_{rss}	Reverse Transfer Capacitance		--	45.5	60	pF

Switching Characteristics

$t_{d(on)}$	Turn-On Delay Time	$V_{DD} = 125\text{ V}, I_D = 8.8\text{ A},$ $R_G = 25\text{ }\Omega$ (Note 4, 5)	--	15	40	ns
t_r	Turn-On Rise Time		--	85	180	ns
$t_{d(off)}$	Turn-Off Delay Time		--	90	190	ns
t_f	Turn-Off Fall Time		--	65	140	ns
Q_g	Total Gate Charge	$V_{DS} = 200\text{ V}, I_D = 8.8\text{ A},$ $V_{GS} = 10\text{ V}$ (Note 4, 5)	--	26.5	35	nC
Q_{gs}	Gate-Source Charge		--	3.5	--	nC
Q_{gd}	Gate-Drain Charge		--	13.5	--	nC

Drain-Source Diode Characteristics and Maximum Ratings

I _S	Maximum Continuous Drain-Source Diode Forward Current		--	--	8.8	A
I _{SM}	Maximum Pulsed Drain-Source Diode Forward Current		--	--	35.2	A
V _{SD}	Drain-Source Diode Forward Voltage	V _{GS} = 0 V, I _S = 8.8 A	--	--	1.5	V
t _{rr}	Reverse Recovery Time	V _{GS} = 0 V, I _S = 8.8 A,	--	218	--	ns
Q _{rr}	Reverse Recovery Charge	dI _F / dt = 100 A/μs (Note 4)	--	1.58	--	μC

Notes:

1. Repetitive Rating : Pulse width limited by maximum junction temperature
2. $L = 5.9\text{ mH}$, $I_{AS} = 8.8\text{ A}$, $V_{DD} = 50\text{ V}$, $R_G = 25\text{ }\Omega$, Starting $T_J = 25^\circ\text{C}$
3. $I_{SD} \leq 8.8\text{ A}$, $di/dt \leq 300\text{ A}/\mu\text{s}$, $V_{DD} \leq BV_{DSS}$, Starting $T_J = 25^\circ\text{C}$
4. Pulse Test : Pulse width $\leq 300\text{ }\mu\text{s}$, Duty cycle $\leq 2\%$
5. Essentially independent of operating temperature

Typical Characteristics

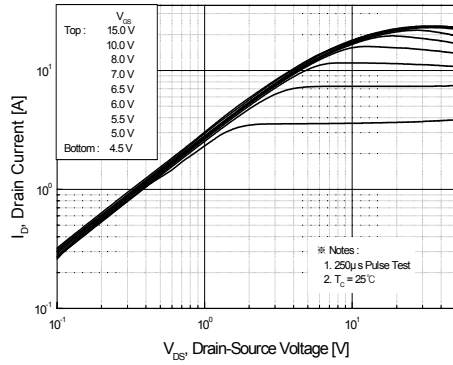


Figure 1. On-Region Characteristics

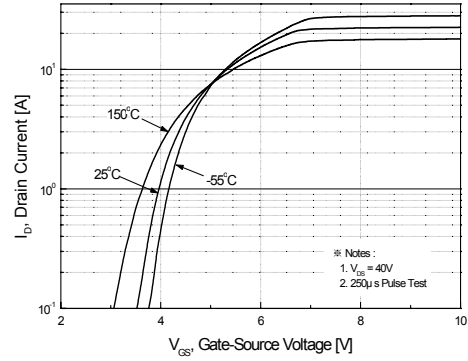


Figure 2. Transfer Characteristics

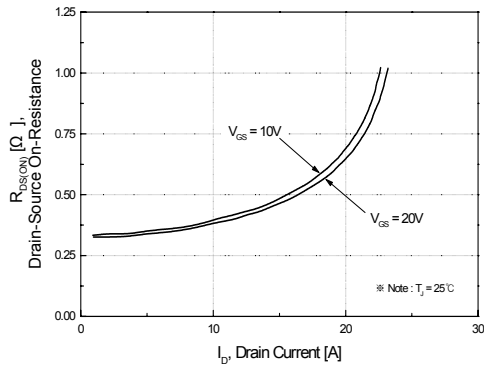


Figure 3. On-Resistance Variation vs Drain Current and Gate Voltage

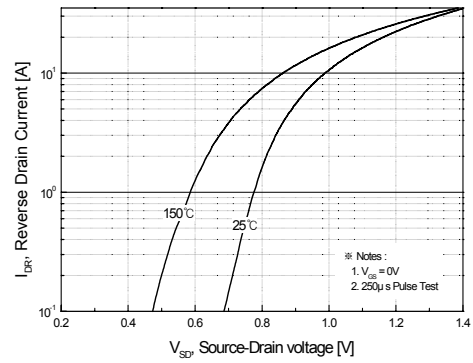


Figure 4. Body Diode Forward Voltage Variation with Source Current and Temperature

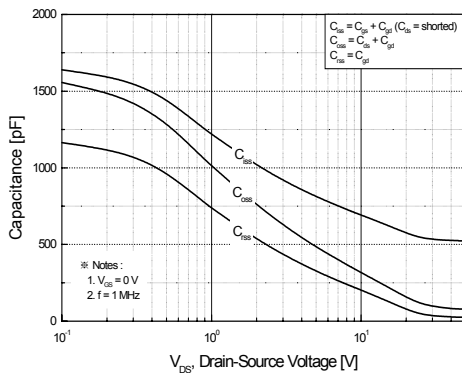


Figure 5. Capacitance Characteristics

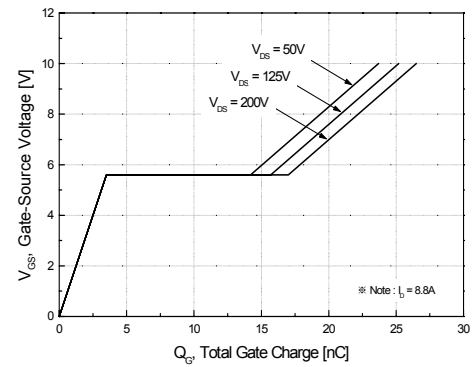


Figure 6. Gate Charge Characteristics

Typical Characteristics (Continued)

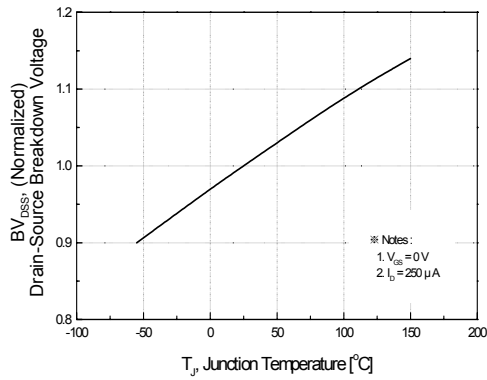


Figure 7. Breakdown Voltage Variation vs Temperature

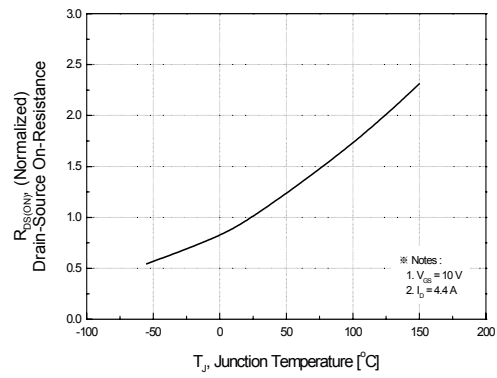


Figure 8. On-Resistance Variation vs Temperature

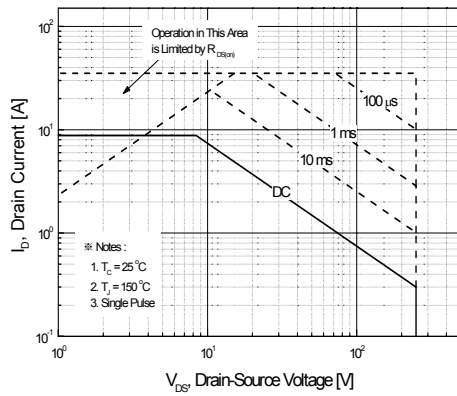


Figure 9. Maximum Safe Operating Area

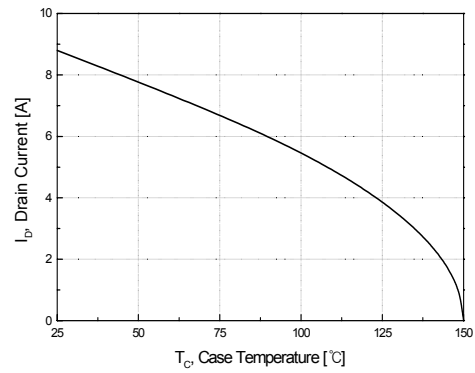


Figure 10. Maximum Drain Current vs Case Temperature

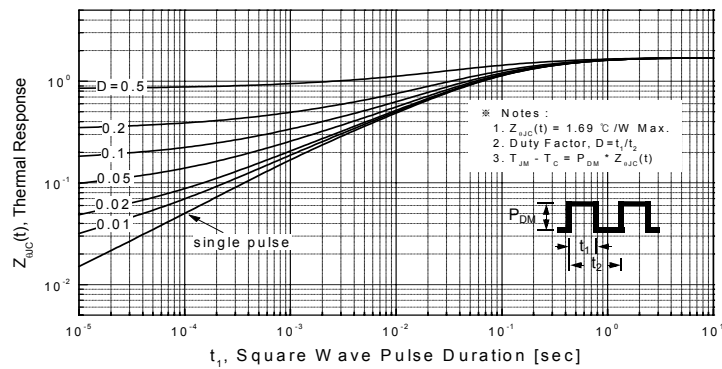
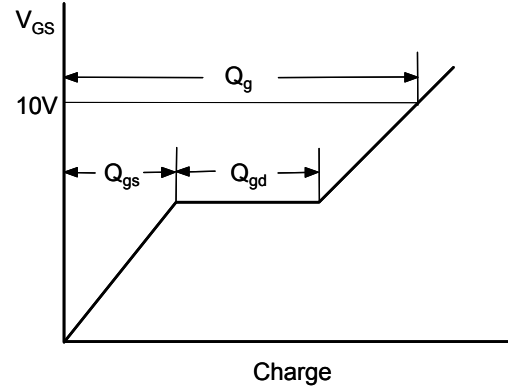
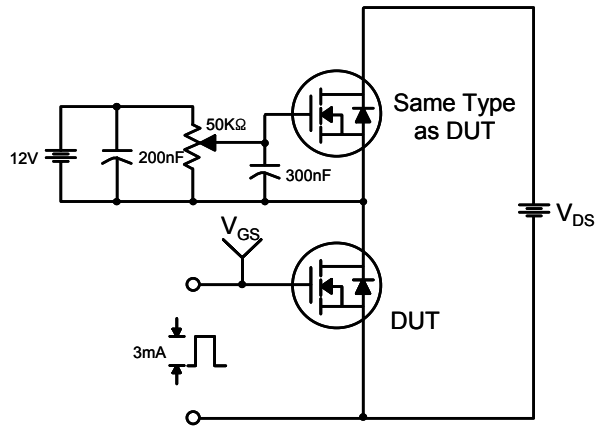
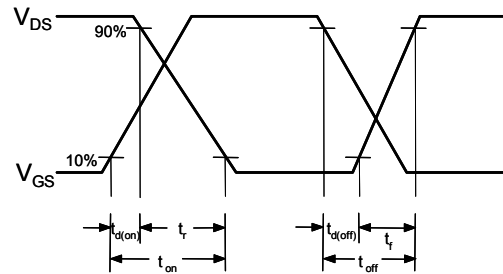
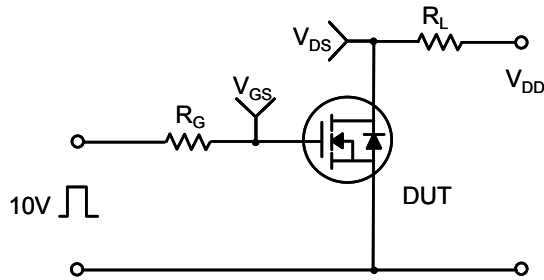


Figure 11. Transient Thermal Response Curve

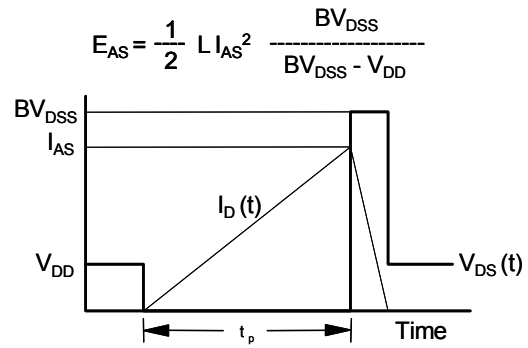
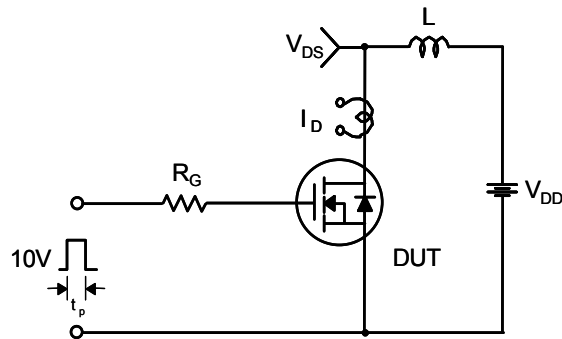
Gate Charge Test Circuit & Waveform



Resistive Switching Test Circuit & Waveforms



Unclamped Inductive Switching Test Circuit & Waveforms



FQB9N25C/FQI9N25C

Technical drawing of a 10-pin D-subminiature connector, showing three views: front, side, and top. Dimensions are in millimeters.

Front View:

- Overall width: 9.90 ± 0.20
- Overall height: 15.30 ± 0.30
- Pin height: 1.40 ± 0.20
- Pin pitch: 2.54 TYP
- Pin diameter: 0.80 ± 0.10
- Internal width: 1.27 ± 0.10
- Internal height: 1.20 ± 0.20
- Internal width (bottom): 4.90 ± 0.20
- Internal height (bottom): 9.20 ± 0.20

Side View:

- Overall width: 4.50 ± 0.20
- Overall height: 15.30 ± 0.30
- Pin height: 1.40 ± 0.20
- Pin pitch: 2.54 ± 0.30
- Pin diameter: 0.80 ± 0.10
- Internal width: 1.27 ± 0.10
- Internal height: 1.20 ± 0.20
- Internal width (bottom): 4.90 ± 0.20
- Internal height (bottom): 9.20 ± 0.20

Top View:

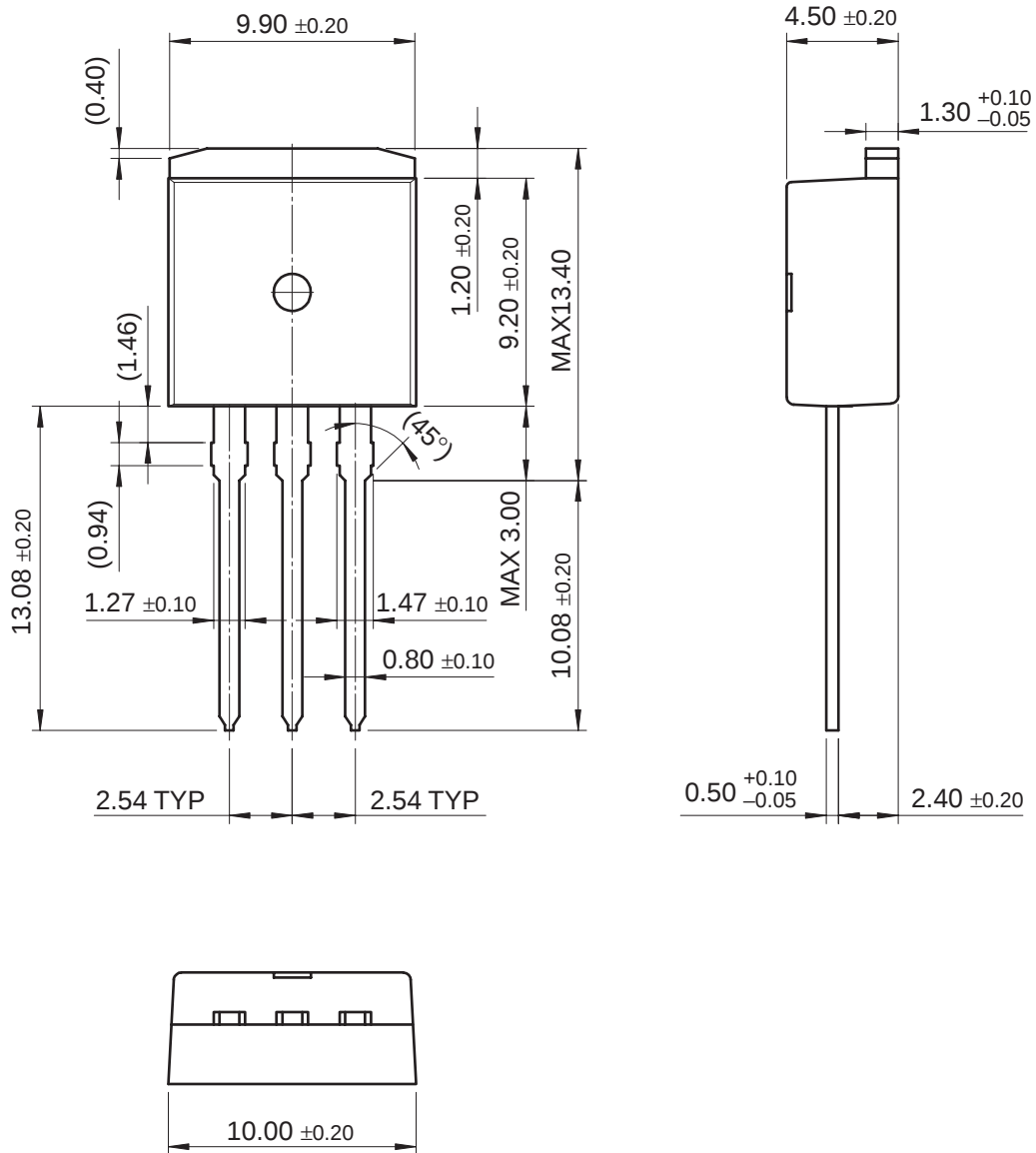
- Overall width: 10.00 ± 0.20
- Overall height: 15.30 ± 0.30
- Pin height: 1.40 ± 0.20
- Pin pitch: 2.54 TYP
- Pin diameter: 0.80 ± 0.10
- Internal width: 1.27 ± 0.10
- Internal height: 1.20 ± 0.20
- Internal width (bottom): 4.90 ± 0.20
- Internal height (bottom): 9.20 ± 0.20

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Rev. A, March 2004

Package Dimensions (Continued)

I²-PAK



Dimensions in Millimeters

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CoolFET™	FPS™	MicroFET™	PowerTrench®	SuperSOT™-6
CROSSVOLT™	FRFET™	MicroPak™	QFET®	SuperSOT™-8
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No Identification Needed	Full Production	This datasheet contains final specifications. Fairchild Semiconductor reserves the right to make changes at any time without notice in order to improve design.
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FQB9N25C

250V N-Channel Advance Q-FET C-Series

Contents

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General description

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Product status/pricing/packaging

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Product	Product status	Pb-free Status	Pricing*	Package type	Leads	Packing method	Package Marking Convention**

FQB9N25CTM	Full Production		\$1.02	TO-263(D2PAK)	2	TAPE REEL	Line 1: \$Y (Fairchild logo) & Z (Asm. Plant Code) & 4 (4-Digit Date Code)
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* Fairchild 1,000 piece Budgetary Pricing

** A sample button will appear if the part is available through Fairchild's on-line samples program. If there is no sample button, please contact a [Fairchild distributor](#) to obtain samples



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Qualification Support

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FQB9N25CTM

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