

To our customers,

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Renesas Electronics website: <http://www.renesas.com>

April 1st, 2010
Renesas Electronics Corporation

Issued by: Renesas Electronics Corporation (<http://www.renesas.com>)

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2SJ550(L), 2SJ550(S)

Silicon P Channel MOS FET

REJ03G0897-0300
(Previous: ADE-208-633A)
Rev.3.00
Sep 07, 2005

Description

High speed power switching

Features

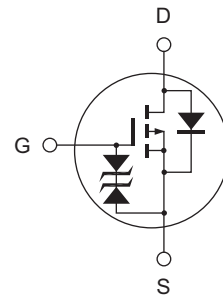
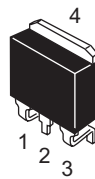
- Low on-resistance
 $R_{DS(on)} = 0.075 \Omega$ typ.
- Low drive current.
- 4 V gate drive devices.
- High speed switching.

Outline

RENESAS Package code: PRSS0004AE-A
(Package name: LDKPAK (L))



RENESAS Package code: PRSS0004AE-B
(Package name: LDKPAK (S)-(1))



1. Gate
2. Drain
3. Source
4. Drain

Absolute Maximum Ratings

(Ta = 25°C)

Item	Symbol	Value	Unit
Drain to source voltage	V_{DS}	-60	V
Gate to source voltage	V_{GS}	±20	V
Drain current	I_D	-15	A
Drain peak current	$I_{D(pulse)}$ ^{Note 1}	-60	A
Body to drain diode reverse drain current	I_{DR}	-15	A
Avalanche current	I_{AP} ^{Note 3}	-15	A
Avalanche energy	E_{AR} ^{Note 3}	19	mJ
Channel dissipation	P_{ch} ^{Note 2}	50	W
Channel temperature	T_{ch}	150	°C
Storage temperature	T_{stg}	-55 to +150	°C

Notes: 1. $PW \leq 10 \mu s$, duty cycle $\leq 1\%$ 2. Value at $T_c = 25^\circ C$ 3. Value at $T_{ch} = 25^\circ C$, $R_g \geq 50 \Omega$

Electrical Characteristics

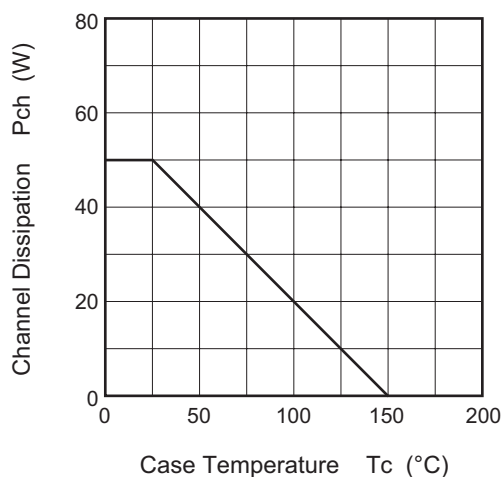
(Ta = 25°C)

Item	Symbol	Min	Typ	Max	Unit	Test Conditions
Drain to source breakdown voltage	$V_{(BR)DSS}$	-60	—	—	V	$I_D = -10 \text{ mA}$, $V_{GS} = 0$
Gate to source breakdown voltage	$V_{(BR)GSS}$	±20	—	—	V	$I_G = \pm 100 \mu A$, $V_{DS} = 0$
Zero gate voltage drain current	I_{DSS}	—	—	-10	μA	$V_{DS} = -60 \text{ V}$, $V_{GS} = 0$
Gate to source leak current	I_{GSS}	—	—	±10	μA	$V_{GS} = \pm 16 \text{ V}$, $V_{DS} = 0$
Gate to source cutoff voltage	$V_{GS(off)}$	-1.0	—	-2.0	V	$I_D = -1 \text{ mA}$, $V_{DS} = -10 \text{ V}$
Static drain to source on state resistance	$R_{DS(on)}$	—	0.075	0.095	Ω	$I_D = -8 \text{ A}$, $V_{GS} = -10 \text{ V}$ ^{Note 4}
	$R_{DS(on)}$	—	0.105	0.155	Ω	$I_D = -8 \text{ A}$, $V_{GS} = -4 \text{ V}$ ^{Note 4}
Forward transfer admittance	$ y_{fs} $	6.5	11	—	S	$I_D = -8 \text{ A}$, $V_{DS} = -10 \text{ V}$ ^{Note 4}
Input capacitance	C_{iss}	—	850	—	pF	$V_{DS} = -10 \text{ V}$
Output capacitance	C_{oss}	—	420	—	pF	$V_{GS} = 0$
Reverse transfer capacitance	C_{rss}	—	110	—	pF	$f = 1 \text{ MHz}$
Turn-on delay time	$t_{d(on)}$	—	12	—	ns	$V_{GS} = -10 \text{ V}$
Rise time	t_r	—	75	—	ns	$I_D = -8 \text{ A}$
Turn-off delay time	$t_{d(off)}$	—	125	—	ns	$R_L = 3.75 \Omega$
Fall time	t_f	—	75	—	ns	
Body to drain diode forward voltage	V_{DF}	—	-1.1	—	V	$I_F = -15 \text{ A}$, $V_{GS} = 0$
Body to drain diode reverse recovery time	t_{rr}	—	70	—	ns	$I_F = -15 \text{ A}$, $V_{GS} = 0$ $di_F/dt = 50 \text{ A}/\mu s$

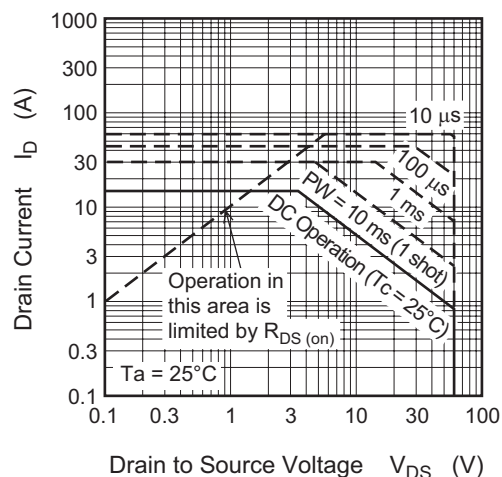
Note: 4. Pulse test

Main Characteristics

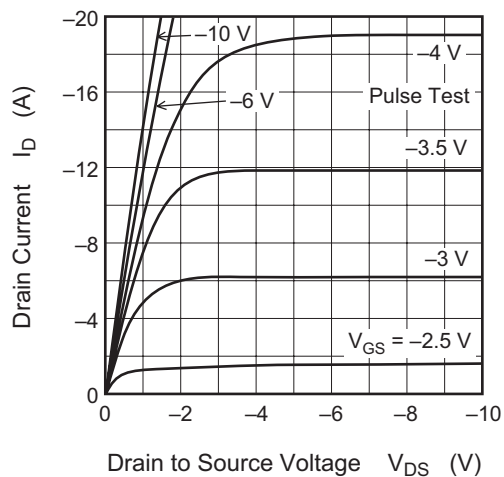
Power vs. Temperature Derating



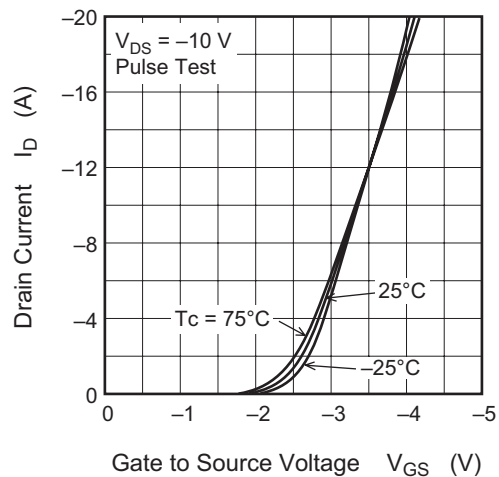
Maximum Safe Operation Area



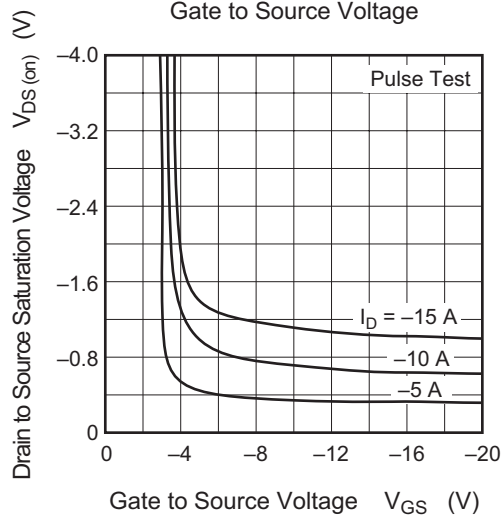
Typical Output Characteristics



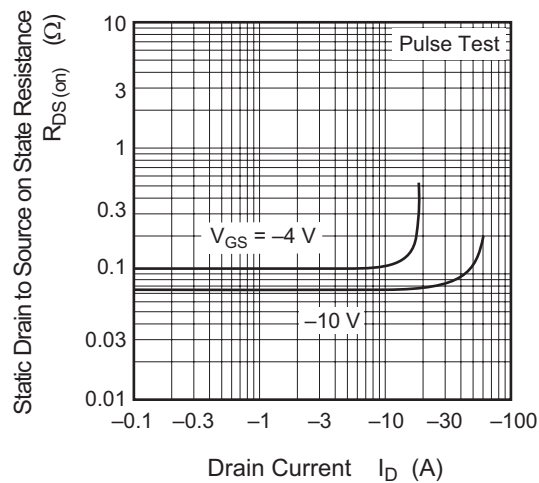
Typical Transfer Characteristics

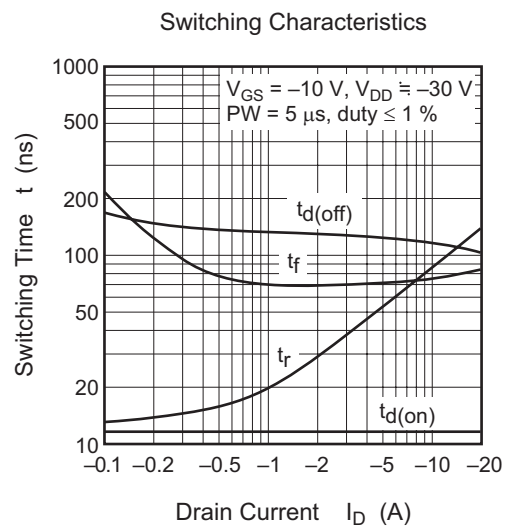
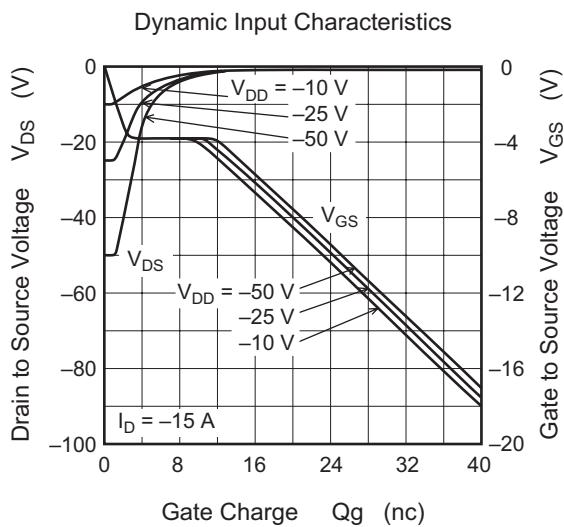
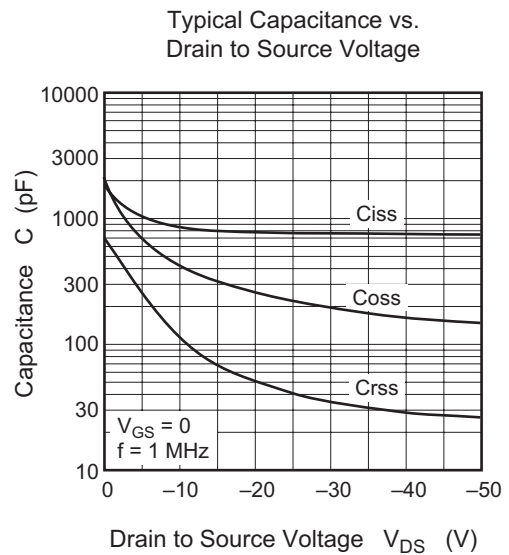
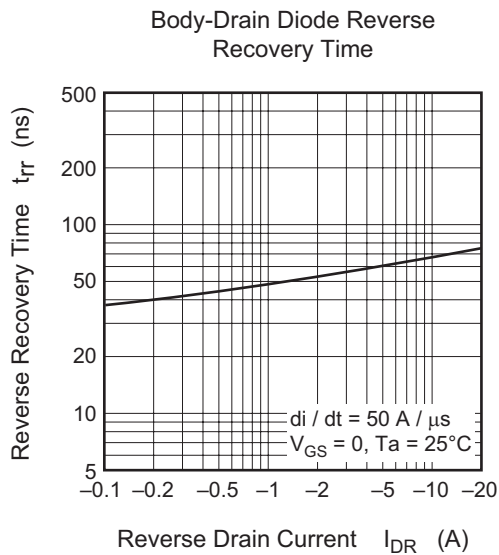
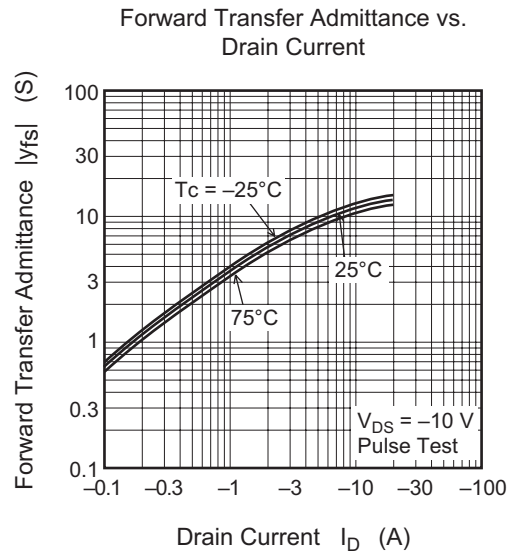
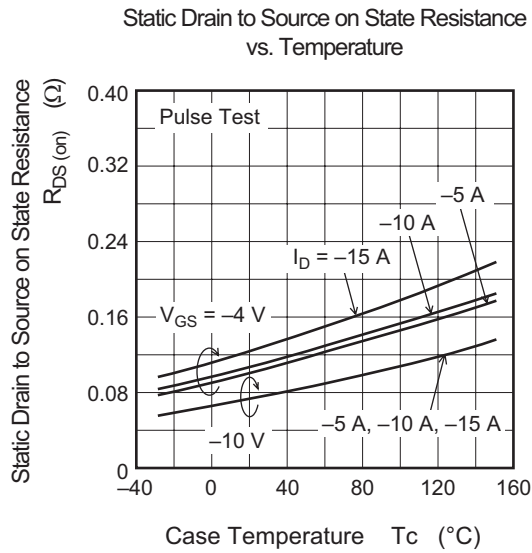


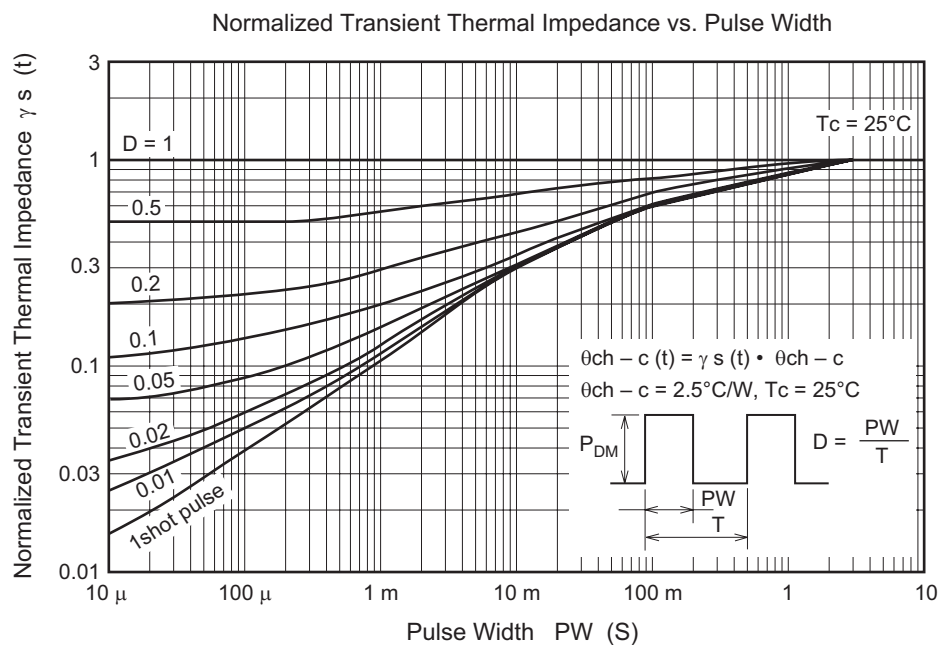
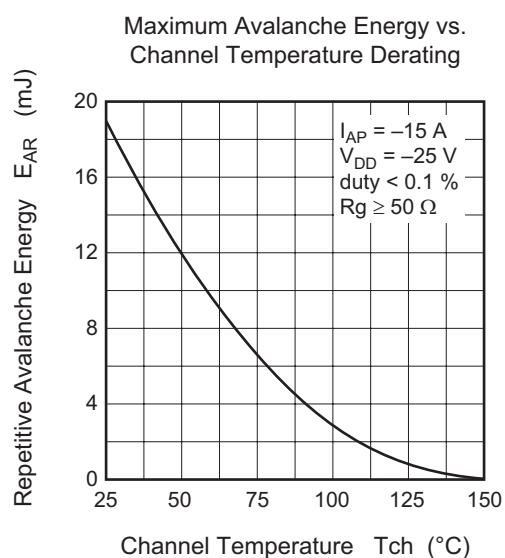
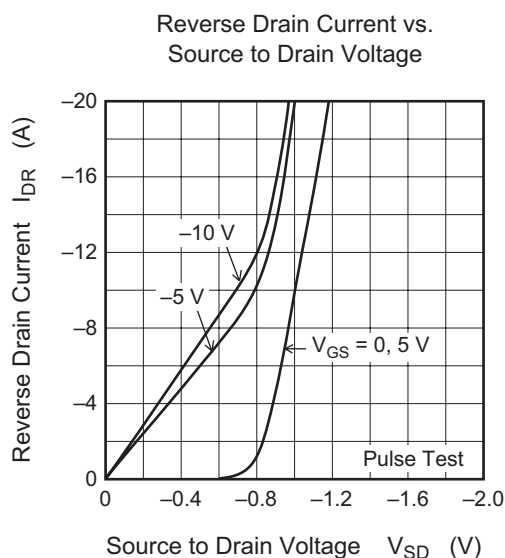
Drain to Source Saturation Voltage vs. Gate to Source Voltage



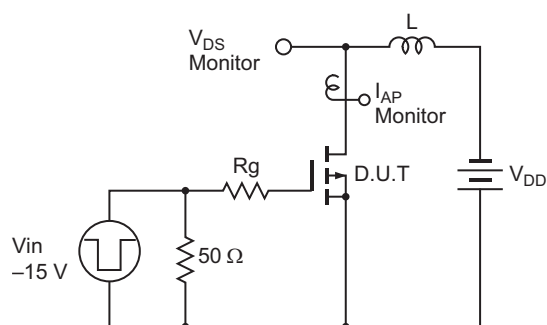
Static Drain to Source on State Resistance vs. Drain Current





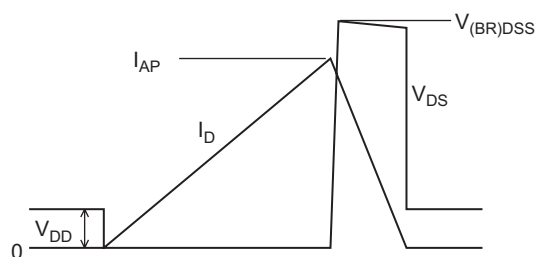


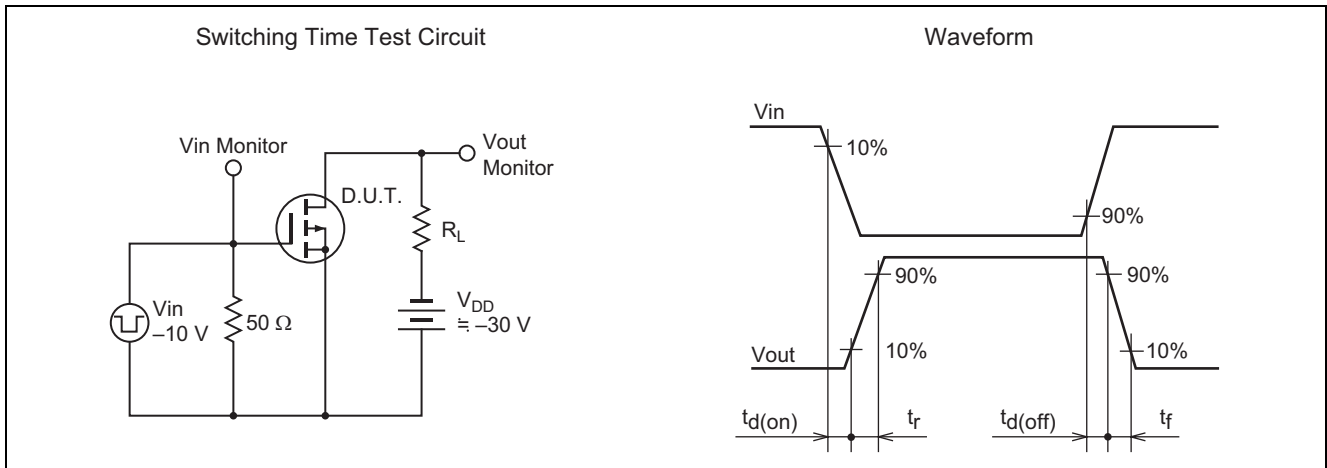
Avalanche Test Circuit



Avalanche Waveform

$$E_{AR} = \frac{1}{2} \cdot L \cdot I_{AP}^2 \cdot \frac{V_{DSS}}{V_{DSS} - V_{DD}}$$

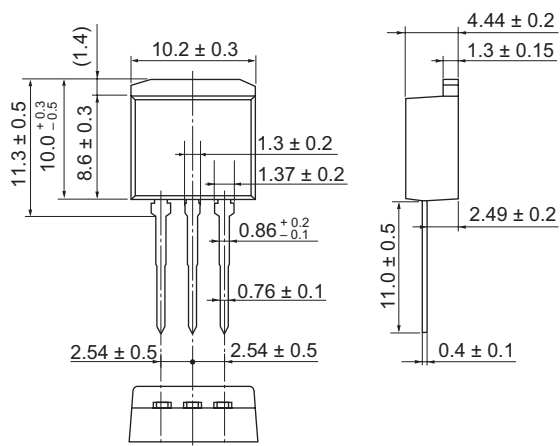




Package Dimensions

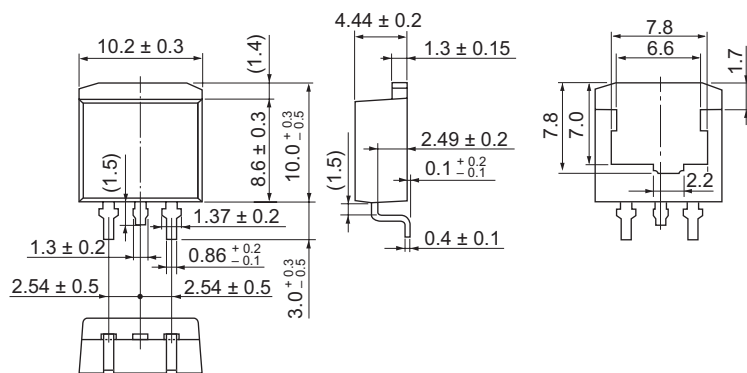
JEITA Package Code	RENESAS Code	Package Name	MASS[Typ.]
—	PRSS0004AE-A	LDBAK(L) / LDBAK(L)V	1.40g

Unit: mm



JEITA Package Code	RENESAS Code	Package Name	MASS[Typ.]
SC-83	PRSS0004AE-B	LDBAK(S)(1) / LDBAK(S)(1)V	1.30g

Unit: mm



Ordering Information

Part Name	Quantity	Shipping Container
2SJ550L-E	500 pcs	Box (Sack)
2SJ550STL-E	1000 pcs	Taping

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