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Renesas Electronics website: <http://www.renesas.com>

April 1st, 2010
Renesas Electronics Corporation

Issued by: Renesas Electronics Corporation (<http://www.renesas.com>)

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HAT1139H

Silicon P Channel Power MOS FET Power Switching

REJ03G1244-0200

Rev.2.00

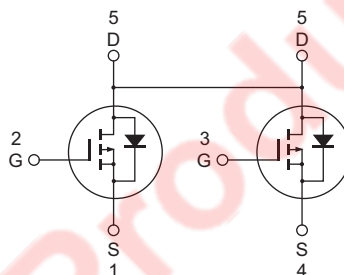
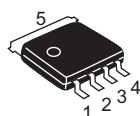
Jun.22.2005

Features

- Capable of -4.5 V gate drive
- Low drive current
- High density mounting
- Low on-resistance
 $R_{DS(on)} = 7.0$ m Ω typ. (at $V_{GS} = -10$ V)

Outline

RENESAS Package code: PTZZ0005DA-A
(Package name: LFPAK)



1, 4 Source
2, 3 Gate
5 Drain

Absolute Maximum Ratings

($T_a = 25^\circ\text{C}$)

Item	Symbol	Ratings	Unit
Drain to source voltage	V_{DSS}	-30	V
Gate to source voltage	V_{GSS}	$-25 / +20$	V
Drain current	I_D	-30	A
Drain peak current	$I_{D(pulse)}$ ^{Note1}	-120	A
Body-drain diode reverse drain current	I_{DR}	-30	A
Channel dissipation	P_{ch} ^{Note2}	15	W
Channel dissipation	P_{ch} ^{Note3}	30	W
Channel temperature	T_{ch}	150	$^\circ\text{C}$
Storage temperature	T_{stg}	-55 to $+150$	$^\circ\text{C}$

Notes: 1. $PW \leq 10$ μs , duty cycle $\leq 1\%$

2. 1 Drive operation : $T_c = 25^\circ\text{C}$

3. 2 Drive operation : $T_c = 25^\circ\text{C}$

Electrical Characteristics

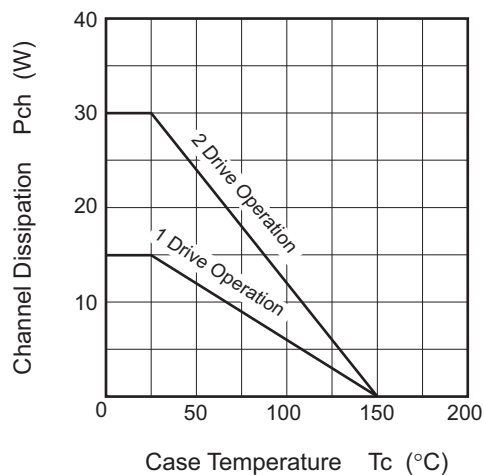
(Ta = 25°C)

Item	Symbol	Min	Typ	Max	Unit	Test Conditions
Drain to source breakdown voltage	$V_{(BR)DSS}$	-30	—	—	V	$I_D = -10 \text{ mA}$, $V_{GS} = 0$
Gate to source leak current	I_{GSS}	—	—	± 0.1	μA	$V_{GS} = -20/+10 \text{ V}$, $V_{DS} = 0$
Zero gate voltage drain current	I_{DSS}	—	—	-1	μA	$V_{DS} = -30 \text{ V}$, $V_{GS} = 0$
Gate to source cutoff voltage	$V_{GS(off)}$	-1.0	—	-2.5	V	$V_{DS} = -10 \text{ V}$, $I_D = -1 \text{ mA}$
Static drain to source on state resistance	$R_{DS(on)}$	—	7.0	9.0	$\text{m}\Omega$	$I_D = -15 \text{ A}$, $V_{GS} = -10 \text{ V}$ ^{Note4}
	$R_{DS(on)}$	—	10.0	14.5	$\text{m}\Omega$	$I_D = -15 \text{ A}$, $V_{GS} = -4.5 \text{ V}$ ^{Note4}
Forward transfer admittance	$ y_{fs} $	27	45	—	S	$I_D = -15 \text{ A}$, $V_{DS} = -10 \text{ V}$ ^{Note4}
Input capacitance	C_{iss}	—	3200	—	pF	$V_{DS} = -10 \text{ V}$, $V_{GS} = 0$, $f = 1 \text{ MHz}$
Output capacitance	C_{oss}	—	720	—	pF	
Reverse transfer capacitance	C_{rss}	—	550	—	pF	
Total gate charge	Q_g	—	73	—	nc	$V_{DD} = -10 \text{ V}$, $V_{GS} = -10 \text{ V}$, $I_D = -30 \text{ A}$
Gate to source charge	Q_{gs}	—	8	—	nc	
Gate to drain charge	Q_{gd}	—	14	—	nc	
Turn-on delay time	$t_{d(on)}$	—	23	—	ns	$V_{GS} = -10 \text{ V}$, $I_D = -15 \text{ A}$, $V_{DD} \cong -10 \text{ V}$, $R_L = 0.67 \Omega$, $R_g = 4.7 \Omega$
Rise time	t_r	—	48	—	ns	
Turn-off delay time	$t_{d(off)}$	—	247	—	ns	
Fall time	t_f	—	186	—	ns	$I_F = -30 \text{ A}$, $V_{GS} = 0$ ^{Note4}
Body-drain diode forward voltage	V_{DF}	—	-0.91	-1.19	V	
Body-drain diode reverse recovery time	t_{rr}	—	185	—	ns	$I_F = -30 \text{ A}$, $V_{GS} = 0$ $diF/dt = 100 \text{ A}/\mu\text{s}$

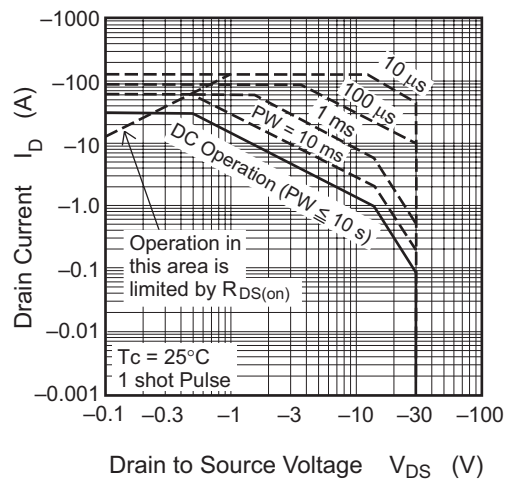
Notes: 4. Pulse test

Main Characteristics

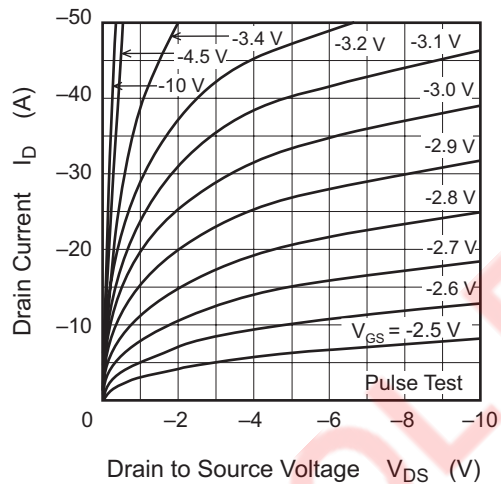
Power vs. Temperature Derating



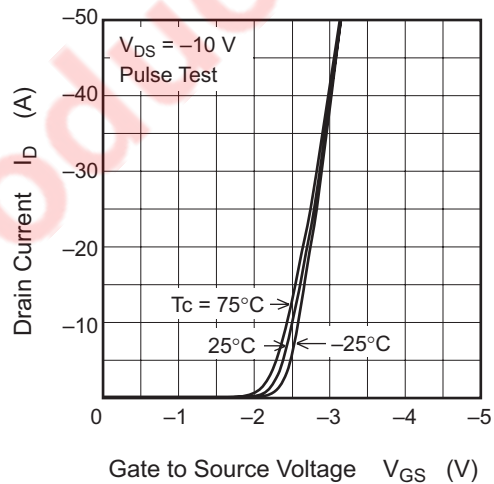
Maximum Safe Operation Area



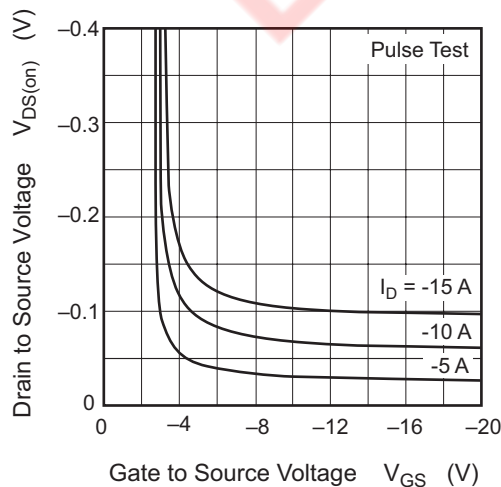
Typical Output Characteristics



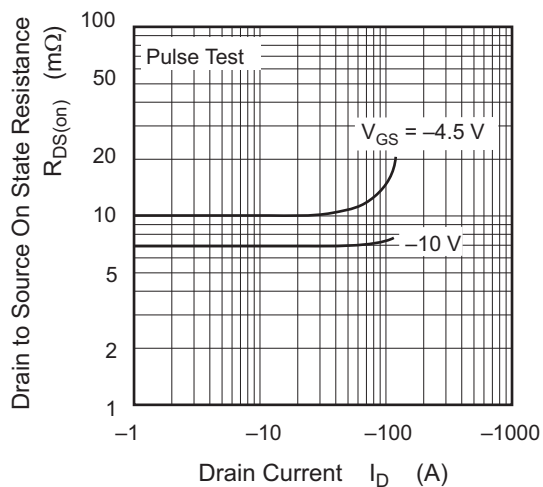
Typical Transfer Characteristics

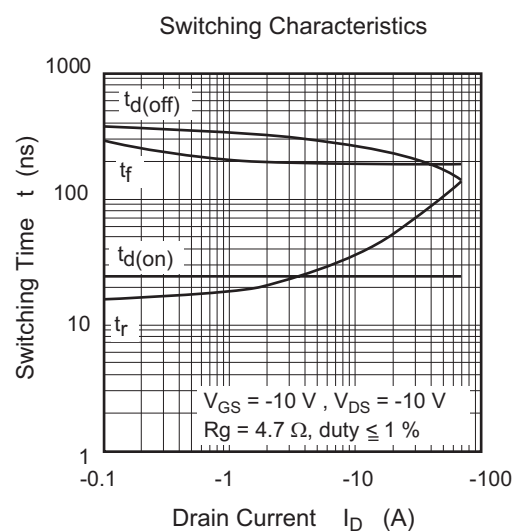
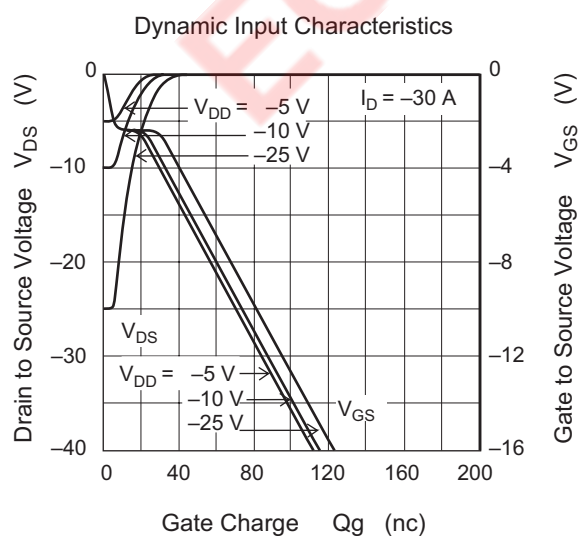
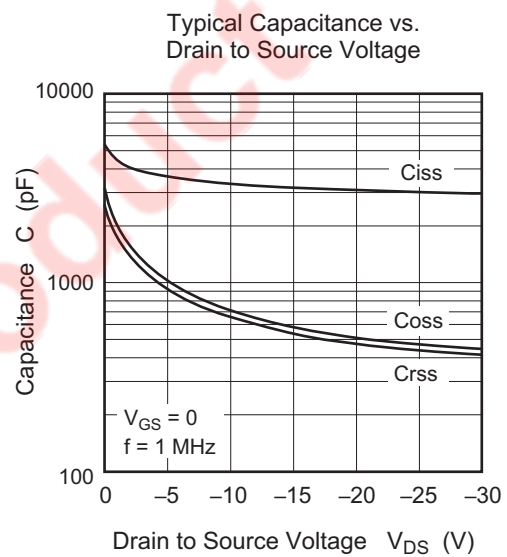
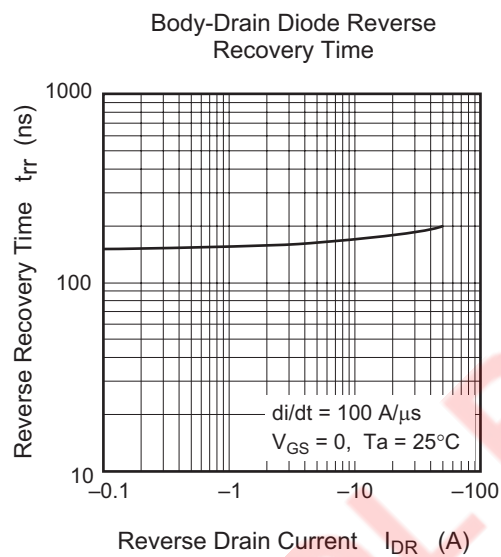
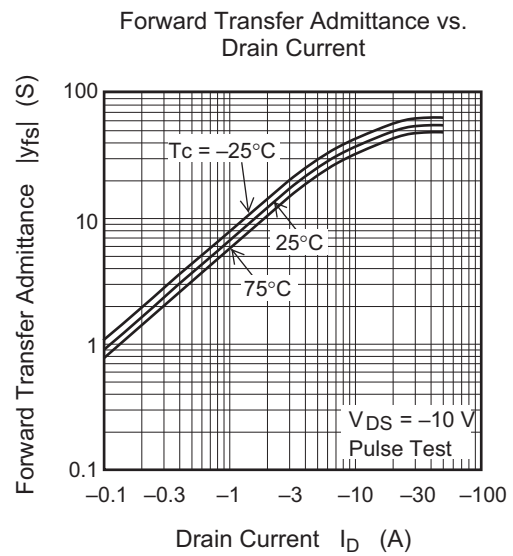
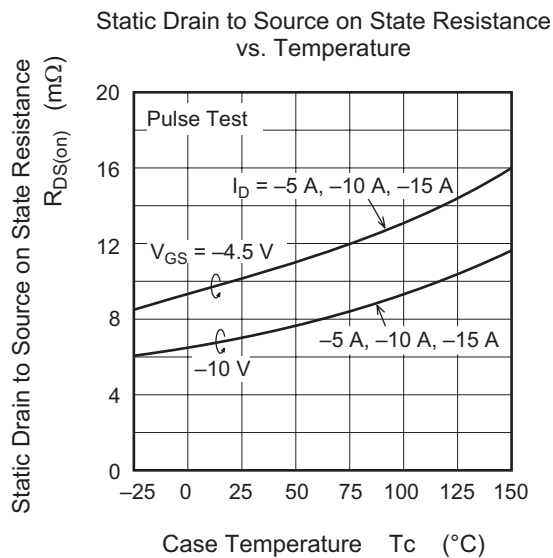


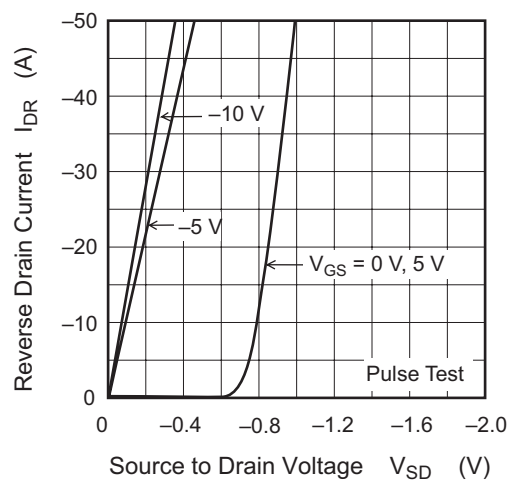
Drain to Source Saturation Voltage vs. Gate to Source Voltage



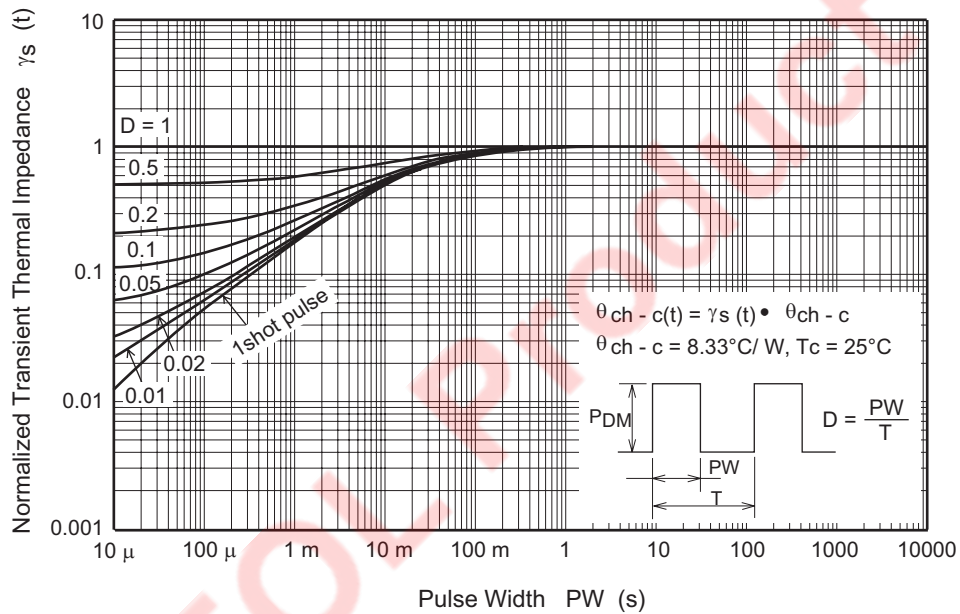
Static Drain to Source on State Resistance vs. Drain Current



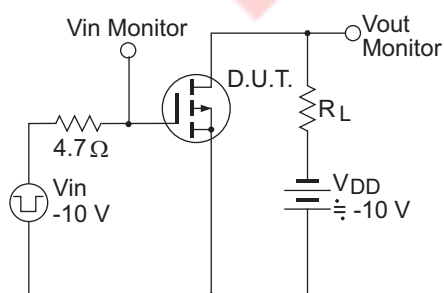


Reverse Drain Current vs.
Source to Drain Voltage

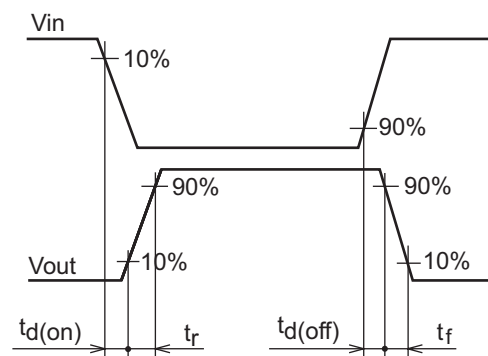
Normalized Transient Thermal Impedance vs. Pulse Width



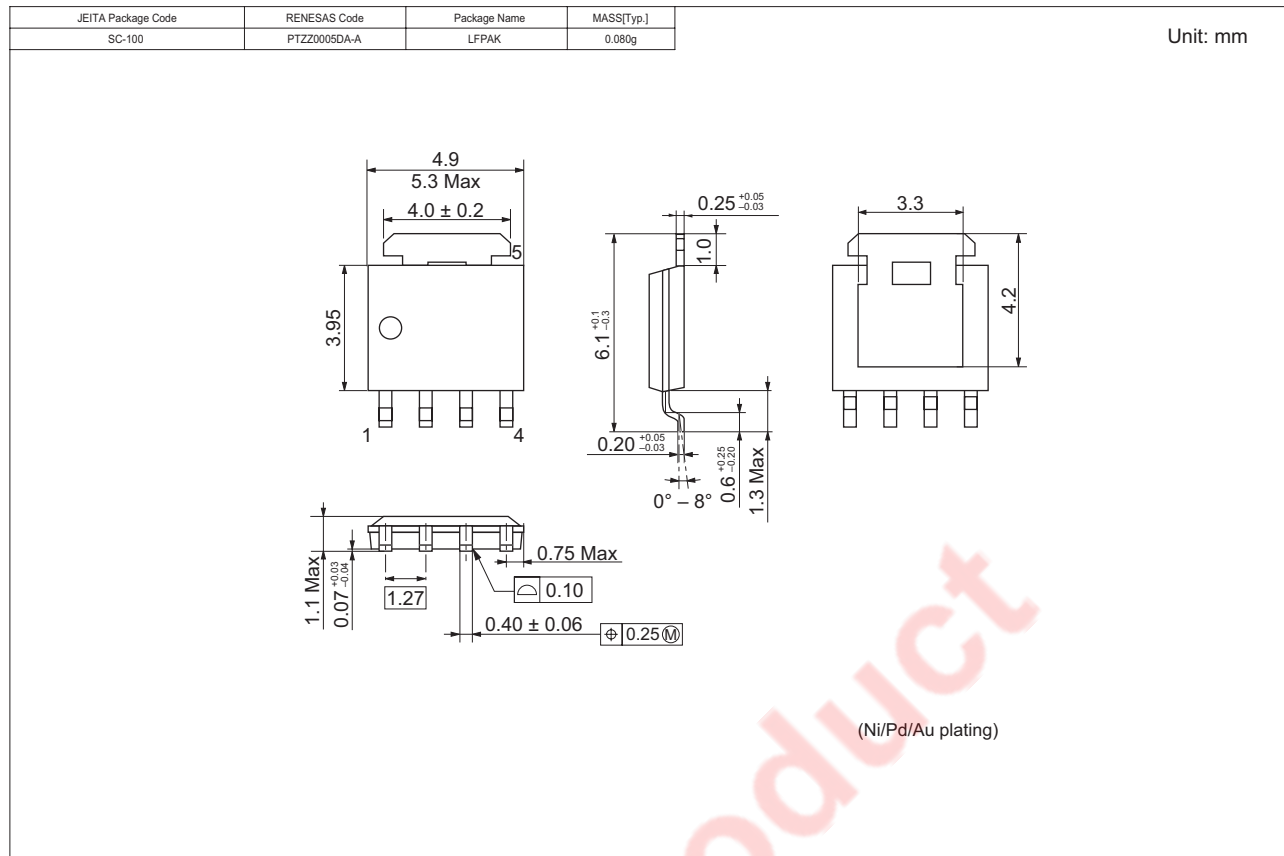
Switching Time Test Circuit



Waveform



Package Dimensions



Ordering Information

Part Name	Quantity	Shipping Container
HAT1139H-EL-E	2500 pcs	Taping

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