

N-Channel 25 V (D-S) MOSFET

PRODUCT SUMMARY

V_{DS} (V)	$R_{DS(on)}$ (Ω)	I_D (A) ^a	Q_g (Typ.)
25	0.0027 at $V_{GS} = 10$ V	36	49 nC
	0.0033 at $V_{GS} = 4.5$ V	29	

FEATURES

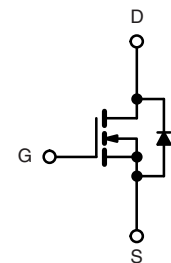
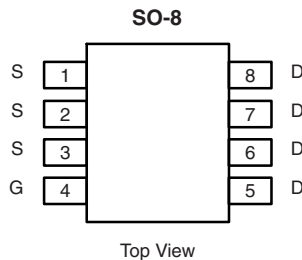
- Halogen-free According to IEC 61249-2-21 Definition
- Low Q_{gd}
- 100 % R_g Tested
- UIS and Capacitance Tested
- Compliant to RoHS Directive 2002/95/EC



RoHS
COMPLIANT
HALOGEN
FREE
Available

APPLICATIONS

- Synchronous Buck - Low Side
 - Notebook
 - Server
 - Workstation
- Synchronous Rectifier - POL



Ordering Information: Si4632DY-T1-E3 (Lead (Pb)-free)
Si4632DY-T1-GE3 (Lead (Pb)-free and Halogen-free)

N-Channel MOSFET

ABSOLUTE MAXIMUM RATINGS ($T_A = 25$ °C, unless otherwise noted)

Parameter	Symbol	Limit	Unit
Drain-Source Voltage	V_{DS}	25	V
Gate-Source Voltage	V_{GS}	± 16	
Continuous Drain Current ($T_J = 150$ °C)	I_D	$T_C = 25$ °C	40
		$T_C = 70$ °C	32
		$T_A = 25$ °C	27 ^{b, c}
		$T_A = 70$ °C	21 ^{b, c}
Pulsed Drain Current	I_{DM}	70	A
Continuous Source-Drain Diode Current	I_S	$T_C = 25$ °C	7.0
		$T_A = 25$ °C	3.0 ^{b, c}
Single Pulse Avalanche Current	I_{AS}	30	
Avalanche Energy	E_{AS}	45	mJ
Maximum Power Dissipation	P_D	$T_C = 25$ °C	7.8
		$T_C = 70$ °C	5.0
		$T_A = 25$ °C	3.5 ^{b, c}
		$T_A = 70$ °C	2.2 ^{b, c}
Operating Junction and Storage Temperature Range	T_J, T_{stg}	- 55 to 150	

THERMAL RESISTANCE RATINGS

Parameter	Symbol	Typical	Maximum	Unit
Maximum Junction-to-Ambient ^{b, d}	R_{thJA}	29	35	°C/W
Maximum Junction-to-Foot (Drain)	R_{thJF}	13	16	

Notes:

- Based on $T_C = 25$ °C.
- Surface mounted on 1" x 1" FR4 board.
- $t = 5$ s.
- Maximum under steady state conditions is 125 °C/W.

SPECIFICATIONS (T _J = 25 °C, unless otherwise noted)						
Parameter	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
Static						
Drain-Source Breakdown Voltage	V _{DS}	V _{GS} = 0 V, I _D = 250 μA	25			V
V _{DS} Temperature Coefficient	ΔV _{DS} /T _J	I _D = 250 μA		23		mV/°C
V _{GS(th)} Temperature Coefficient	ΔV _{GS(th)} /T _J			- 6		
Gate-Source Threshold Voltage	V _{GS(th)}	V _{DS} = V _{GS} , I _D = 250 μA	1.2		2.6	V
Gate-Source Leakage	I _{GSS}	V _{DS} = 0 V, V _{GS} = ± 16 V			± 100	nA
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} = 25 V, V _{GS} = 0 V			1	μA
		V _{DS} = 25 V, V _{GS} = 0 V, T _J = 55 °C			10	
On-State Drain Current ^a	I _{D(on)}	V _{DS} = ≥ 5 V, V _{GS} = 10 V	30			A
Drain-Source On-State Resistance ^a	R _{DS(on)}	V _{GS} = 10 V, I _D = 20 A		0.0022	0.0027	Ω
		V _{GS} = 4.5 V, I _D = 15 A		0.0027	0.0033	
Forward Transconductance ^a	g _{fs}	V _{DS} = 15 V, I _D = 20 A		73		S
Dynamic ^b						
Input Capacitance	C _{iss}	V _{DS} = 15 V, V _{GS} = 0 V, f = 1 MHz	3275	7450	11175	pF
Output Capacitance	C _{oss}		495	990	1485	
Reverse Transfer Capacitance	C _{rss}		230	460	690	
Total Gate Charge	Q _g	V _{DS} = 15 V, V _{GS} = 10 V, I _D = 20 A		108	161	nC
Gate-Source Charge	Q _{gs}	V _{DS} = 15 V, V _{GS} = 4.5 V, I _D = 20 A		49	73	
Gate-Drain Charge	Q _{gd}			19		
Gate Resistance	R _g			11		
		f = 1 MHz		1.3	2.0	Ω
Turn-On Delay Time	t _{d(on)}	V _{DD} = 15 V, R _L = 1.5 Ω I _D ≡ 10 A, V _{GEN} = 4.5 V, R _g = 1 Ω		42	65	ns
Rise Time	t _r			115	175	
Turn-Off DelayTime	t _{d(off)}			55	85	
Fall Time	t _f			14	23	
Turn-On Delay Time	t _{d(on)}	V _{DD} = 15 V, R _L = 1.5 Ω I _D ≡ 10 A, V _{GEN} = 10 V, R _g = 1 Ω		20	30	
Rise Time	t _r			69	105	
Turn-Off DelayTime	t _{d(off)}			58	90	
Fall Time	t _f			8	15	
Drain-Source Body Diode Characteristics						
Continous Source-Drain Diode Current	I _S	T _C = 25 °C			7	A
Pulse Diode Forward Current ^a	I _{SM}				70	
Body Diode Voltage	V _{SD}	I _S = 3 A		0.75	1.1	V
Body Diode Reverse Recovery Time	t _{rr}	I _F = 13 A, dI/dt = 100 A/μs, T _J = 25 °C		44	70	ns
Body Diode Reverse Recovery Charge	Q _{rr}			42	65	nC
Reverse Recovery Fall Time	t _a			22		ns
Reverse Recovery Rise Time	t _b			22		

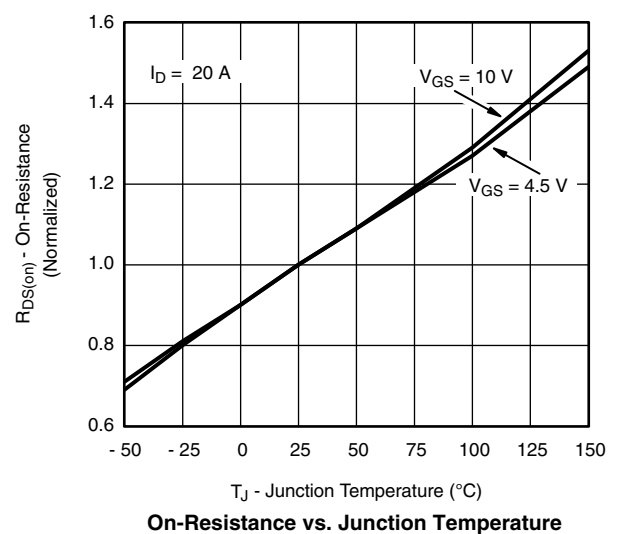
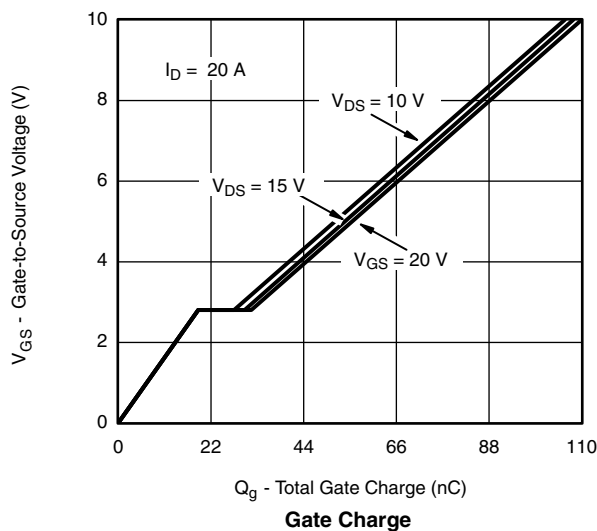
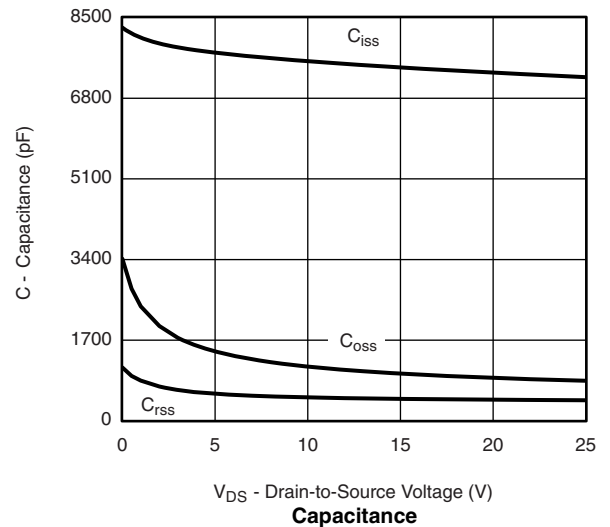
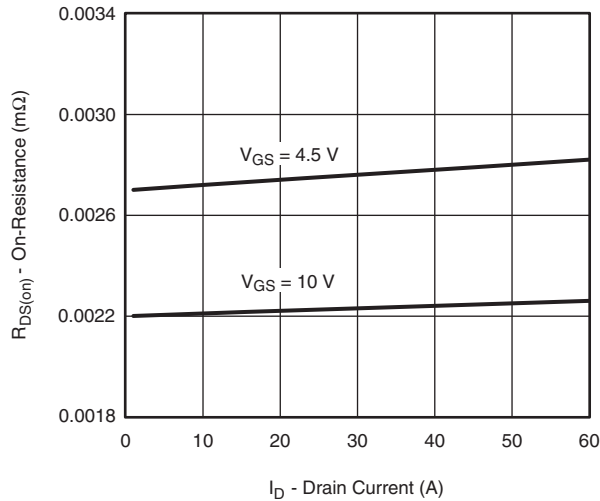
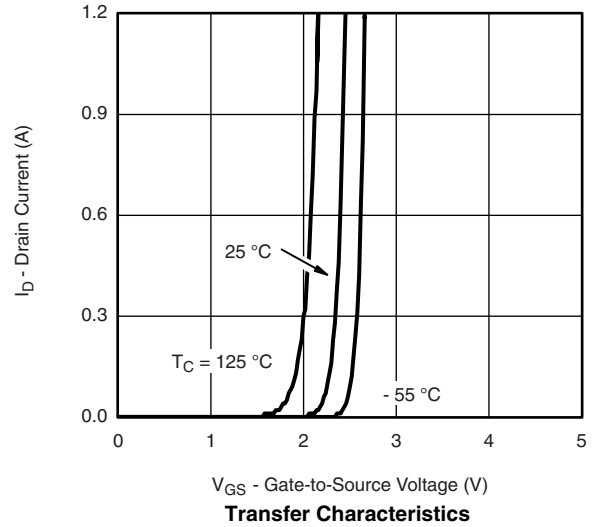
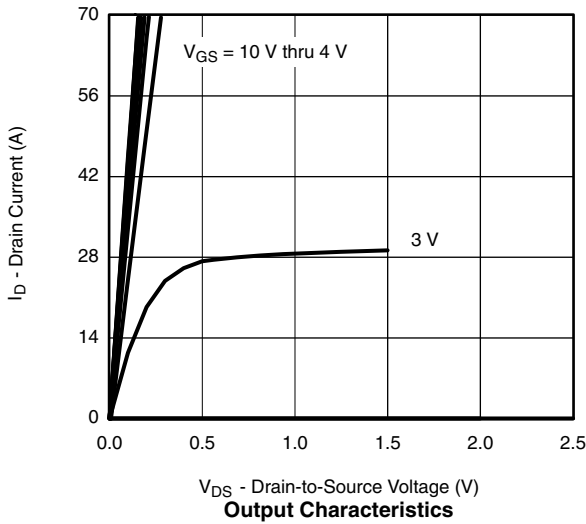
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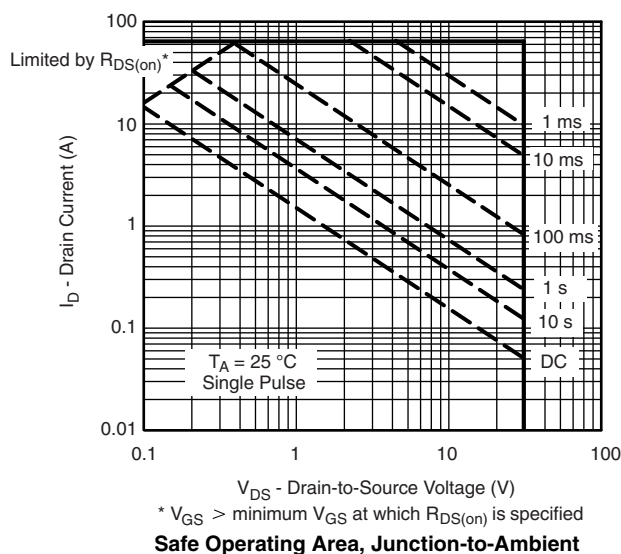
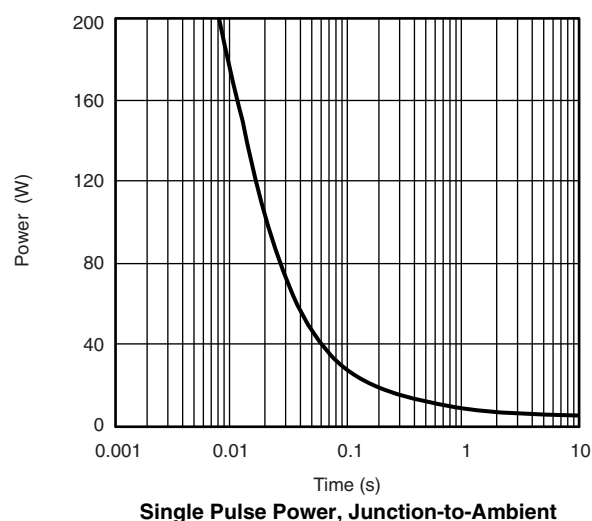
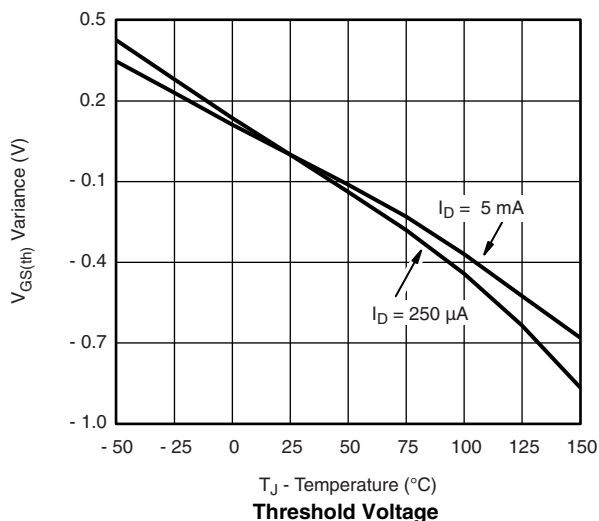
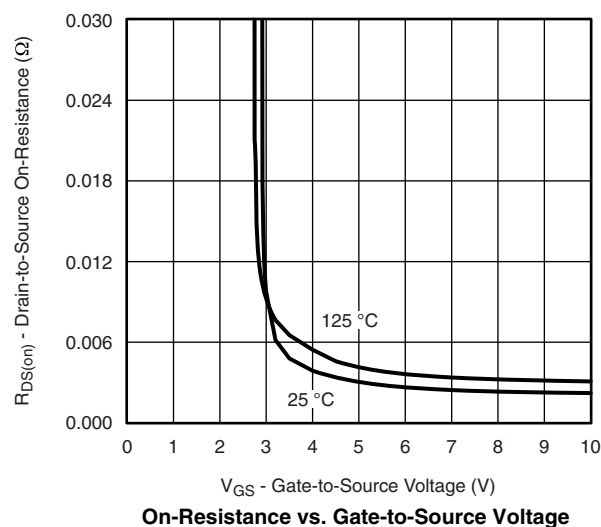
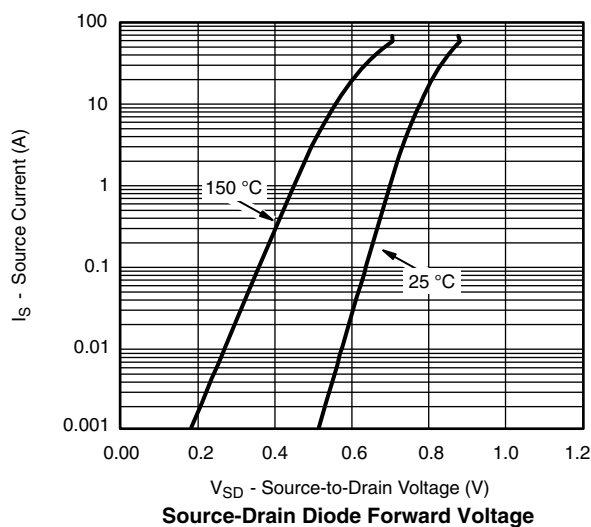
a. Pulse test; pulse width $\leq 300\text{ }\mu\text{s}$, duty cycle $\leq 2\%$.

b. Guaranteed by design, not subject to production testing.

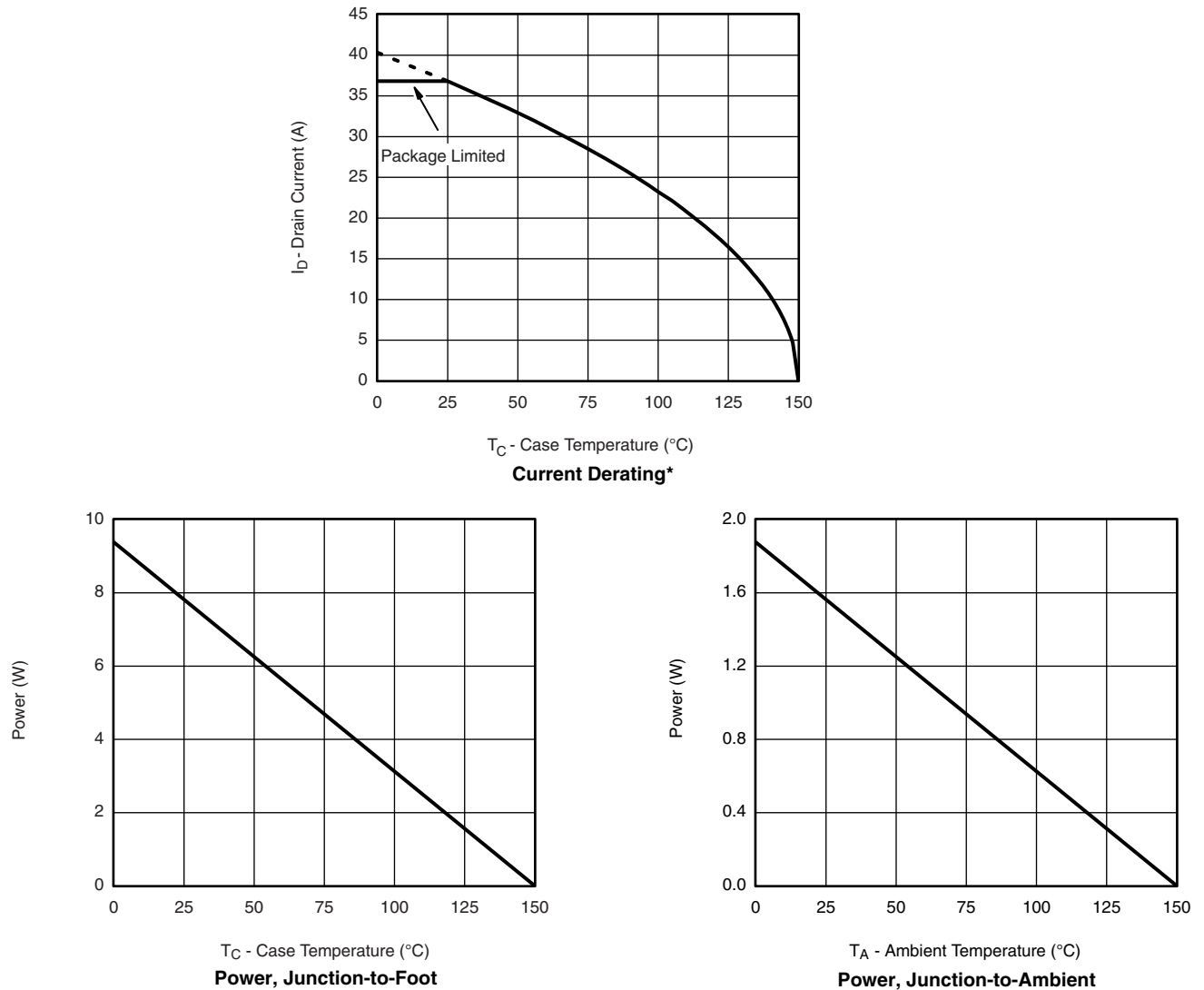
Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

TYPICAL CHARACTERISTICS ($T_A = 25^\circ\text{C}$, unless otherwise noted)

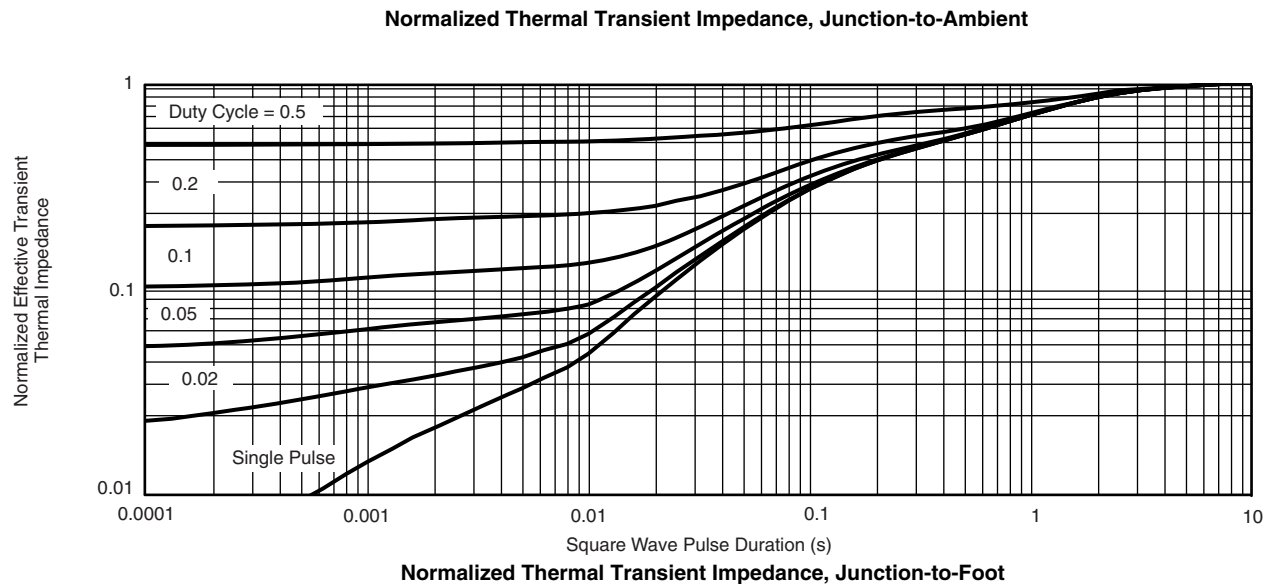
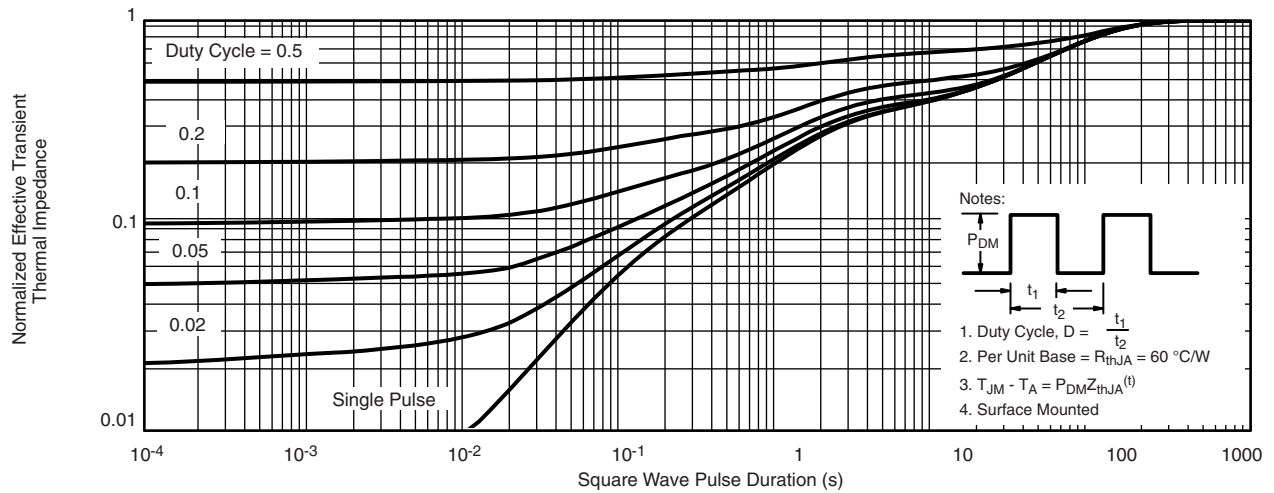


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* The power dissipation P_D is based on $T_{J(\max)} = 150\text{ }^{\circ}\text{C}$, using junction-to-case thermal resistance, and is more useful in settling the upper dissipation limit for cases where additional heatsinking is used. It is used to determine the current rating, when this rating falls below the package limit.

TYPICAL CHARACTERISTICS ($T_A = 25\text{ }^{\circ}\text{C}$, unless otherwise noted)

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