

August 1997

Features

- 31A, 55V
- **Ultra Low On-Resistance**, $r_{DS(ON)} = 0.032\Omega$
- Diode Exhibits Both High Speed and Soft Recovery
- **Temperature Compensating PSPICE Model**
- **Thermal Impedance PSPICE Model**
- **Peak Current vs Pulse Width Curve**
- **UIS Rating Curve**

Ordering Information

PART NUMBER	PACKAGE	BRAND
HUF75321P3	TO-220AB	75321P
HUF75321S3	TO-262AA	75321S
HUF75321S3S	TO-263AB	75321S

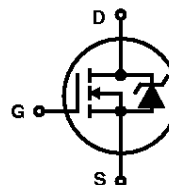
NOTE: When ordering, use the entire part number. Add the suffix T to obtain the TO-263AB variant in tape and reel, e.g., HUF75321S3ST.

Description

The HUF75321 N-Channel power MOSFET is manufactured using the innovative *UltraFET™* process. This advanced process technology achieves the lowest possible on-resistance per silicon area, resulting in outstanding performance. This device is capable of withstanding high energy in the avalanche mode and the diode exhibits very low reverse recovery time and stored charge. It was designed for use in applications where power efficiency is important, such as switching regulators, switching converters, motor drivers, relay drivers, low-voltage bus switches, and power management in portable and battery-operated products.

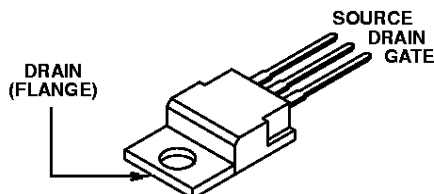
Formerly developmental type TA75321.

Symbol

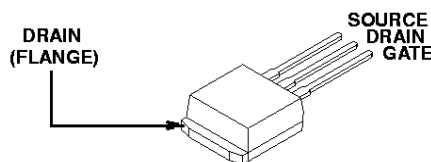


Packaging

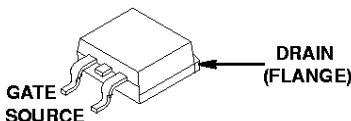
JEDEC TO-220AB



JEDEC TO-262AA



JEDEC TO-263AB



HUF75321P3, HUF75321S3, HUF75321S3S

Absolute Maximum Ratings $T_C = 25^\circ\text{C}$, Unless Otherwise Specified

Drain to Source Voltage	V_{DSS}	55	V
Drain to Gate Voltage ($R_{GS} = 20\text{k}\Omega$) (Note 1)	V_{DGR}	55	V
Gate to Source Voltage	V_{GS}	± 20	V
Drain Current			
Continuous (Figure 2)	I_D	31	A
Pulsed Drain Current	I_{DM}	Figure 5	
Pulsed Avalanche Rating	E_{AS}	Figures 12,14,15	
Power Dissipation (Figure 4)	P_D	70	W
Derate Above 25°C (Figure 1)		0.47	W/ $^\circ\text{C}$
Operating and Storage Temperature	T_J, T_{STG}	-55 to 175	$^\circ\text{C}$
Soldering Temperature of Leads for 10s	T_L	260	$^\circ\text{C}$

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied

NOTE:

1. $T_J = 25^\circ\text{C}$ to 150°C .

Electrical Specifications $T_C = 25^\circ\text{C}$, Unless Otherwise Specified

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Drain to Source Breakdown Voltage	BV_{DSS}	$I_D = 250\mu\text{A}$, $V_{GS} = 0\text{V}$ (Figure 10)	55	-	-	V
Gate to Source Threshold Voltage	$V_{GS(TH)}$	$V_{GS} = V_{DS}$, $I_D = 250\mu\text{A}$ (Figure 9)	2	-	4	V
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS} = 50\text{V}$, $V_{GS} = 0\text{V}$	-	-	1	μA
		$V_{DS} = 45\text{V}$, $V_{GS} = 0\text{V}$, $T_C = 150^\circ\text{C}$	-	-	250	μA
Gate to Source Leakage Current	I_{GSS}	$V_{GS} = \pm 20\text{V}$	-	-	100	nA
Drain to Source On Resistance	$r_{DS(ON)}$	$I_D = 31\text{A}$, $V_{GS} = 10\text{V}$ (Figure 8)	-	-	0.032	Ω
Turn-On Time	t_{ON}	$V_{DD} = 30\text{V}$, $I_D \cong 31\text{A}$, $R_L = 0.968\Omega$, $V_{GS} = 10\text{V}$, $R_{GS} = 25\Omega$ (Figures 18,19)	-	-	100	ns
Turn-On Delay Time	$t_{d(ON)}$		-	11	-	ns
Rise Time	t_r		-	55	-	ns
Turn-Off Delay Time	$t_{d(OFF)}$		-	47	-	ns
Fall Time	t_f		-	66	-	ns
Turn-Off Time	t_{OFF}		-	-	170	ns
Total Gate Charge	$Q_g(TOT)$	$V_{GS} = 0\text{V}$ to 20V	-	36	44	nC
Gate Charge at 10V	$Q_g(10)$	$V_{GS} = 0\text{V}$ to 10V	-	21	26	nC
Threshold Gate Charge	$Q_g(TH)$	$V_{GS} = 0\text{V}$ to 2V	-	1.3	1.6	nC
Input Capacitance	C_{ISS}	$V_{DS} = 25\text{V}$, $V_{GS} = 0\text{V}$, $f = 1\text{MHz}$ (Figure 11)	-	709	-	pF
			-	270	-	pF
			-	64	-	pF
Reverse Transfer Capacitance	C_{RSS}		-	-	-	pF
Thermal Resistance Junction to Case	$R_{\theta JC}$	(Figure 3)	-	-	2.15	$^\circ\text{C/W}$
Thermal Resistance Junction to Ambient	$R_{\theta JA}$	TO-247	-	-	30	$^\circ\text{C/W}$
		TO-220, TO-262, and TO-263	-	-	62	$^\circ\text{C/W}$

Source to Drain Diode Specifications

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Source to Drain Diode Voltage	V_{SD}	$I_{SD} = 31\text{A}$	-	-	1.25	V
Reverse Recovery Time	t_{rr}	$I_{SD} = 31\text{A}$, $dI_{SD}/dt = 100\text{A}/\mu\text{s}$	-	-	59	ns
Reverse Recovered Charge	Q_{RR}	$I_{SD} = 31\text{A}$, $dI_{SD}/dt = 100\text{A}/\mu\text{s}$	-	-	82	nC

Typical Performance Curves

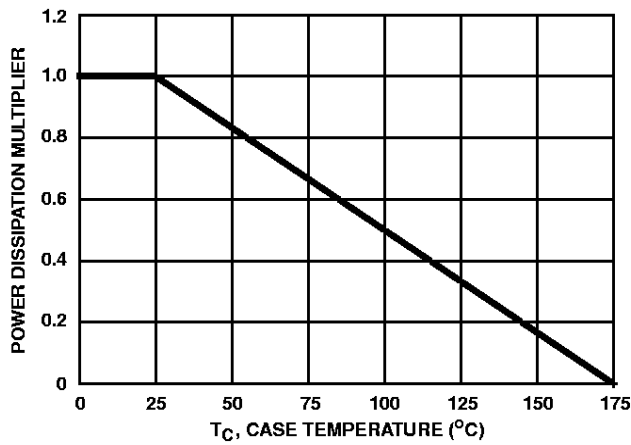


FIGURE 1. NORMALIZED POWER DISSIPATION vs CASE TEMPERATURE

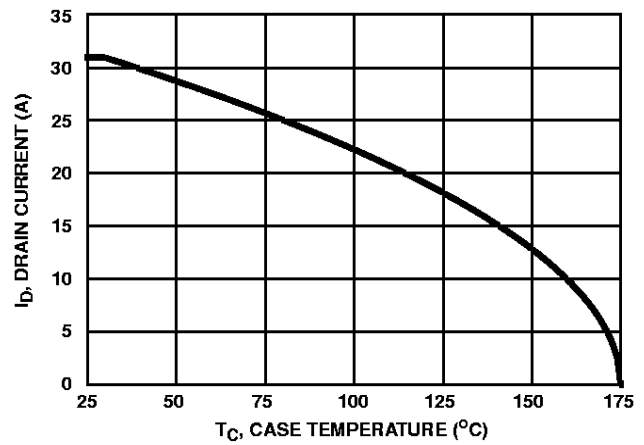


FIGURE 2. MAXIMUM CONTINUOUS DRAIN CURRENT vs CASE TEMPERATURE

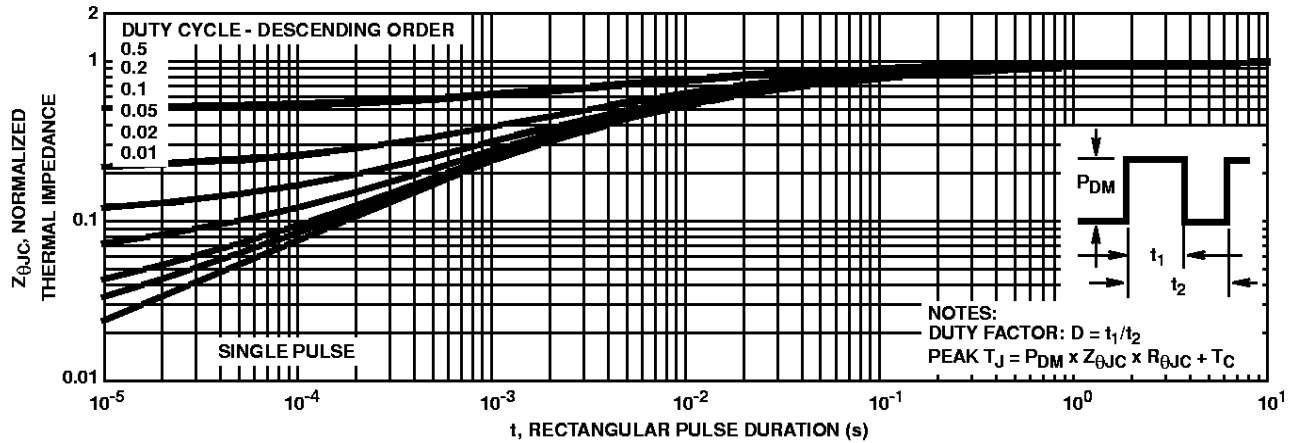


FIGURE 3. NORMALIZED MAXIMUM TRANSIENT THERMAL IMPEDANCE

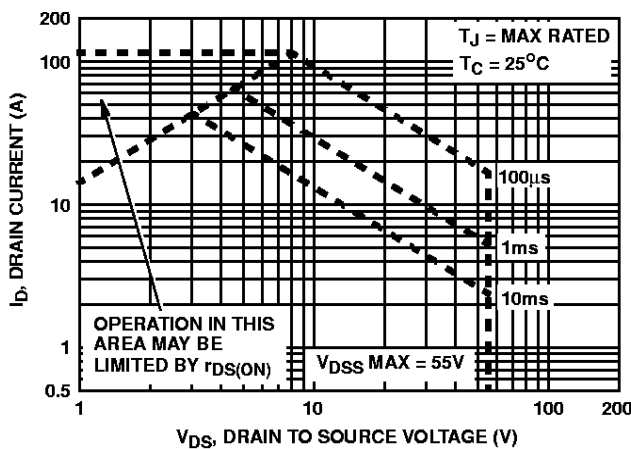


FIGURE 4. FORWARD BIAS SAFE OPERATING AREA

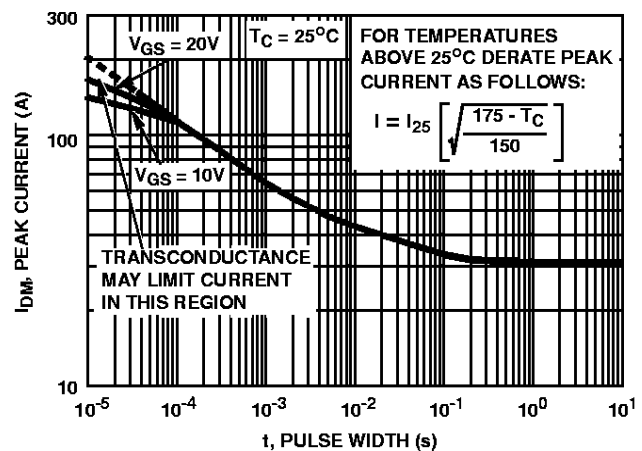


FIGURE 5. PEAK CURRENT CAPABILITY

Typical Performance Curves (Continued)

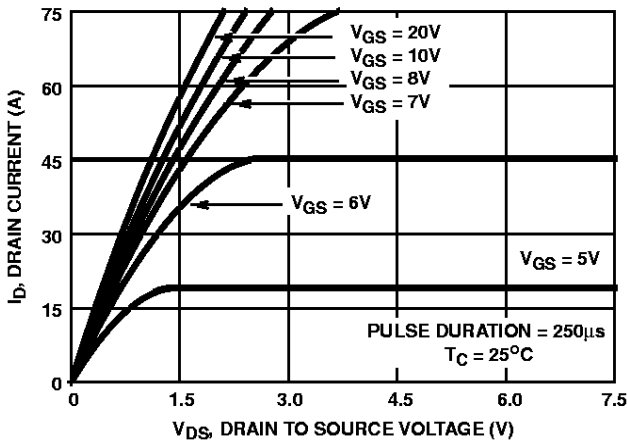


FIGURE 6. SATURATION CHARACTERISTICS

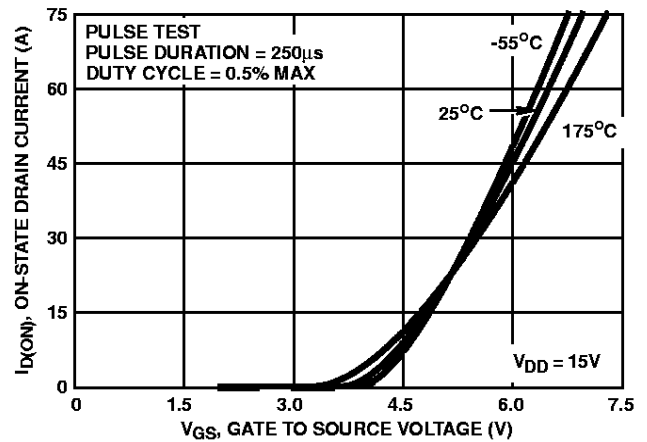


FIGURE 7. TRANSFER CHARACTERISTICS

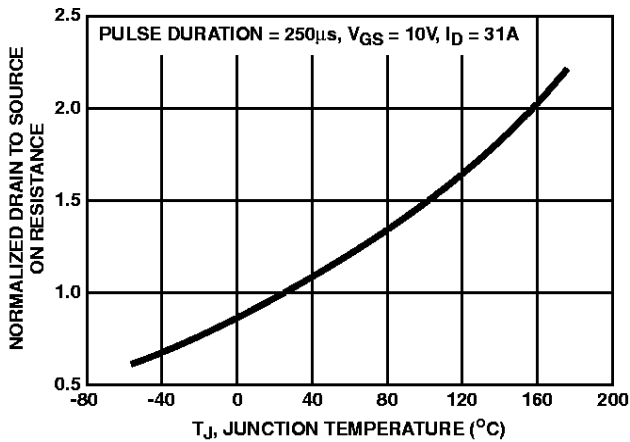


FIGURE 8. NORMALIZED DRAIN TO SOURCE ON RESISTANCE vs JUNCTION TEMPERATURE

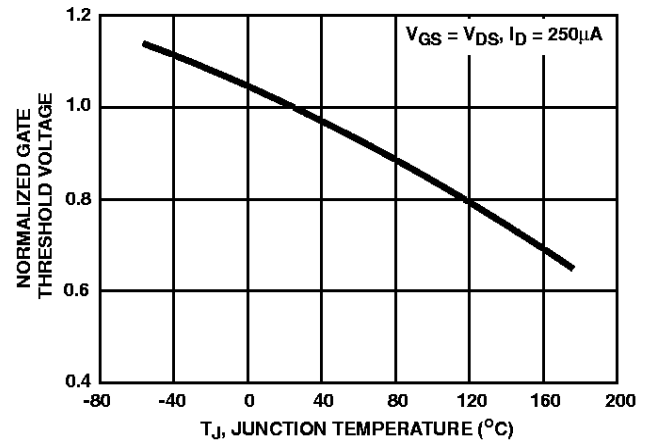


FIGURE 9. NORMALIZED GATE THRESHOLD VOLTAGE vs JUNCTION TEMPERATURE

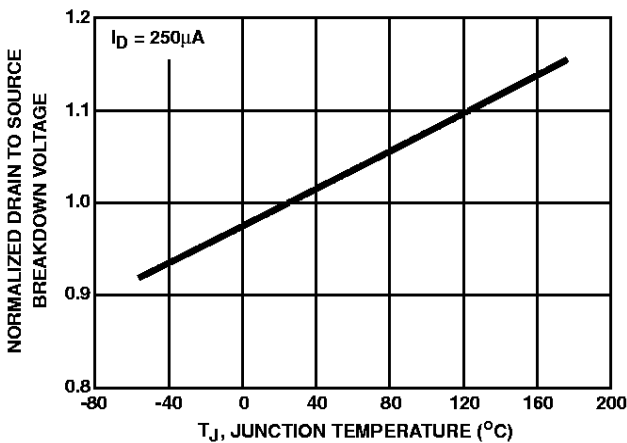


FIGURE 10. NORMALIZED DRAIN TO SOURCE BREAKDOWN VOLTAGE vs JUNCTION TEMPERATURE

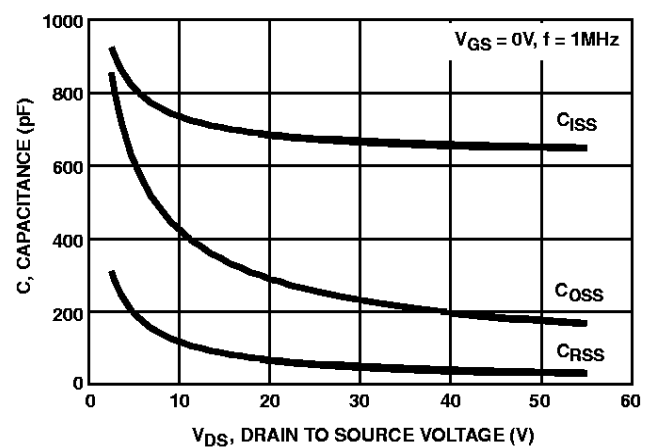
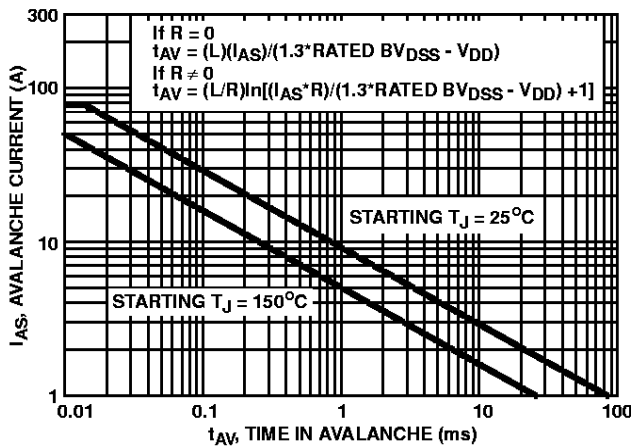


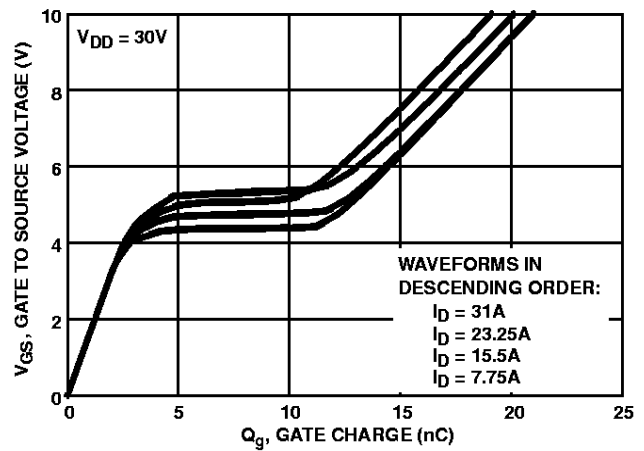
FIGURE 11. CAPACITANCE vs DRAIN TO SOURCE VOLTAGE

Typical Performance Curves (Continued)



NOTE: Refer to Harris Application Notes AN9321 and AN9322.

FIGURE 12. UNCLAMPED INDUCTIVE SWITCHING CAPABILITY



NOTE: Refer to Harris Application Notes AN7254 and AN7260.

FIGURE 13. GATE CHARGE WAVEFORMS FOR CONSTANT GATE CURRENT

Test Circuits and Waveforms

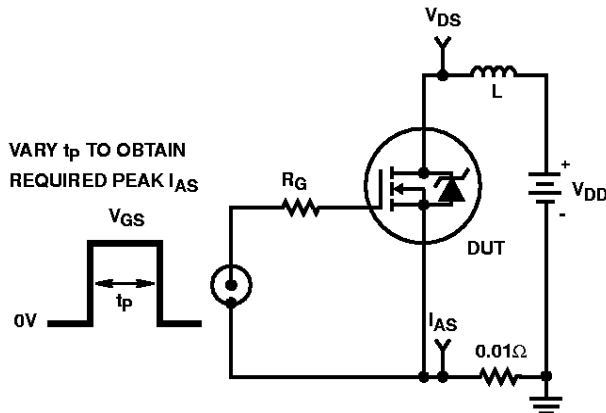


FIGURE 14. UNCLAMPED ENERGY TEST CIRCUIT

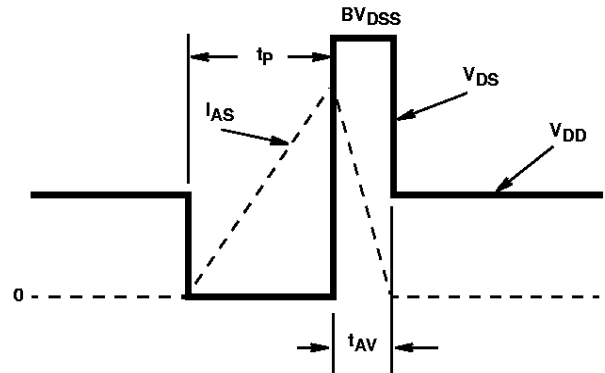


FIGURE 15. UNCLAMPED ENERGY WAVEFORMS

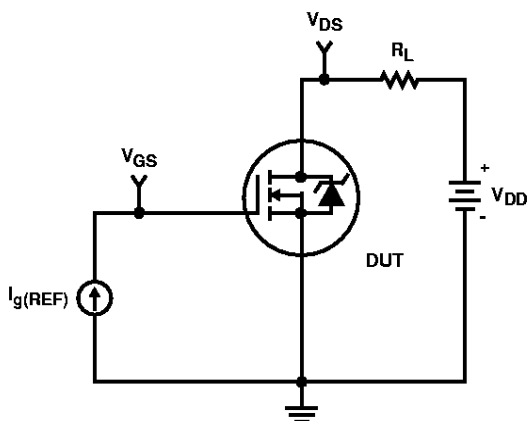


FIGURE 16. GATE CHARGE TEST CIRCUIT

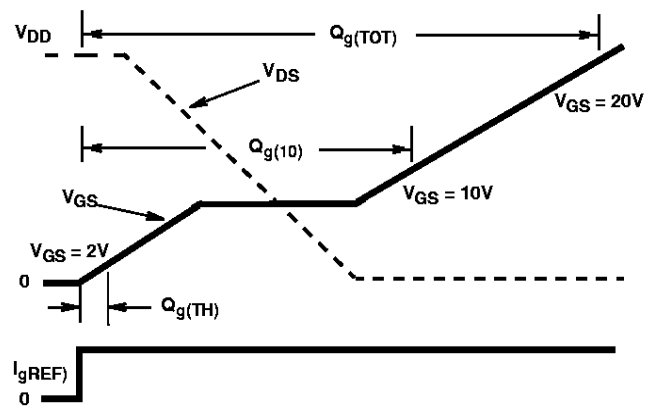


FIGURE 17. GATE CHARGE WAVEFORM

Test Circuits and Waveforms (Continued)

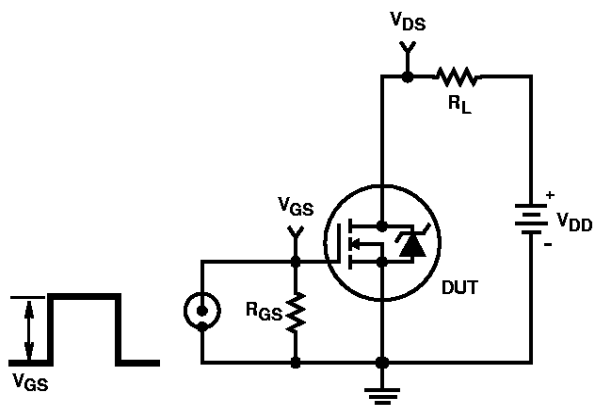


FIGURE 18. SWITCHING TIME TEST CIRCUIT

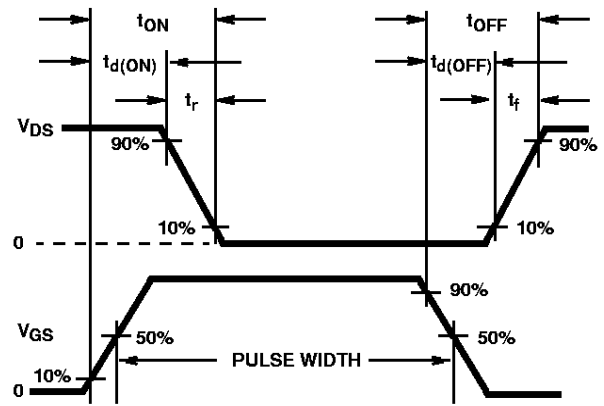


FIGURE 19. RESISTIVE SWITCHING WAVEFORMS

HUF75321P3, HUF75321S3, HUF75321S3S

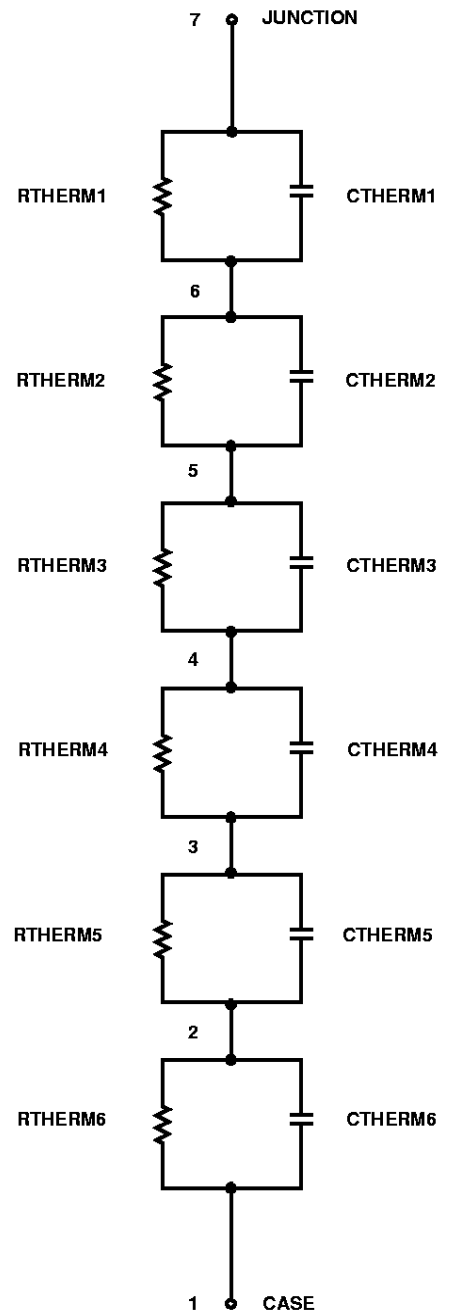
PSPICE Thermal Model

REV 13June 97

HUF75321

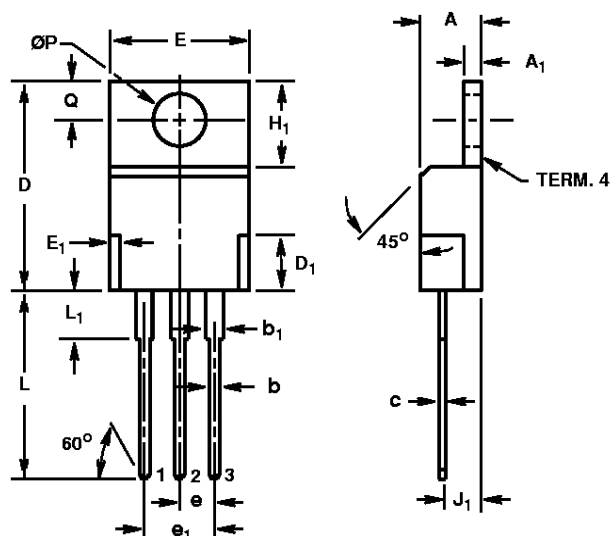
CTHERM1 7 6 4.90e-7
 CHERM2 6 5 4.50e-4
 CHERM3 5 4 1.62e-3
 CHERM4 4 3 1.30e-2
 CHERM5 3 2 1.20e-1
 CHERM6 2 1 1.20

RHERM1 7 6 2.40e-2
 RHERM2 6 5 7.80e-2
 RHERM3 5 4 4.55e-1
 RHERM4 4 3 6.80e-1
 RHERM5 3 2 4.10e-1
 RHERM6 2 1 3.90e-1



TO-220AB

3 LEAD JEDEC TO-220AB PLASTIC PACKAGE



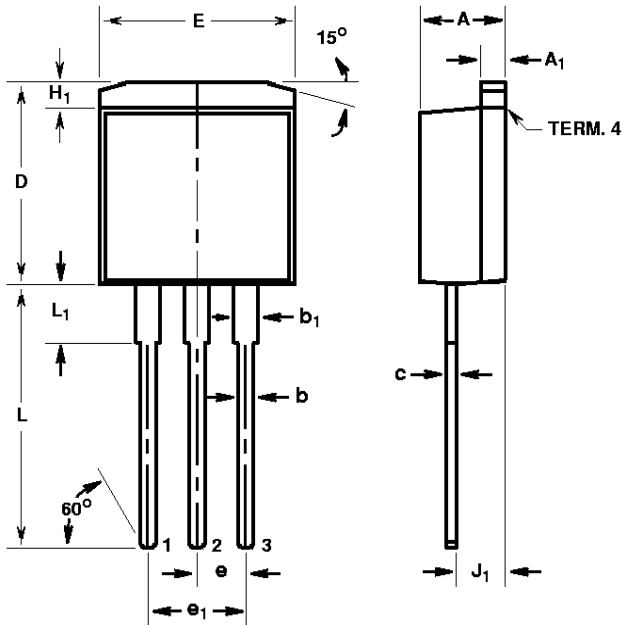
SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.170	0.180	4.32	4.57	-
A ₁	0.048	0.052	1.22	1.32	-
b	0.030	0.034	0.77	0.86	3, 4
b ₁	0.045	0.055	1.15	1.39	2, 3
c	0.014	0.019	0.36	0.48	2, 3, 4
D	0.590	0.610	14.99	15.49	-
D ₁	-	0.160	-	4.06	-
E	0.395	0.410	10.04	10.41	-
E ₁	-	0.030	-	0.76	-
e	0.100 TYP		2.54 TYP		5
e ₁	0.200 BSC		5.08 BSC		5
H ₁	0.235	0.255	5.97	6.47	-
J ₁	0.100	0.110	2.54	2.79	6
L	0.530	0.550	13.47	13.97	-
L ₁	0.130	0.150	3.31	3.81	2
ØP	0.149	0.153	3.79	3.88	-
Q	0.102	0.112	2.60	2.84	-

NOTES:

1. These dimensions are within allowable dimensions of Rev. J of JEDEC TO-220AB outline dated 3-24-87.
2. Lead dimension and finish uncontrolled in L₁.
3. Lead dimension (without solder).
4. Add typically 0.002 inches (0.05mm) for solder coating.
5. Position of lead to be measured 0.250 inches (6.35mm) from bottom of dimension D.
6. Position of lead to be measured 0.100 inches (2.54mm) from bottom of dimension D.
7. Controlling dimension: Inch.
8. Revision 2 dated 7-97.

HUF75321P3, HUF75321S3, HUF75321S3S

TO-262AA 3 LEAD JEDEC TO-262AA PLASTIC PACKAGE

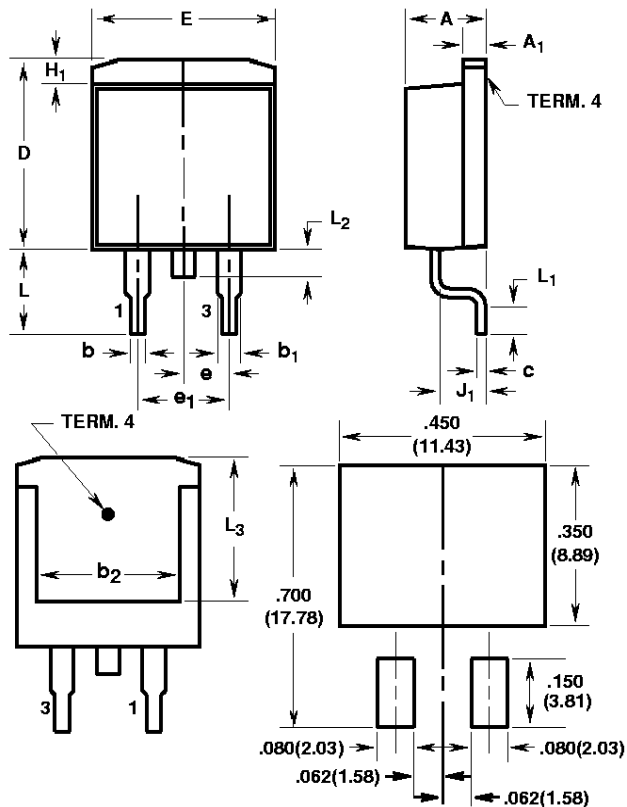


SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.170	0.180	4.32	4.57	-
A ₁	0.048	0.052	1.22	1.32	3, 4
b	0.030	0.034	0.77	0.86	3, 4
b ₁	0.045	0.055	1.15	1.39	3, 4
c	0.018	0.022	0.46	0.55	3, 4
D	0.405	0.425	10.29	10.79	-
E	0.395	0.405	10.04	10.28	-
e	0.100 TYP		2.54 TYP		5
e ₁	0.200 BSC		5.08 BSC		5
H ₁	0.045	0.055	1.15	1.39	-
J ₁	0.095	0.105	2.42	2.66	6
L	0.530	0.550	13.47	13.97	-
L ₁	0.110	0.130	2.80	3.30	2

NOTES:

- These dimensions are within allowable dimensions of Rev. A of JEDEC TO-262AA outline dated 6-90.
- Solder finish uncontrolled in this area.
- Dimension (without solder).
- Add typically 0.002 inches (0.05mm) for solder plating.
- Position of lead to be measured 0.250 inches (6.35mm) from bottom of dimension D.
- Position of lead to be measured 0.100 inches (2.54mm) from bottom of dimension D.
- Controlling dimension: Inch.
- Revision 5 dated 7-97.

TO-263AB SURFACE MOUNT JEDEC TO-263AB PLASTIC PACKAGE



SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.170	0.180	4.32	4.57	-
A ₁	0.048	0.052	1.22	1.32	4, 5
b	0.030	0.034	0.77	0.86	4, 5
b ₁	0.045	0.055	1.15	1.39	4, 5
b ₂	0.310	-	7.88	-	2
c	0.018	0.022	0.46	0.55	4, 5
D	0.405	0.425	10.29	10.79	-
E	0.395	0.405	10.04	10.28	-
e	0.100 TYP		2.54 TYP		7
e ₁	0.200 BSC		5.08 BSC		7
H ₁	0.045	0.055	1.15	1.39	-
J ₁	0.095	0.105	2.42	2.66	-
L	0.175	0.195	4.45	4.95	-
L ₁	0.090	0.110	2.29	2.79	4, 6
L ₂	0.050	0.070	1.27	1.77	3
L ₃	0.315	-	8.01	-	2

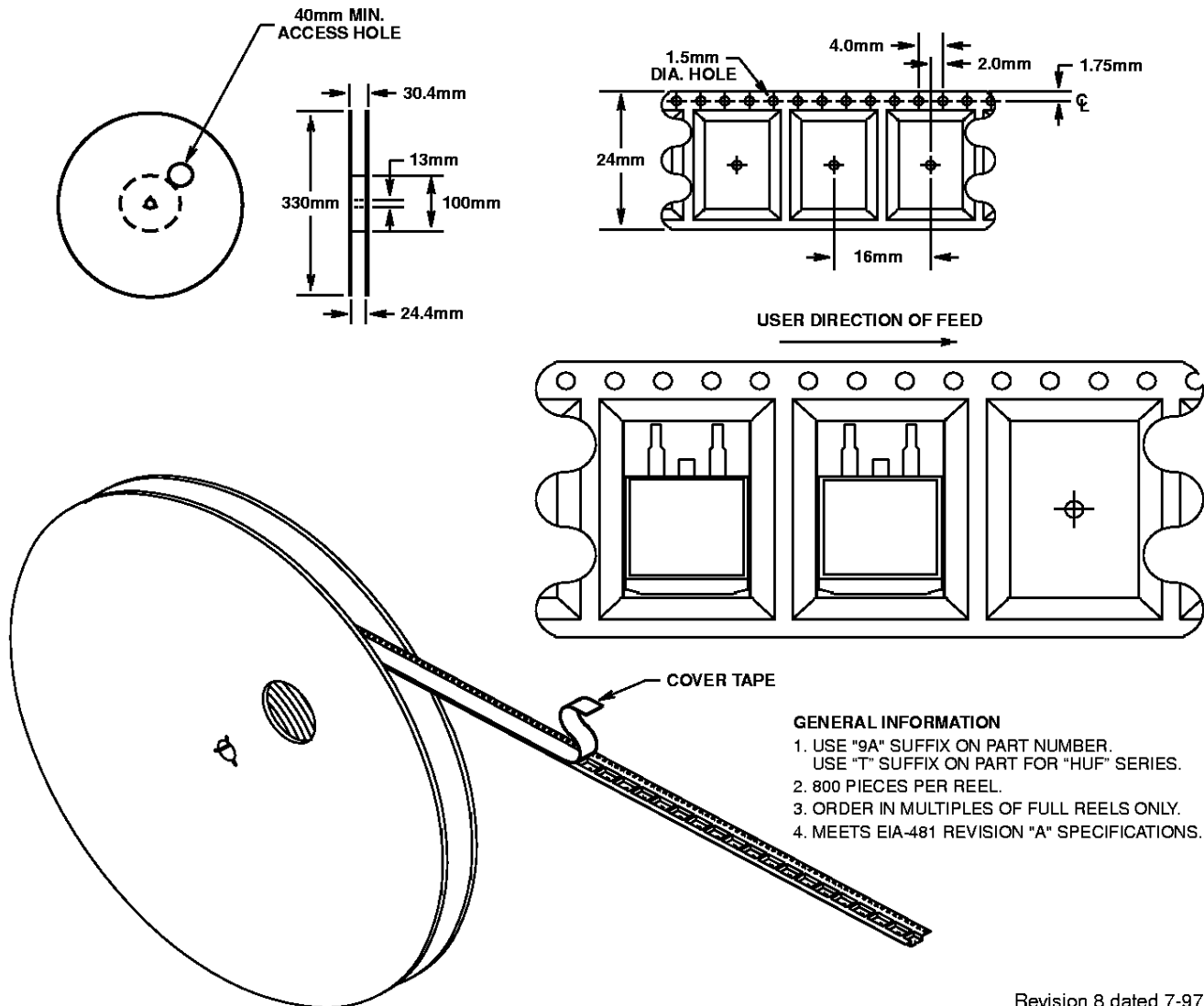
NOTES:

- These dimensions are within allowable dimensions of Rev. C of JEDEC TO-263AB outline dated 2-92.
- L₃ and b₂ dimensions established a minimum mounting surface for terminal 4.
- Solder finish uncontrolled in this area.
- Dimension (without solder).
- Add typically 0.002 inches (0.05mm) for solder plating.
- L₁ is the terminal length for soldering.
- Position of lead to be measured 0.120 inches (3.05mm) from bottom of dimension D.
- Controlling dimension: Inch.
- Revision 8 dated 7-97.

MINIMUM PAD SIZE RECOMMENDED FOR SURFACE-MOUNTED APPLICATIONS

TO-263AB

24mm TAPE AND REEL



Revision 8 dated 7-97

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